POWER SYSTEM PROTECTION & CONTROL
STAGE 2B-PSP102

TEXTBOOK/WORKBOOK

POWER SYSTEM PROTECTION & CONTROL

STAGE 2B-PSP102

Textbook/Workbook

TABLE OF CONTENTS

POWER SYSTEM PROTECTION & CONTROL

STAGE 2B-PSP102

COURSE OVERVIEW

OVERVIEW

After completion of this course, the trainee will achieve the necessary knowledge and skills to identify the different types of electromechanical protective relays, the main protection schemes, the features of relay test equipment, and brief idea about digital systems, and their applications.

OBJECTIVES

Upon completion of this course, the trainees will be able to:

- Demonstrate the different types of electromechanical relays.

- Illustrate the protection schemes and their applications.

- Familiarize with digital systems and their applications.

CONTENTS

The contents of the (2B) course material are divided into three (3) units of instructions with eighteen (18) lessons.

Text and workshop material

Unit 1   Types of Electromechanical Protective Relays.

Unit 2   Types of Protection Schemes.

Unit 3   Introduction to Digital Systems.

DURATION

This course is for duration of nine (9) weeks to cover theoretical part, practical tasks, and field visits.

POWER SYSTEM PROTECTION & CONTROL
STAGE 2B-PSP102

PACING SCHEDULE

TEXTBOOK/WORKBOOK

Unit	Description	Duration (Hours)
1	Types of electromechanical protective relays	65
2	Types of protection schemes	70
3	Introduction to digital systems	65
	TOTAL	**200**

SAFETY PRECAUTIONS FOR RELAYS WORKSHOP

1. Before injecting electricity, check the relay terminals from the catalog.

2. Check also the suitable amount of current and voltage that required to the relay.

3. Place the relays in its recommended position before performing the tasks.

4. Adjusting and calibration to the relay setting need sensitivity and grow in small steps.

5. Each protective relay has its own safety precautions and must be read carefully before performing any task.

6. Most protective relays have excessive weight in kilograms and must be careful when carry.

7. The relay must be checked by visual inspection before any operation.

8. The history of the relay checking must be known before operation.

9. The primary or secondary test set that required to connect with the relay must be studded before use.

10. Any addition tools and requirements that needed during task operation must be known and read about.
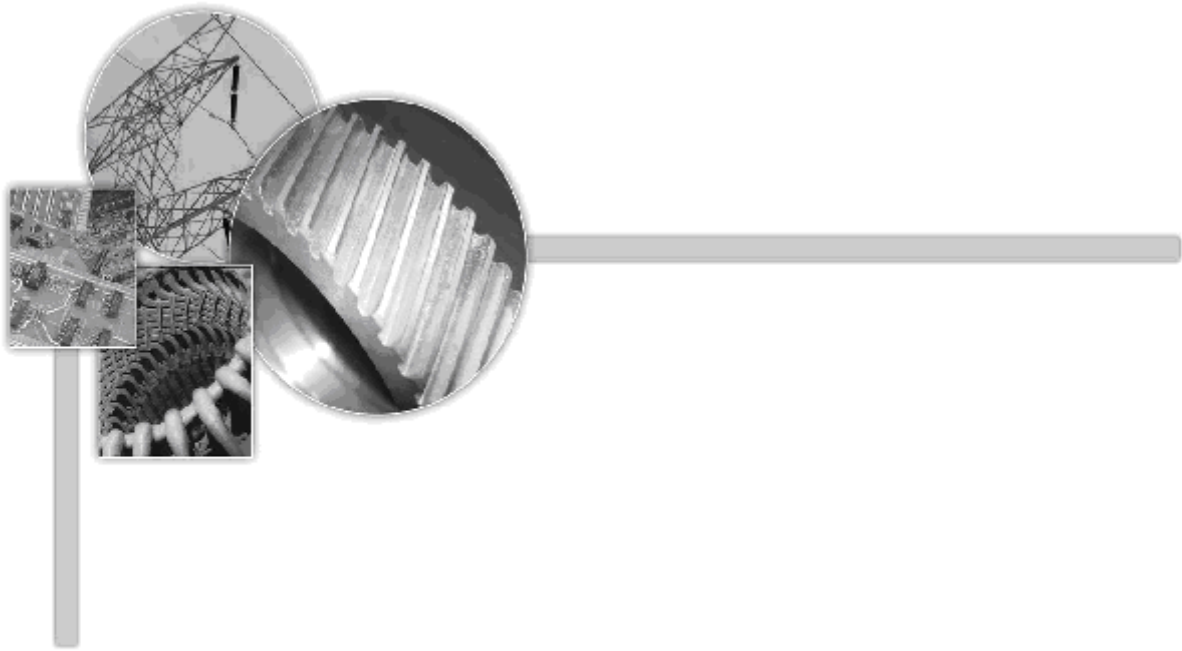
UNIT 1

TYPES OF ELECTROMECHANICAL PROTECTIVE RELAYS

UNIT 1

TYPES OF ELECTROMECHANICAL
PROTECTIVE RELAYS

OVERVIEW

In this unit, the trainees learn the principles and operation of electromechanical relays. It is classified as single input quantity or double input quantities. Some of them operate with plunger, clapper, and induction disc or induction cylinder. This unit discusses some types of protection such as time overcurrent, over/under voltage, directional and frequency protection.
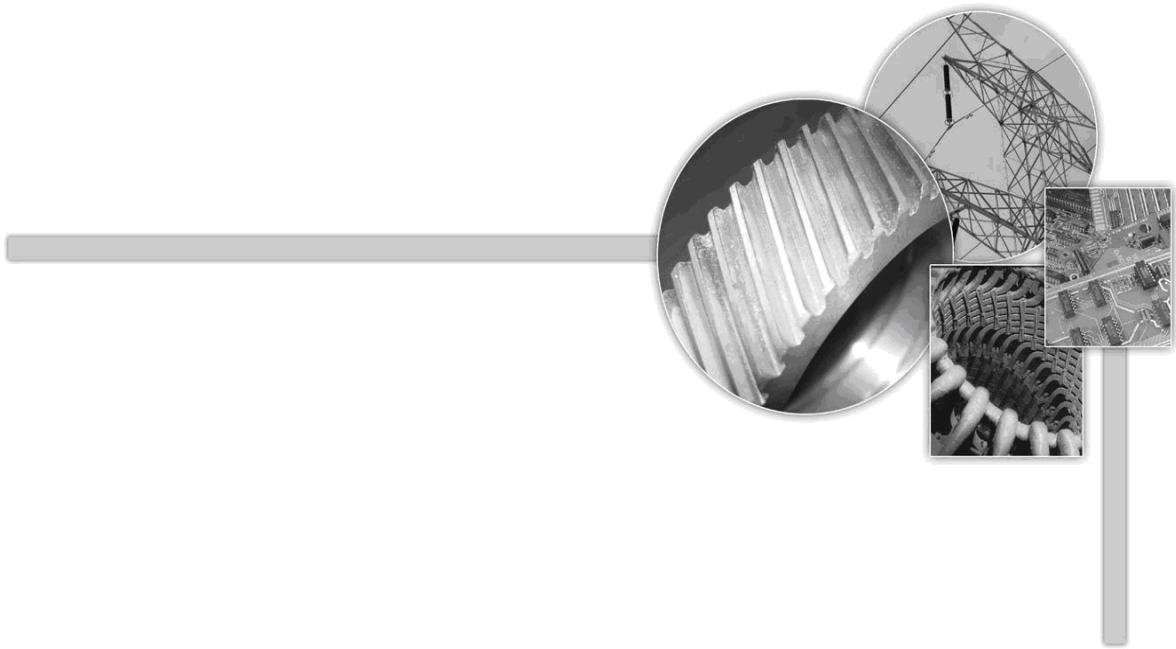
OBJECTIVES

Upon completion of this unit, the trainees will be able to:

- Identify the principles of plunger and clapper type relays.

- Demonstrate the induction disc relay and its applications.

- Verify the construction of induction cylinder relay and its applications.

- Demonstrate basic protective relays such as time overcurrent, over/under voltage, directional, and frequency relays.

LESSON 1.1

PLUNGER AND CLAPPER TYPE RELAYS

LESSON 1.1

PLUNGER AND CLAPPER TYPE RELAYS

OVERVIEW

This lesson covers the operation of plunger and clapper type relays identifying the parts in each type of relay. It discusses the pick-up and drop-out of the relays.

OBJECTIVES

Upon completion of this lesson, the trainees should be able to:

- Demonstrate the parts and operation of plunger type relay.

- Demonstrate the parts and operation of clapper type relay.

- Identify the pick-up and drop-out values of plunger and clapper relays.

- Adjust and calibrate plunger and clapper relay setting.

Task 1.1-1: Plunger relay type SV.

Task 1.1-2: Clapper relay type SG.

INTRODUCTION

Protective relays represent an important part in the protection system, it works as a comparison process, that it compares two mechanical quantities. One of them is the damping spring force; already exist most of the time. The electrical signal is converted to electromagnetic force, which represents the actual current or voltage of the system. When the damping force is greater than the actual force, it means normal operation and no fault occurs. When the damping force is less than the actual force, it means abnormal operation, (fault occurs), resulting in relay operation, producing trip signal. This rule is reversed in some applications such as under voltage relay.

PLUNGER TYPE RELAYS (SOLENOID TYPE)

The plunger type relay is a magnetic-attraction relay, which has a bar, or cylinder armature that is attracted axially into a solenoid coil. The coil is cylindrical with an external magnetic structure and center plunger, as shown in Fig. 1.1-1.
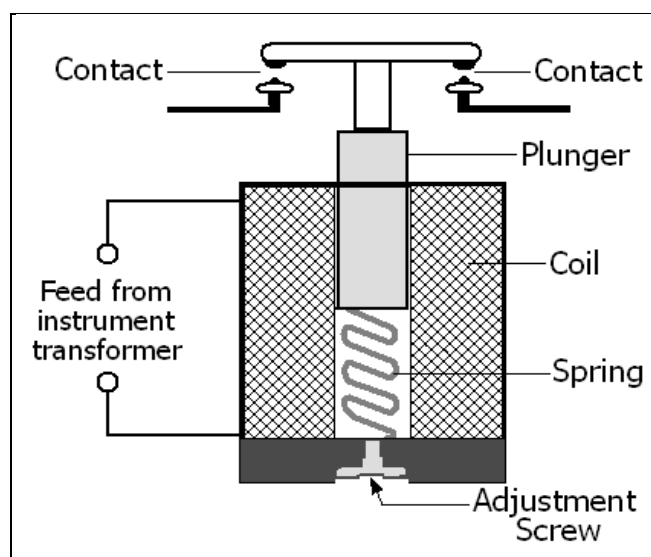
Fig. 1.1-1 Plunger Type Relay

The armature operates a moving contact up and down, facing a fixed contact. The principle of electromagnetic attraction can be used equally well on either AC or DC. When the current or voltage applied to the coil exceeds the pickup value, the plunger

moves down to operate a set of contacts. The required electromagnetic force **(F)** to move the plunger is proportional to the square of the current in the coil. The plunger unit's operating characteristics are largely determined by the plunger shape, the internal core, magnetic structure, coil design, and magnetic shunts.

When the magnetic field, produced by current flowing in the coil, is sufficiently strong, the armature or plunger moves and causes the relay action. This, in turn, completes the circuit to the trip-coil of the circuit breaker. Normally, the operation of this relay is instantaneous (no intentional time delay).
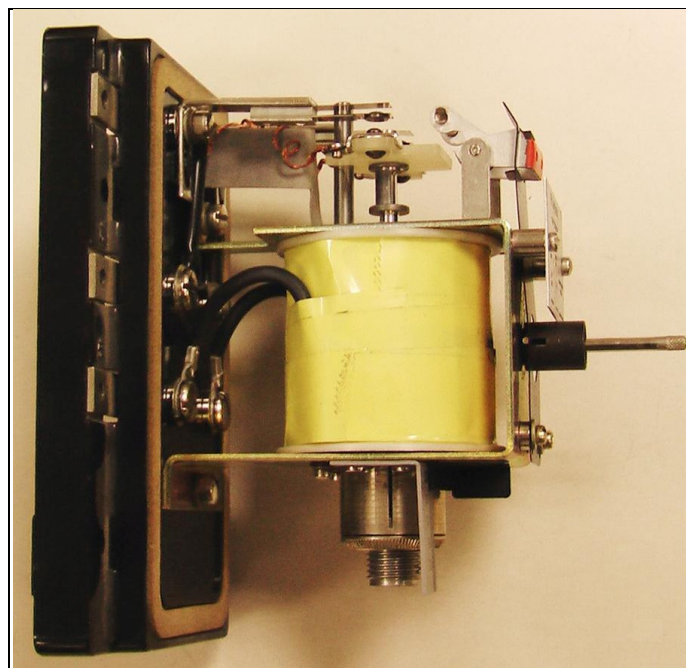
Fig. 1.1-2 Plunger Voltage Relay

Some types of plunger relays are used as a high drop-out instantaneous overcurrent unit. The relay coil has thick wire material with a few number of turns, and very small coil resistance (typically 0.1 to 0.5 Ω range). A helical spring absorbs the AC plunger vibrations, producing good contact action. The air gap provides a ratio of drop-out to pickup of 90 percent or greater over a two-to-one pickup range. The pickup range can be varied from a two-to one to a four-to-one range by adjusting core screw. When the pickup range is increased to four-to-one, the drop-out ratio will decrease to approximately 45 percent.

Other types of plunger relay are used as an instantaneous over or under voltage unit. The relay coil has fine wire with a large number of turns, and very high coil resistance (typically 2kΩ to 100kΩ range). An adjustable flux shunt permits settings that are more precise over the nominal four-to-one pickup range. This unit is relatively independent of frequency, operating on DC to 60 Hz nominal frequency. It is available in high and low drop-out versions. Over voltage relay has normally open contacts and used as a monitor to the voltage to indicate if it exists or not. Under voltage relays has normally close contacts.

OPERATING CHARACTERISTICS

Some types of plunger relays divide the coil into parts to give different setting for operation, by means of tap block, as shown in Fig. 1.1-3. Each tap block terminal has a different operating characteristic curve.
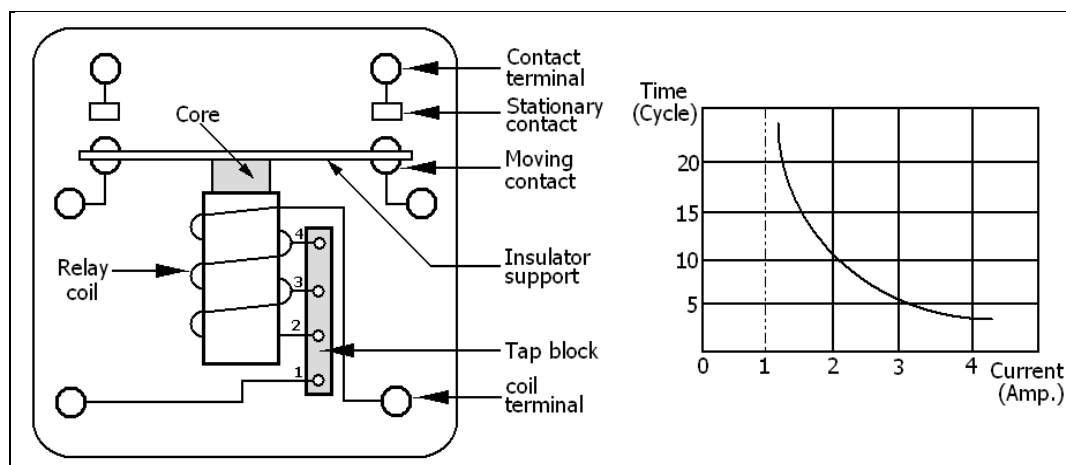
Fig. 1.1-3 Operating Characteristics of Plunger Type Relay

EXAMPLE

Voltage relay type SV and current relay type SC (Westinghouse made); Fig. 1.1-4 and 1.1-5 respectively are suitable for any application where an instantaneous plunger relay of high accuracy is required. These relays are utilized for protective and for auxiliary services where some of their features are desired.
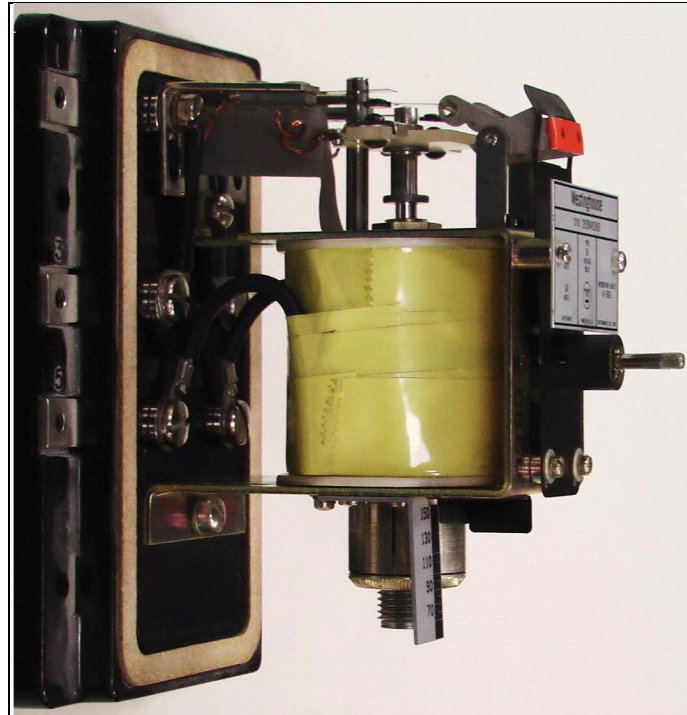
Fig. 1.1-4 SV Voltage Relay (Westinghouse)

SC (current relay) and SV (voltage relay) are adjustable over a wide range of current or voltage. Each relay is provided with a mechanical operation indicator and a calibrated scale to indicate the pick-up setting.

The high drop-out to pick-ratio (90 - 98%) of the Type SC and SV relays make them particularly suitable for use as fault detectors to supervise main protective relays. A typical application involves an SV voltage operated relay in a generator back-up protection scheme. The SV relays are used to supervise an overcurrent unit when the overcurrent unit is to operate on less than full load current if the voltage drops below a predetermined level.

Fig. 1.1-5 shows construction of SC plunger type relay.

1	Two independent reversible stationary contact
2	Moving contact arm with two contacts
3	Operation indicator
4	Plunger
5	Name plate
6	Target reset
7	Coil
8	Adjustable magnetic shunt
9	Calibrated scale
10	Core screw
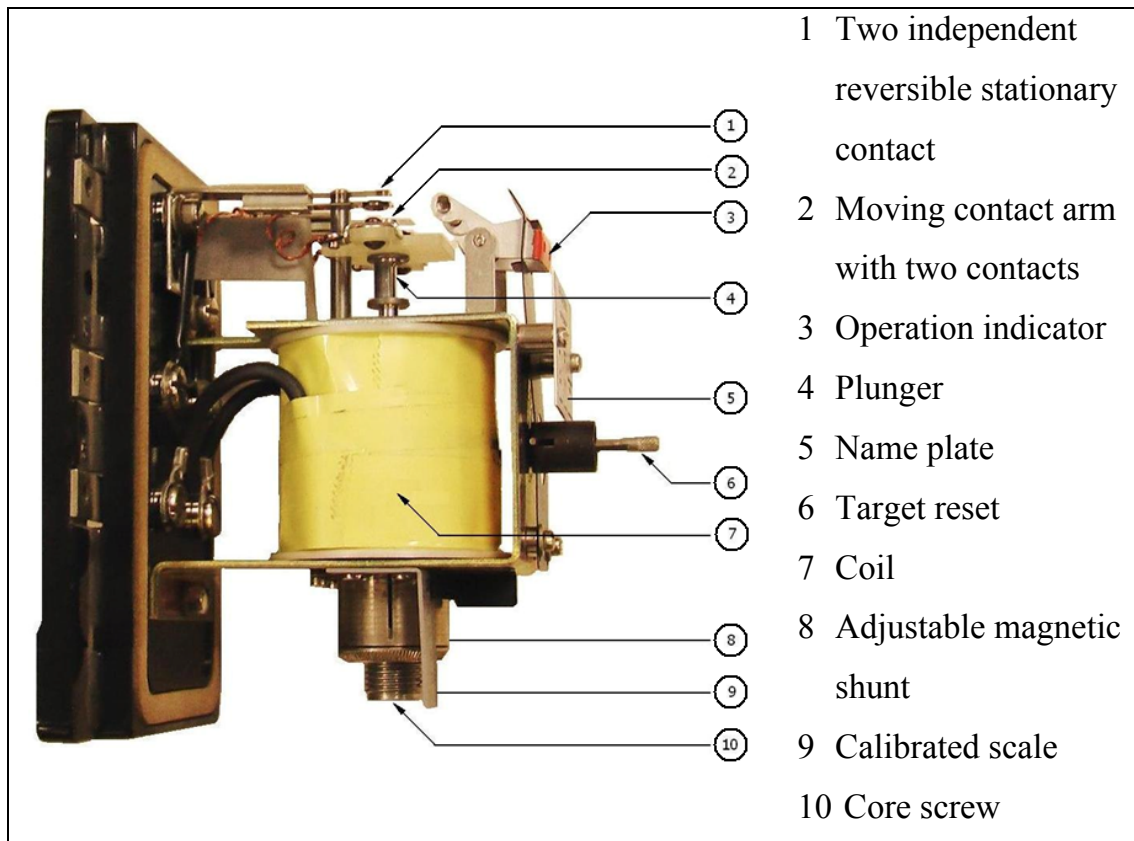
Fig. 1.1-5 Construction of Plunger Type Relay

Clapper Type Relays

The clapper type or hinged-armature type of relay is a magnetic attraction relay. The core of the solenoid coil is stationary and the hinged movable armature is attracted to the face of the core. The armature operates moving contacts facing fixed contacts. The contacts may be arranged to make or break when the armature pulls in or drops out, respectively.

The clapper units have a U-shaped magnetic frame. The armature is hinged at one side and spring-restrained at the other. When the associated electrical coil is energized, the armature moves towards the magnetic core, opening or closing a set of contacts with a torque proportional to the square of the coil current. The pickup and drop-out values of clapper units are less accurate than those of plunger units. Clapper units are primarily applied as auxiliary or go/no-go units.
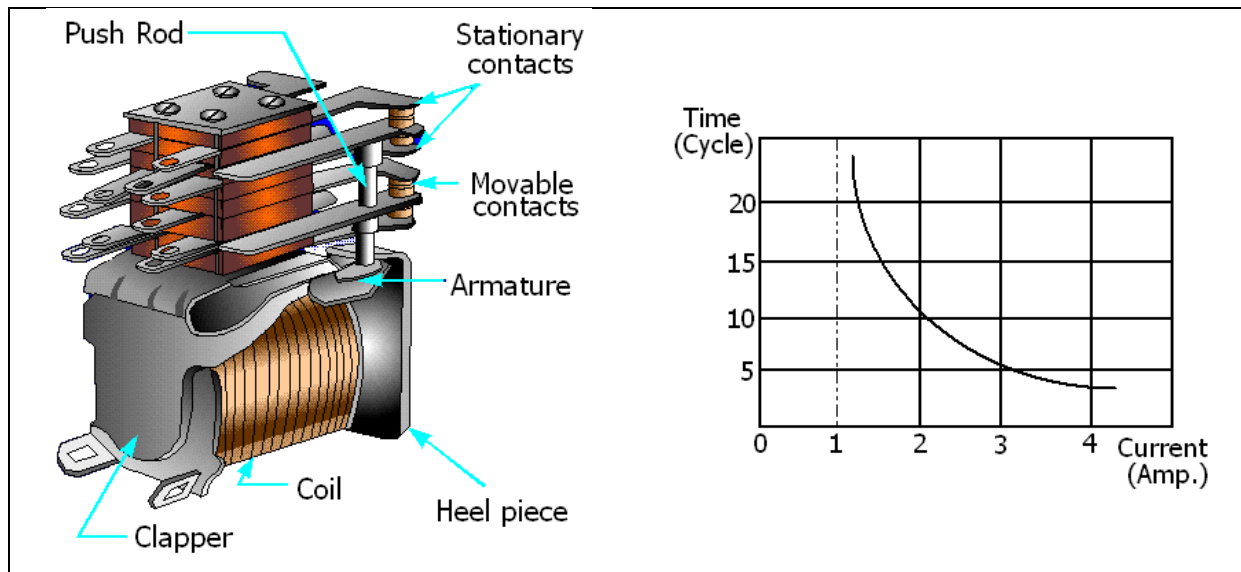
Fig. 1.1-6 Clapper Type Relay and its Operating Characteristics

EXAMPLE

SG clapper type relay shown in Fig. 1.1-7 is used as auxiliary relay for miscellaneous automatic and remote control switching.
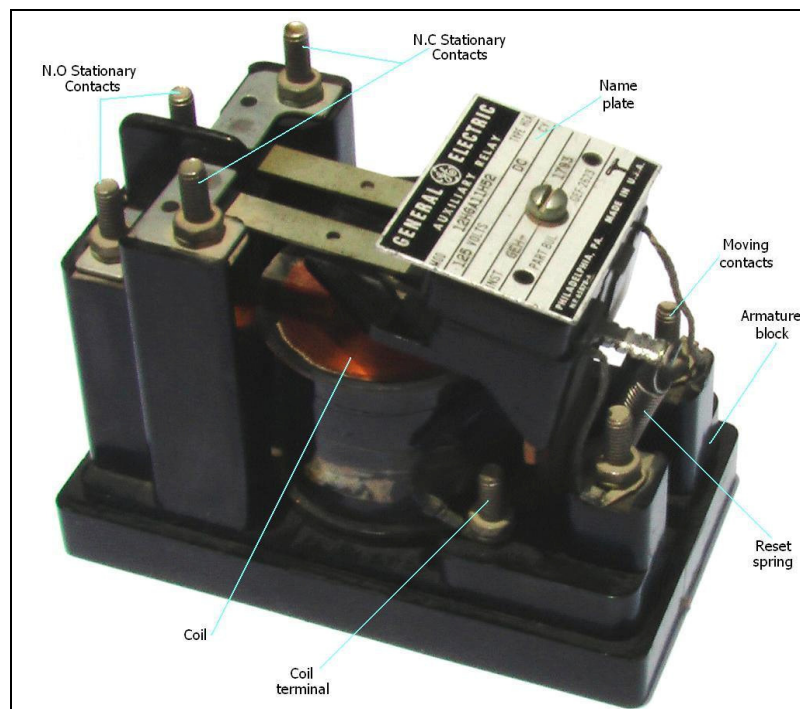
Fig. 1.1-7 SG Clapper Type Relay

The SG relays, are clapper-type devices designed to operate over a wide range of AC and DC voltages. When their coils are energized at or above pickup rating, the moving contacts on the armature block close or open with the two stationary contacts to complete the electrically independent circuits.

Closed types are supplied with two make and two break contacts. Open types (front connected) can be supplied with two make and two break contacts or with only the two make contacts, which can be reversed to provide one make, one break or two break contact circuits.

Small coil springs on the moving contact arms provide adequate contact pressure to assure positive contact action between the moving and stationary contacts. DC types have a bronze pin on the core, which serves as a stop pin for the armature and prevents magnetic seal-in of the armature due to residual magnetism. AC types have a non-magnetic washer at the base of the core assembly to prevent the armature from sticking in the close-gap position. Copper shading rings are also provided on the core face of the AC types to prevent chattering of the armature.

RELAY CONTACTS

Both of moving and stationary contacts are made of silver. Each closing and carry about 12 Amperes continuously or carry 30 Amperes for short time.

A modified version of the clapper relay is the so-called, telephone relay because of its wide application in the telephone service. It is used where contact currents are very small.
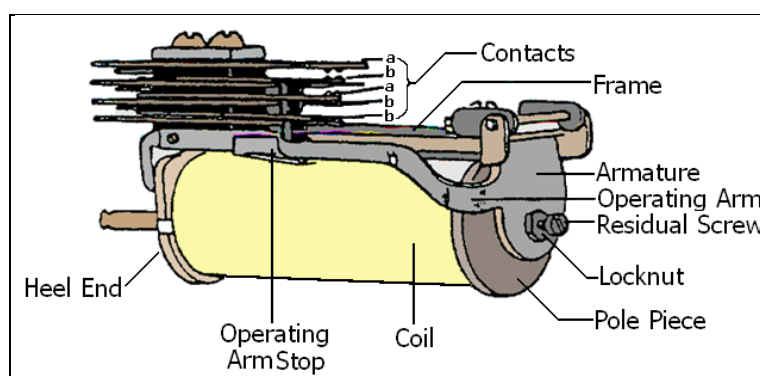
Fig. 1.1-8 Telephone Relay

SUMMARY

- Plunger relay compares spring force with electromagnetic force.

- In over voltage or overcurrent, at normal operation, spring force is higher than electromagnetic force, whereas in the case of abnormal operation; spring force is less than electromagnetic force.

- Plunger relay works as voltage relay to monitor the system voltage if it exists or not.

- Plunger relay can operate by AC or DC depending on design.

- Some types of plunger relays work by AC with internal rectifier.

- Plunger type voltage-relay always has fine wire coil with a large number of turns.

- Plunger type current-relay always has thick wire coil with little number of turns.

GLOSSARY

Plunger: Movable iron core inside hollow coil

Spring: Flexible strip metal coil

Stationary contact: Fixed contact

SPST contact: Single Pole Single Through contact

SPDT contact: Single pole double through contact

DPDT contact: Double Pole Double Through contact

Adjustment screw: A way to control the spring force

Clapper relay: Type of auxiliary relays

REVIEW EXERCISE

Circle the letter a, b, c or d that correctly completes the statement and follow the directions to answer the other questions:

1. Plunger type relay is ……………………………………………………….

   a) Time delay unit.   b) Instantaneous unit.

   c) Both (a) and (b).   d) None of above.

2. The type of relay shown in Fig. 1.1-9 is …………………………………….

   a) Plunger type.

   b) Clapper type.

   c) Induction disc type.

   d) None of the above.

   Fig. 1.1-9
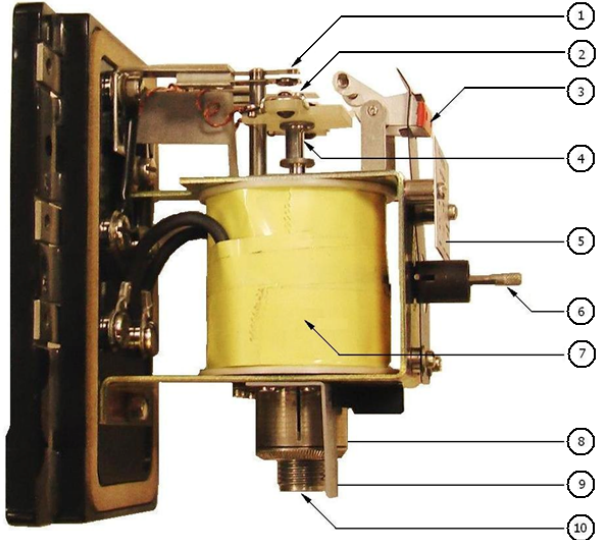
3. The target in the relay provides ………………………………………….

   a) Visual indication of operation.   b) Density of the current in the circuit.

   c) Polarity of the circuit.   d) All of above.

4. Clapper type relays are used extensively in ……………………….

   a) Electronic amplifiers.   b) Telephone services.

   c) Electronic protective relays.   d) All of above.

5. Clapper type relays are designed for …………………. operation.

   a) AC only.   b) DC only.

c) Both (a) and (b).   d) None of above.

6. Match the components listed below with the number on the plunger type relay.
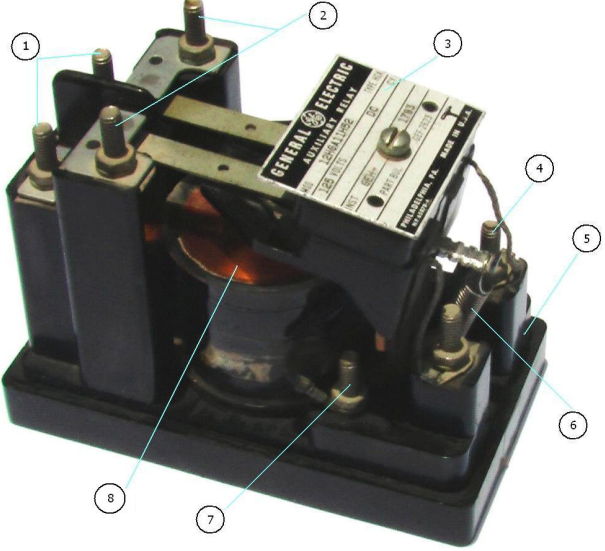
DESCRIPTION	ANS.	
Plunger		
Coil		
Adjustable magnetic shunt		
Core screw		
Stationary contacts		
Moving contacts		
Operation indicator		
Target reset		
Name plate		
Calibrated scale		

7. Match the components listed below with the number on the clapper type relay.

DESCRIPTION	ANS.	
Coil		
NC Stationary contacts		
Name plate		
Reset spring		
Moving contacts		
Armature block		
Coil terminals		
NO Stationary contacts		

TASK 1.1-1

PLUNGER RELAY TYPE SV

OBJECTIVES

Upon completion of this task, the participants will be able to:

- Demonstrate the parts of plunger type SV relay.

- Check pick-up and drop-out values.

- Determine reset factor or drop-out ratio.

TOOLS, EQUIPMENT & MATERIALS

- Plunger voltage relay (Westinghouse type SV), shown in Fig. 1-1.
- Relays tool kit
- Secondary injection test set as a voltage source
- Relay instruction manual
- AC Voltmeter
- Personal safety equipment as recommended in relay workshop.

PROCEDURE

OBJECTIVE 1: DEMONSTRATION PLUNGER RELAY

1. Identify the stationary contacts.
2. Identify operating indicator.
3. Identify target latch.
4. Identify relay coil and calibrated scale
5. Identify adjustable magnetic shunt and core screw.
6. Identify and read the relay nameplate.
7. Determine the required information from the relay nameplate.
8. Compare the nameplate information and relay manual data.

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1   Two reversible stationary contact

2   Moving contact arm with two contacts

3   Operation indicator

4   Plunger

5   Name plate

6   Target reset

7   Coil

8   Adjustable magnetic shunt

9   Calibrated scale

10 Core screw

Fig. 1-1 Plunger Type Relay

OBJECTIVE 2: CHECKING THE RELAY PICK-UP

9. Set the adjustable magnetic shunt to the relay operating voltage.

10. Connect the voltmeter to the relay coil.

11. Slowly raise the tester voltage from zero until the relay contact closes.

12. Record the voltmeter reading pick-up value, $V_{PICK-UP}$ = ………………………..

OBJECTIVE 3: CHECKING THE RELAY DROP-OUT

13. Slowly decrease the tester voltage until the relay contact releases.

14. Record the voltmeter reading drop-out value, $V_{DROP-OUT}$ = ……………………

OBJECTIVE 4: DETERMINING RESET FACTOR (DROP-OUT RATIO)

15. Calculate reset factor or Drop Out Ratio for the plunger relay

   % Drop Out Ratio = ($V_{DROP-OUT}$ / $V_{PICK-UP}$) x 100 = ...

16. A good % drop out ratio, which is more than 90%

17. Return the voltage source to zero and shut down the relay tool kit.

TASK 1.1-2

CLAPPER RELAY TYPE SG

OBJECTIVES

Upon completion of this task, the participants will be able to:

- Demonstrate the parts of clapper type relay.

- Check pick-up and drop-out values.

- Check reset factor or drop-out ratio.

TOOLS, EQUIPMENT & MATERIALS

- Clapper auxiliary relay (Westinghouse type SG), shown in Fig. 2-1.
- Relays tool kit
- DC variable supply
- DC voltmeter
- Personal safety equipment as recommended in relay workshop.

PROCEDURE

OBJECTIVE 1: DEMONSTRATION THE CLAPPER RELAY

1. Identify the coil and coil terminals of the relay.
2. Identify the terminals to contact connections.
3. Identify stationary contacts.
4. Identify moving contact.
5. Identify contact wipe armature spring.
6. Identify armature block.
7. Identify armature reset spring.
8. Identify and read the relay nameplate.
9. Determine the required information from the relay nameplate.
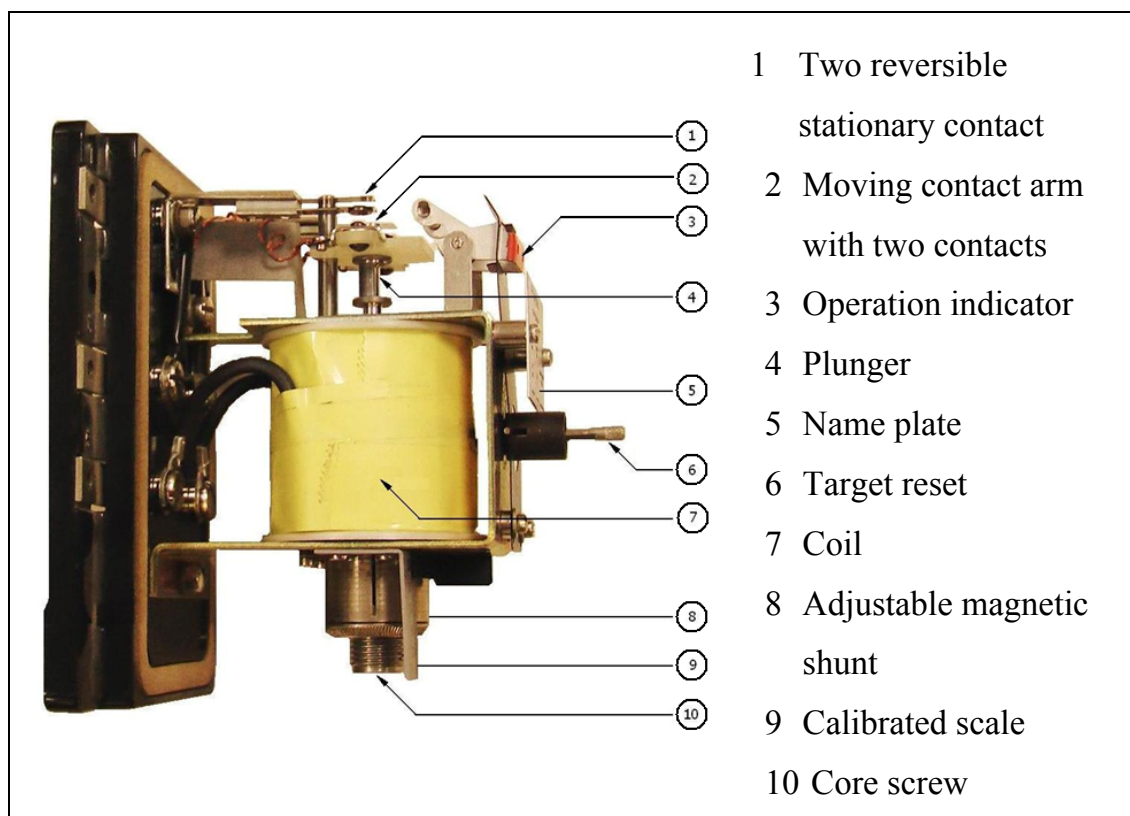10. Compare the nameplate information and relay manual data.
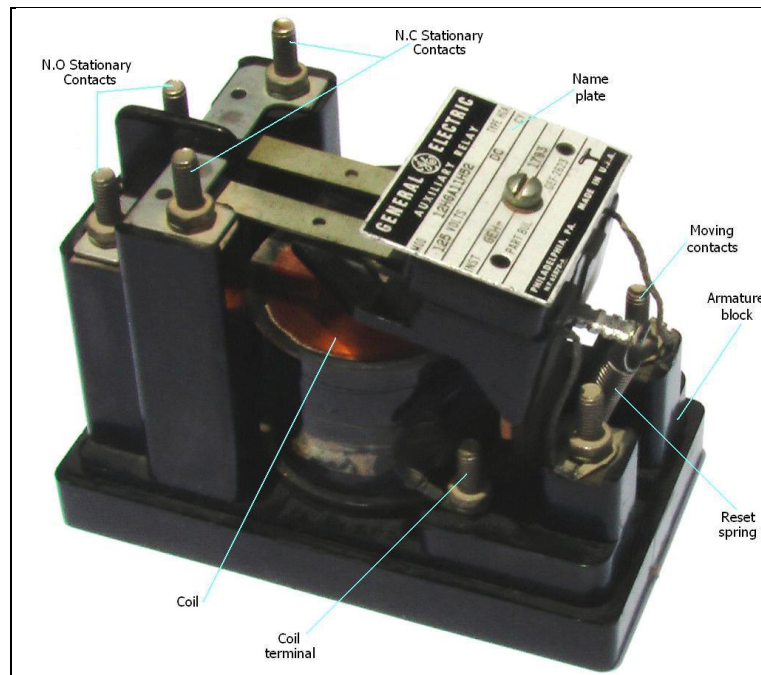
Fig. 2-1 Clapper Type Relay

OBJECTIVE 2: CHECKING THE RELAY PICK-UP

11. Connect the relay to the test set, and adjust the supply to zero voltage DC to the relay terminals and note contacts movement in step 12.

12. Gradually increase the supply until the contact closes.

13. Record the voltmeter reading (pick-up voltage).

OBJECTIVE 3: CHECKING THE RELAY DROP-OUT

14. Gradually, decrease the DC voltage until the contact opens.

15. Record the voltmeter reading (drop-out voltage).

OBJECTIVE 4: DETERMINING RESET FACTOR (DROP-OUT RATIO)

16. Calculate reset factor or Drop-Out Ratio for the clapper relay.

% Drop Out Ratio = $(V_{DROP-OUT} / V_{PICK-UP})$ x 100 = ...

17. A good drop out ratio, which is more than 90%

18. Return the voltage source to zero and shut down the test set.
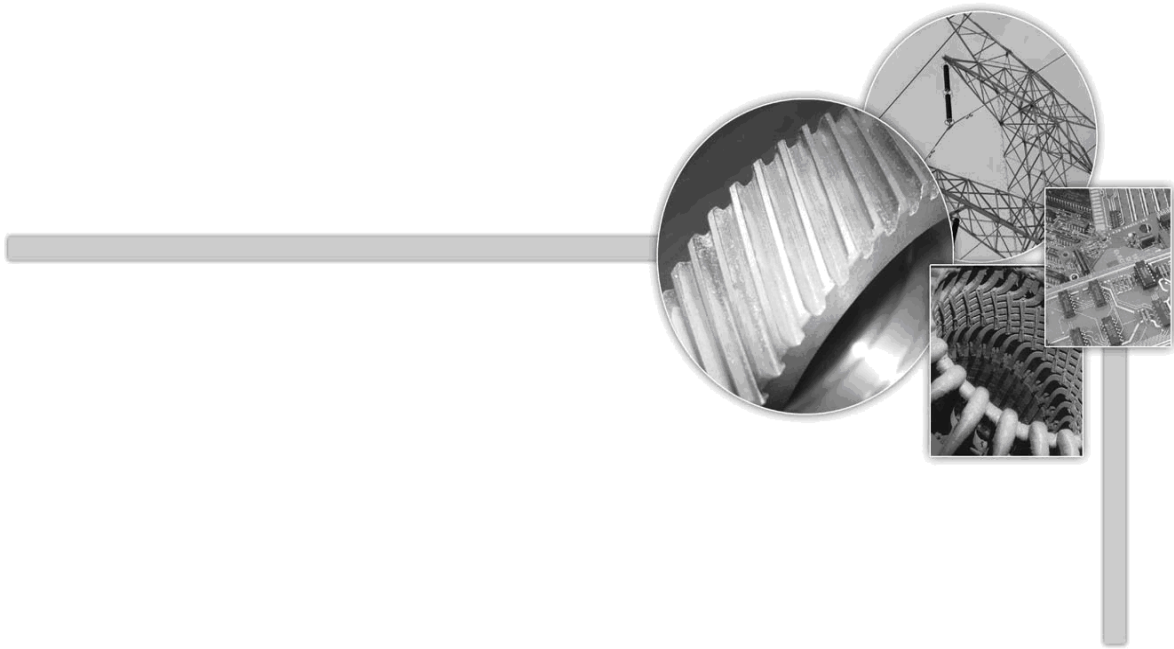
LESSON 1.2

INDUCTION DISC & TIME-OVERCURRENT RELAYS

LESSON 1.2

INDUCTION DISC & TIME-OVERCURRENT RELAYS

OVERVIEW

This lesson describes the construction and operation of induction disc unit and its applications in directional and overcurrent protection. The lesson discusses the current and time setting for the inverse time overcurrent relay.

OBJECTIVES

Upon completion of this lesson, the trainees will be able to:

- Identify the construction of induction disc relay.
- Demonstrate the operating characteristics of single and double input quantities induction disc units.
- Verify application of induction disc unit in overcurrent protection.
- Perform the calibration of current and time settings for IFC type relay.

Task 1.2-1: Demonstration for induction disc relay.

Task 1.2-2: Checking for inverse time overcurrent relay.

INTRODUCTION

The electromagnetic induction disc relay is frequently used where the time of relay operation should depend upon the amount of an overcurrent. The relay is essentially a small induction motor or watt-hour meter. It starts to turn when the current exceeds a previously selected threshold value, and rotates faster as the current increases. This relay has one set of stationary contacts and one set moves as the disc turns. The distance, which the disc must travel to close the contacts is adjusted by setting the position of the time dial control. The magnitude of current, which initiates disc movement, is set by choosing the tap on the current coil. The resulting operation of the relay contact operation is dependent upon the tap and the time dial settings. The relay timing can be varied from a few cycles to as long as 30 seconds. The actual speed-torque characteristic of the relay can be controlled by the designer to give a wide variety of operating characteristics.

THEORY AND OPERATION

An aluminum disc rotates between the pole faces of an electromagnet, which produces the sweeping flux necessary to cause rotation of the disc.
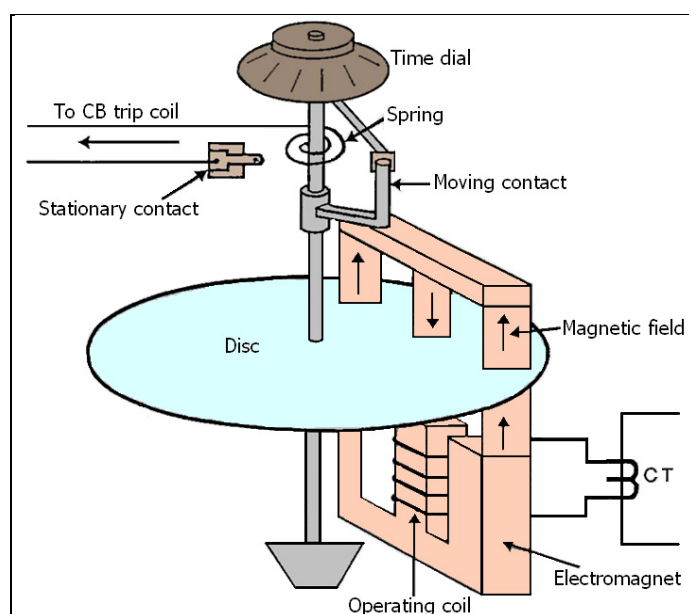
Fig. 1.2-1 Typical Electro-mechanical Time Overcurrent Relay

The relay operates by torque derived from the interaction of fluxes produced by an electromagnet with that from induced current in the plane of a rotating Aluminum disc. The operating coil in Fig. 1.2-1 has three poles on one side of the disc and a common magnetic member or keeper on the opposite side. The main coil is on the center leg. Current (I) in the main coil produces flux φ, which passes through the air gap and disc to the keeper. A small portion of the flux is shunted off through the side air gap. The flux, Φ divides as Φ_L through the left-hand leg and as Φ_R through the right-hand leg, where $\Phi = \Phi_L + \Phi_R$.

In Fig. 1.2-2, the right pass of flux causes Φ_R to lag both Φ_L and Φ, producing a torque action between the two fluxes, and this action leads to rotate the disc. Electromagnet is constructed to make it sensitive to current or voltage. A current-sensitive electromagnet is wound with a few turns of heavy copper wire. The voltage-sensitive electromagnet is wound with many turns of fine copper wire. This induction coil is connected to the secondary of a current transformer for current sensing or to the secondary of a potential transformer for voltage sensing. The amount of current or voltage that the induction coil sees is proportional to the primary system values. Electromagnet induces flux into the disc to cause rotation of the disc and closing for the relay contacts.
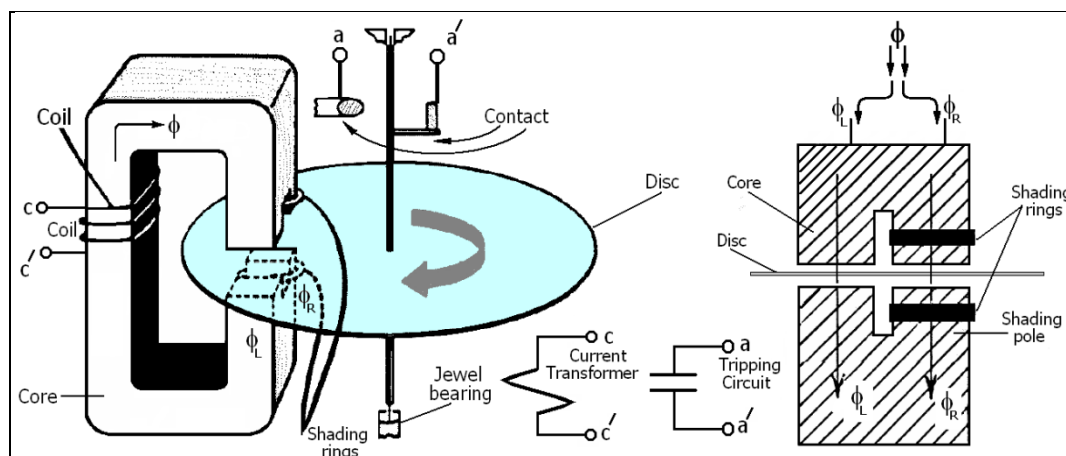
Fig. 1.2-2 Induction Disc Type Relay

Operating range of electromagnet is adjusted by selecting a tap value on the tap block of operating coil. The relay contacts material is made of silver.

The disc must be electrically conductive to allow it to carry small induced eddy currents within it and be non-magnetic so that it will not be attracted to the electromagnet. The spiral spring mounted to the shaft ensures a uniform pickup throughout the full range of disc travel. The aluminum disc is mounted on a vertical insulated shaft that rides on a lower jeweled bearing and a stainless steel pin on top. Their construction is designed to provide the least amount of friction possible.

As the disc rotates, the spring increases its tension and a larger current is required to keep the disc in motion at the same speed. To compensate for this effect, a series of holes graduated in size and spacing, are provided in the disc. So that a constant operating current will produce a constant disc speed through the entire disc travel.

DRAG (DAMPING) MAGNET

Drifting occurs when the disc begins to rotate and the actuating value drops below the pickup value of the relay disc but continues to turn or drift because of inertia. This condition may cause false tripping.

Fig. 1.2-3 Induction Disc Relay

The damping magnet is a permanent magnet that provides negative torque on the disc. This negative torque slows the disc down to a steady speed and prevents the disc from drifting. Thus, based on the current that is fed from the CT to the relay, the disc speed

will be proportional to the system current. The relay will now operate with torque proportional to the load conditions of the circuit it is protecting.

SPIRAL SPRING

Once the disc closes the contacts, it must be reset by hand, unless a spiral or reset spring is added, as shown in Fig. 1.2-3. The spiral spring has three functions. The first is to reset the disc once the abnormal condition has stopped or the circuit is tripped. Another function is to provide the initial negative torque on the disc and to allow an adjustment of minimum pickup. The last function is to provide a temporary path for the DC tripping current from the external circuit to the moving contact. The spiral spring is not designed to carry the tripping current for very long; thus, a seal-in, bypass function is required.
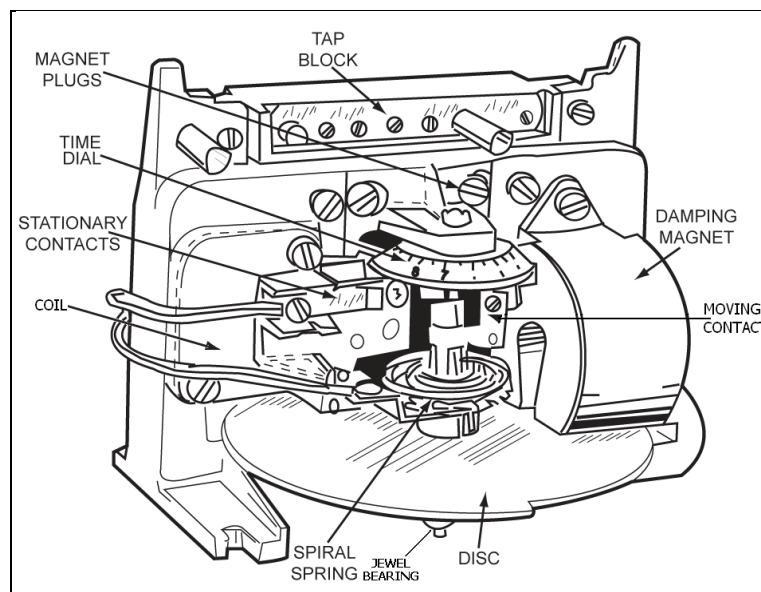

Fig. 1.2-4 Parts of Induction Disc Relay

TIME DIAL

Fig. 1.2-4 shows parts of induction disc relay. Some method of providing time adjustment is required. The time dial provides this adjustment by changing the distance between the moving and stationary contacts, as shown in Fig. 1.2-4.

The greater the distance the disc must travel the greater the time it will take for the contacts to close. The time dial employs a stop, which the contact rests upon. Turning the time dial to a higher number opens the contact distance. Time dial changes do not affect the shape of the time-current characteristic curve.

INDUCTION DISC UNIT APPLICATIONS

There are two types of induction disc unit applications:

1-   Single input quantity.

2-   Double input quantities.

SINGLE INPUT QUANTITY

Single input quantity applies to overcurrent, and over/under voltage protective relays.

DOUBLE INPUT QUANTITIES

Double input quantities apply to directional unit protective relay.

INDUCTION DISC DIRECTIONAL UNIT

Induction disc directional unit is an example for double input quantities relay. The rotation of the disc occurs due to interaction between fluxes of current and voltage coils. The angle between V & I is very important factor to produce maximum torque during fault. The connection of the directional relay unit is shown in Fig. 1.2-5.
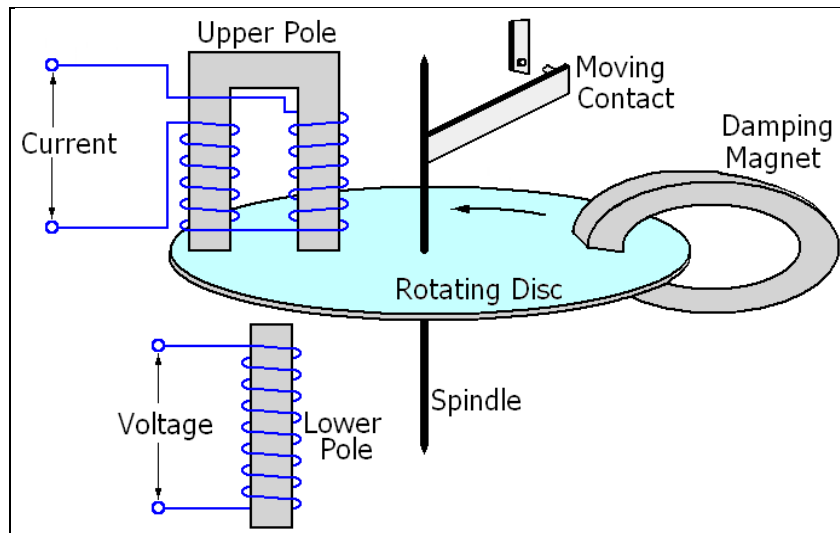
Fig. 1.2-5 Induction Disc Directional Unit
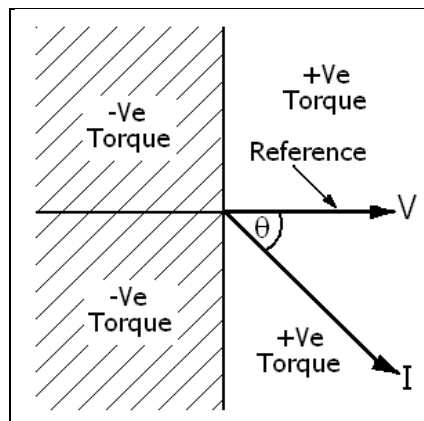
Fig. 1.2-6 Vector Diagram of V and I

In normal operation, a positive torque produces disc rotation clockwise away from the stationary contact. At abnormal condition, the current is reversed producing a negative torque that rotates the disc counter-clockwise towards the stationary contact. The voltage is used as a reference to the current. The torque equation is expressed as follow:

T = K V I cos θ

Where: θ is the angle between V & I

V: is the reference voltage from voltage transformer.

I: is the relay current from current transformer.

K: is a constant.

Contacts close for I in un-shaded region and open in shaded region. There is a target and seal-in unit mounted on the front of the unit with its coil in series and contacts in parallel with the contacts of the time Over-Current unit, such that when the induction unit contacts close, the seal-in unit picks up and seals in. When the seal-in unit picks up, it raises a target into view, which latches up and remains exposed until released by pressing a button.

INDUCTION DISC INVERSE TIME O/C UNIT

Induction disk Time Over-Current element is an example for the single input quantity. AC Current is supplied to the relay coil and by inductive coupling to the upper pole as shown in Fig. 1.2-7.

Fig. 1.2-7 Induction Disc Inverse Time O/C Unit

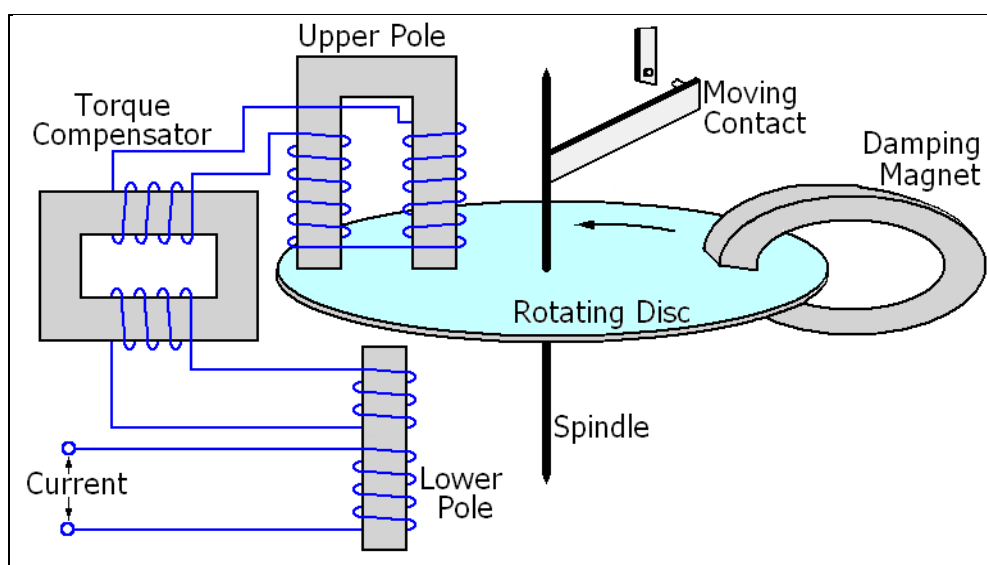The upper pole induces currents in the disk. Torque is produced by the reaction between two induced fluxes in the disc. Adjustment to current setting is done by coil tap selected and time setting is by contact travel.

In Fig. 1.2-7, the relay is adjusted for minimum times down to (0.05-0.1) sec. The relay characteristic is selected according to the desired application.

There are four different time characteristic curves, as shown in Fig. 1.2-8, that the relay unit can be set for one of the following characteristics:

1- . Inverse. 2- Very inverse.

3- Extremely inverse 4- Instantaneous.

- **Inverse type relays** are likely to provide faster overall protection in applications where the available fault current magnitudes vary considerably. Inverse characteristic is used for highly inductive loads such as large motors, where it takes long starting time for current to reaches steady state.

- **The very inverse** O/C relay is particularly suitable if there is a substantial reduction of fault current as the distance from the power source increases. It is particularly well suited for application where the fault current magnitude is dependent mainly upon the location of fault relative to the relay and only slightly upon the system generating set-up at the time of the fault or provide faster overall protection in applications where the available fault current magnitude remains fairly constant due to a relatively constant generating capacity. Very inverse characteristic is used for the loads subjected to transient operation or repeated switching.

- **Extremely inverse** characteristic is used when the time of travel is approximately inversely proportional to the square of the current. This makes it suitable for the protection of distribution feeder circuits in which the feeder is subjected to peak currents on switching in, as would be the case in a power circuit supplying induction motors, with high starting currents. The long time operating characteristic of extremely inverse relay at normal peak load makes this relay, particularly, suitable for grading the fuses. The extremely inverse time characteristics often permits successful pick up of inductive loads and at the same time provides adequate fault protection.

- **Instantaneous** characteristic is used for general purpose applications, which need fast trip when exposed to abnormal condition.
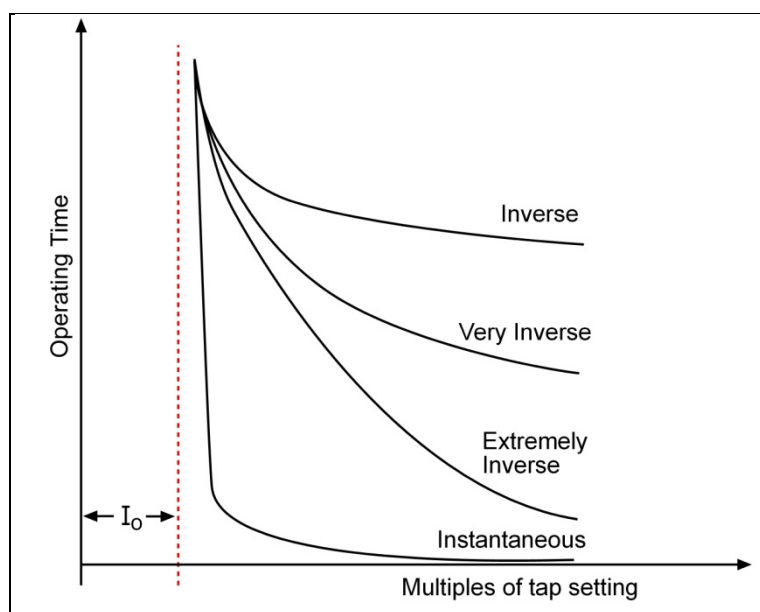
Fig. 1.2-8 Operates for I greater than I_O

The following table summarizes the applications for each characteristic.

Current-Time Characteristic	Main Application	Criterion	Response Time (s) with $I/I_p = 10$ and TM = 1
Inverse Time	Main or back-up protection for power lines with good step selection.	Unaffected by location; mainly controlled by transmitted power.	3.6
Very Inverse Time	As above, particularly for detecting earth faults	More affected by location	1.6
Extremely Inverse Time	Protection of incoming feeders	Fuse discrimination little affected by inrush currents	0.6

Table 1.2-1

NOMINAL CURRENT (I_O): It is the adjustable setting value, which makes no intersection with relay curves, as shown in Fig. 1.2-9.
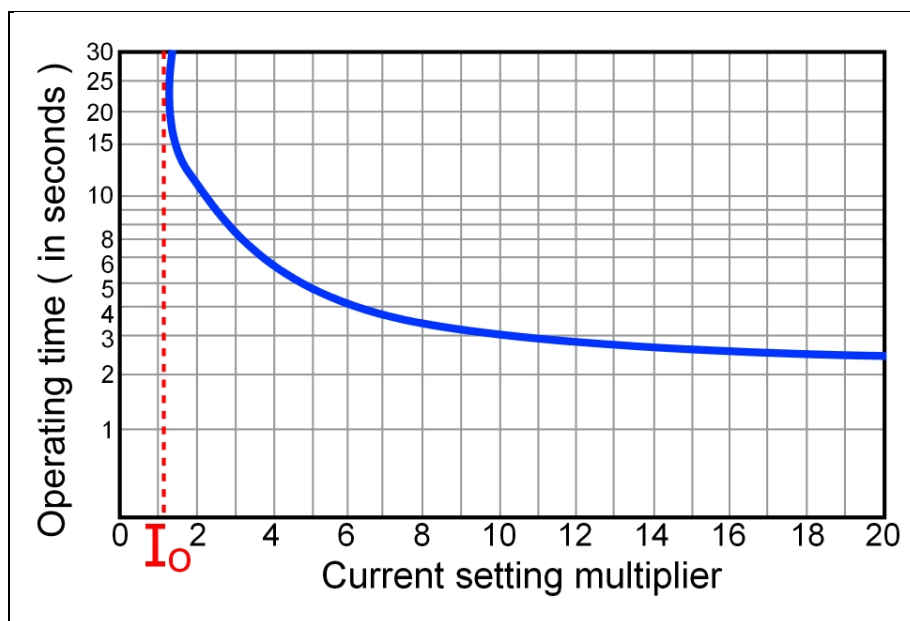
Fig. 1.2-9 Operating Characteristics of Time Overcurrent Relay

TIME OVERCURRENT RELAY

For the induction disc time overcurrent relay, when there is sufficient current passing through the operating coil, the disk starts to move towards the stationary contact. This is called the pick-up current. Taps are provided to allow adjustment of the pick-up or, tension of the spring can be adjusted. As the disk rotates, it carries with it the relay operating contact and this finally is brought up against the fixed contact, thus closing the tripping circuit.

Remember, the magnitude of current in the operating coil is proportional to the primary current passing through the CT; hence the greater the primary current, the faster the disk will rotate. Fig. 1.2-10 shows the well-known inverse time characteristic of the induction relay. The higher the level of fault current, the quicker is the operation of the relay. Moreover, for any particular current value, we can adjust the operating time by adjusting the time dial to increase the distance that the moving contact must travel. When reading these curves, remember that the value of current along the base is expressed relative to pick-up current.
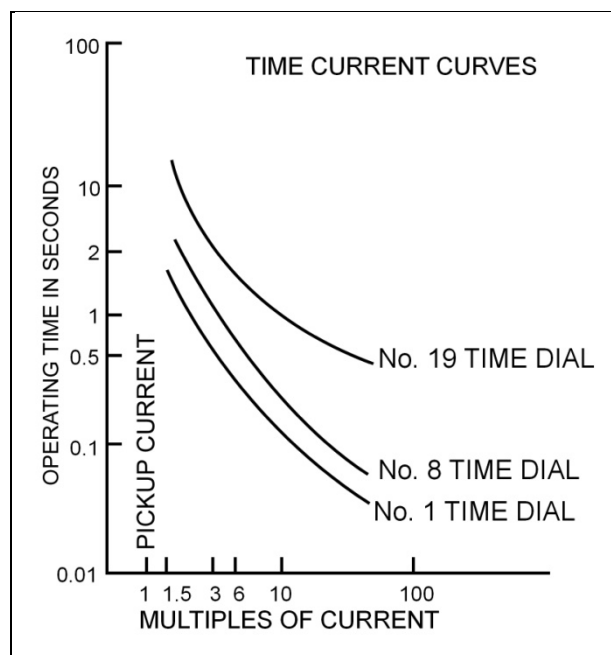
Fig. 1.2-10 Inverse Time Characteristic of Induction Relay

The main coil has a range of discrete current settings so that the sensitivity can be set for a particular situation. The relay coil is given a nominal rating, usually 5A, which is referred to as 100%.

a)   50% - 200% in seven steps for overcurrent relays (2.5 A – 10 A)

b)   20% - 80% in seven steps for earth fault relays (1A – 4 A)

The required plug setting is obtained by inserting a plug in the appropriate position in the plug bridge. To avoid open-circuiting the secondary of current transformer, the setting is automatically set to the highest value when no plug is inserted, as shown in Fig. 1.2-11.

Time multiplier setting (TMS), is given a value from 0.1 to 1.0. With a TMS of 1.0, the disc is set for maximum travel or time delay. The relay is a self resetting device and, therefore, is fitted with a flag to indicate operation. By using the ratio relay current to relay setting current one curve can be used for all plug settings. The ratio of relay current to relay setting current is called the Plug Setting Multiplier (PSM). And Relay Current = Primary Current/ CT ratio.
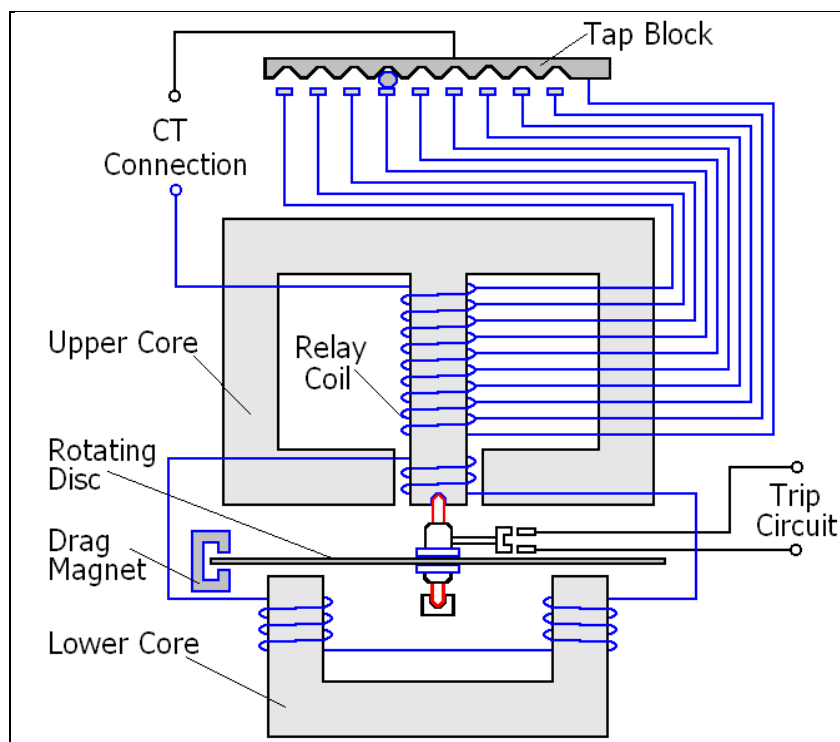
Fig. 1.2-11 Induction Relay Setting

OVERCURRENT PROTECTION APPLICATIONS

The Overcurrent protection has a wide range of applications as follows:

1. **Motor Protection:** Overcurrent protection is the basic type of protection used against overloads and short-circuits in stator windings of motors. Inverse time and instantaneous phase and ground overcurrent relays can be employed for small/medium size motors.

2. **Line Protection:** The lines (feeders) can be protected by:
    *   Instantaneous overcurrent relays
    *   Inverse time relays
    *   Directional overcurrent relays
    *   Distance relays

3. **Overcurrent Protection for 3-Phase Circuits**

    O/C protection with three O/C relays and three CTs, as shown in Fig. 1.2-12, is used for multiphase fault protection.

a) USING 3-CTs & 3-O/C RELAYS
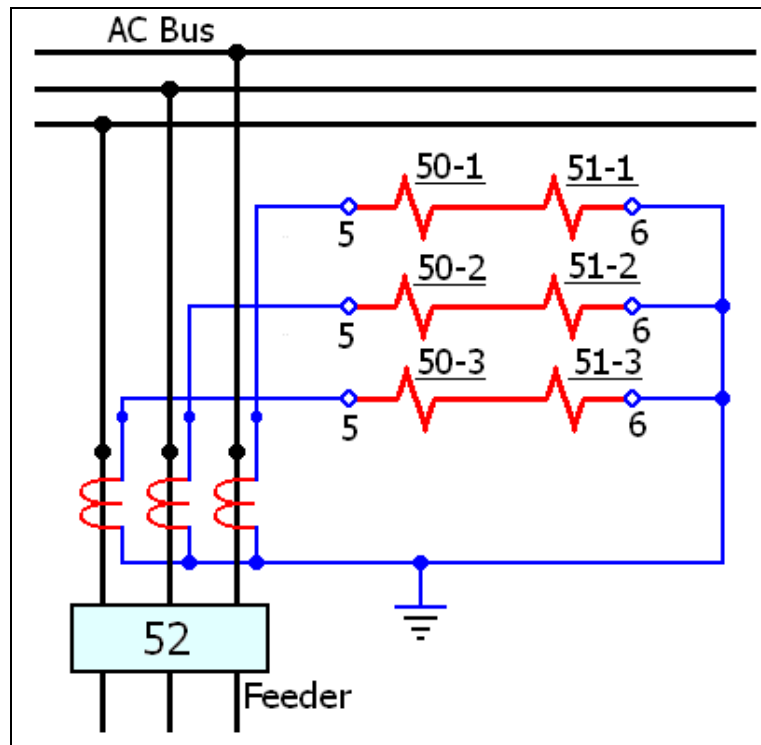
Fig. 1.2-12 O/C Protection with Three O/C Relays and Three CTs

b) USING 2-CTs & 2-O/C RELAYS
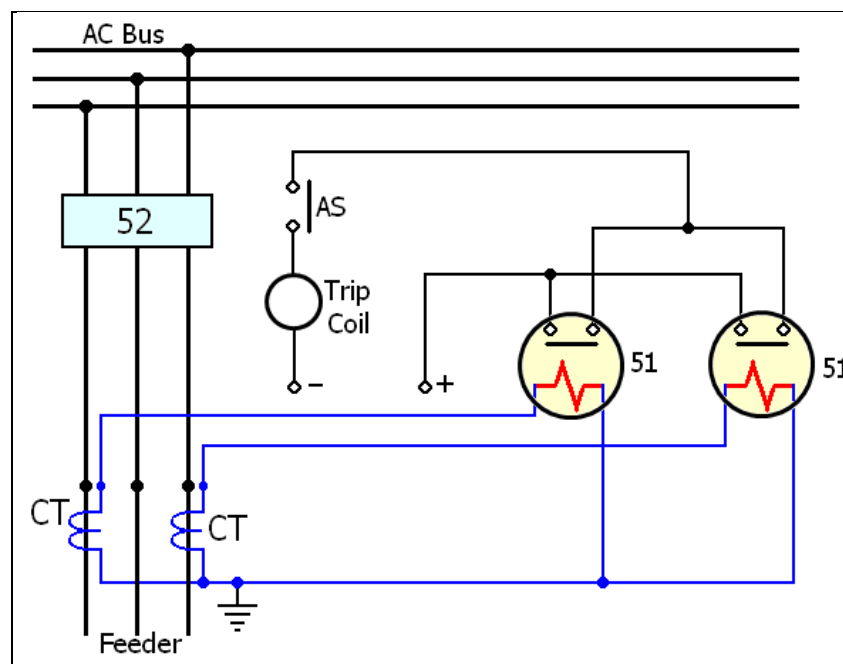
Fig. 1.2-13 Overcurrent Protection with Two Overcurrent Relays

This system is used for phase to phase fault protection and does not work in case of phase to ground fault. This scheme is used in isolated (ungrounded) networks.

TRIPPING CIRCUIT

Fig. 1.2-14 shows a typical tripping circuit. "TC" denotes the Trip Coil, which activates the breaker when fault current is detected. A seal-in circuit is normally connected across the relay contacts in order to protect against contact bounce or inadequate closure.
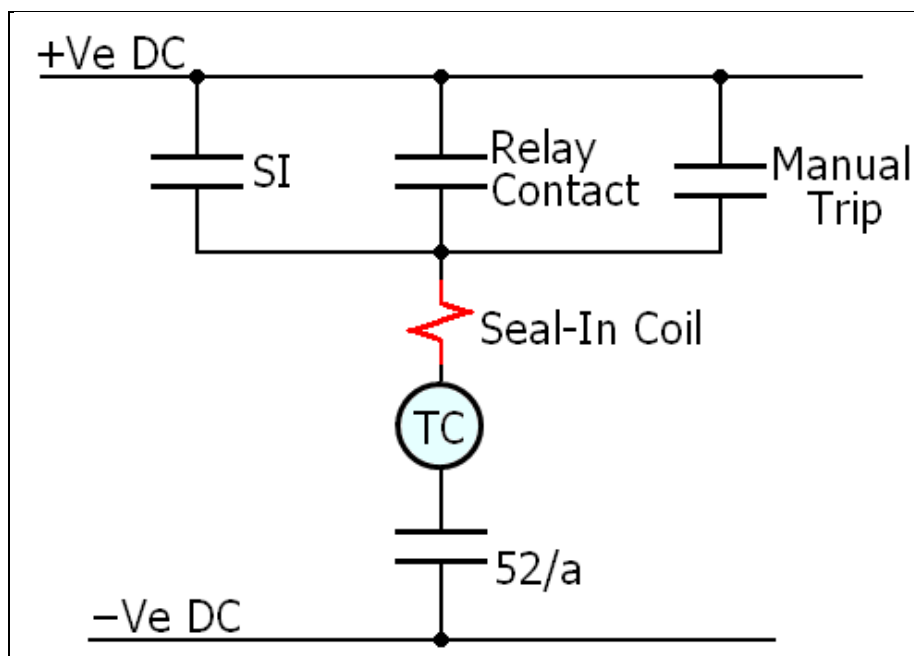
Fig. 1.2-14 Tripping Circuit

Often the time overcurrent relay includes an instantaneous element built into the same casing. The instantaneous relay tripping contacts are independent, wired in parallel with the time overcurrent tripping contacts. When the relay does operate, a target drops from either the instantaneous element or the time overcurrent element. When the relay operates, the disk rotates. If the operating signal is removed, the relay will start to reset. However, if a new operating signal is received before the relay is completely reset it will close in a shorter operating time.

TYPE IFC TIME O/C RELAY

Type IFC relay is induction disc type, as shown in Fig. 1.2-15. Relay IFC has main (Time Unit), instantaneous unit and seal-in unit. The target and seal-in unit is mounted on the left viewing from the front. Seal-in unit has its coil in series and its contacts in parallel with the contacts of time O/C unit such that when the induction unit contacts close, the seal-in unit picks up and seals-in.
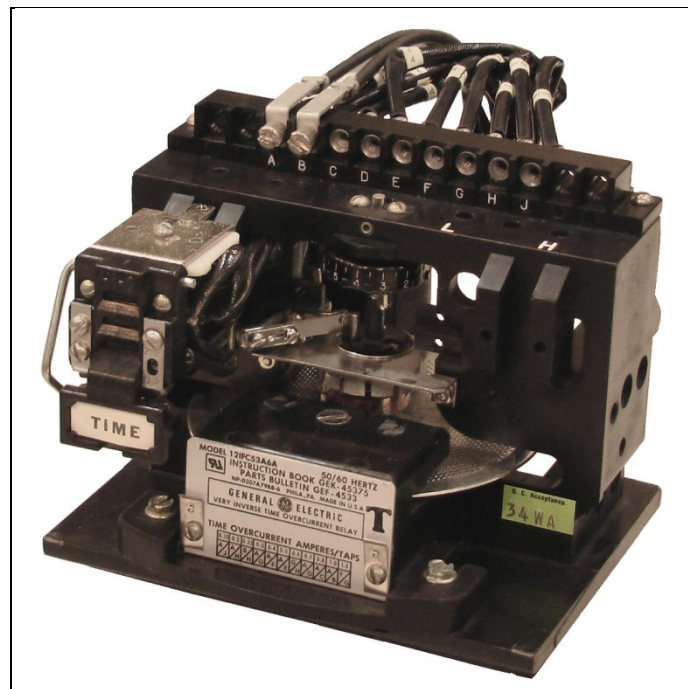
Fig. 1.2-15 Induction Disc O/C Relay Type IFC

When the seal-in unit picks up, it raises a target into view, which latches up and remains exposed until released by pressing a button. Instantaneous unit is a small hinge (clapper) type unit with contacts normally connected in parallel with the contacts of the time O/C unit and its coil is connected in series with the time O/C unit. When the instantaneous unit picks up, it raises a target, which latches up and remains exposed until it is released.

EXAMPLE 1.2-1

For the following circuit, using time-current characteristics, find the time that the overcurrent relay will delay before tripping the breaker if the primary current is 3000A and O/C relay tap setting is at 10A. The time-dial setting is at position (3).
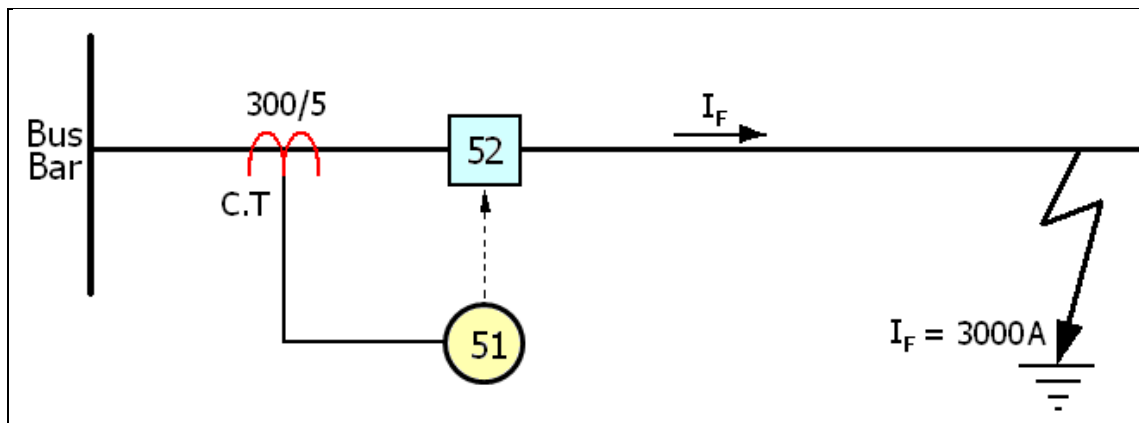
Fig. 1.2-16 Overcurrent Fault Example

SOLUTION

Secondary Fault Current = (N_P / N_S) x I_P where: $N_P / N_S = I_S / I_P$

(5/ 300) x 3000 = 50A

Multiple = 50 / 10 = 5

From the relay curves, start from the origin, select 5 multiples and then go up for the intersection with the selected curve.

When the time dial is adjusted at position(3), look for the intersection between vertical line and curve (3), then go left to get the trip time for this fault.

Trip time = 0.7 second = 700 m sec.
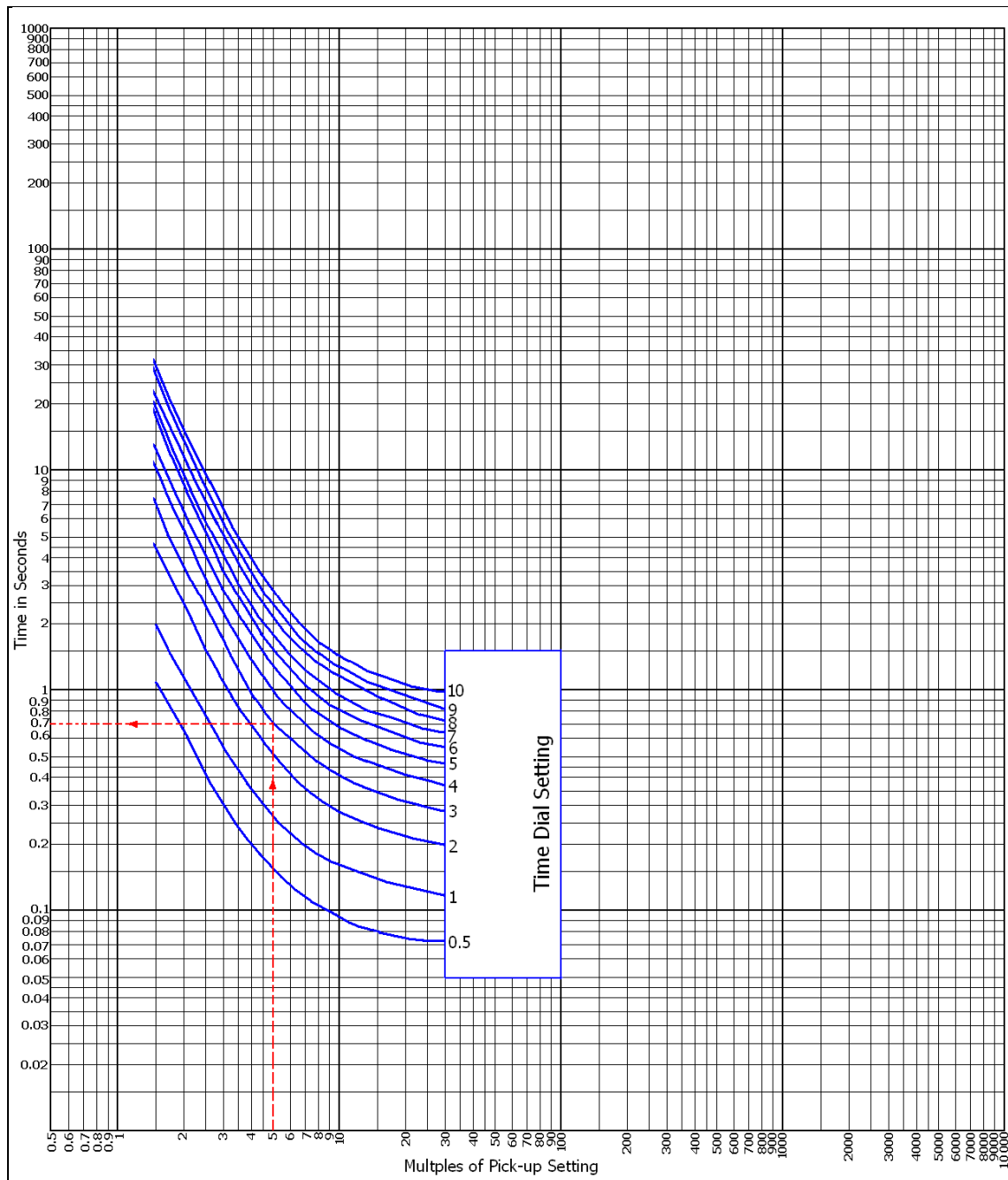
Fig. 1.2-17 Time Current Characteristics for Relay IFC-53A

Note

The major disadvantage of the induction disc relays generally, its reset time is long, when a fault F_1 occurs on feeder 1, as shown in Fig. 1.2-18. Both O/Cs of feeder 1 & that of incoming feeder, start at the same time. Feeder 1 will trip first and incoming O/C will begin to rest. If another fault F_2 happened on another feeder, the relay of the

incoming will continue operation with a less time and may trip before the faulty feeder, which means no co-ordination and false tripping.
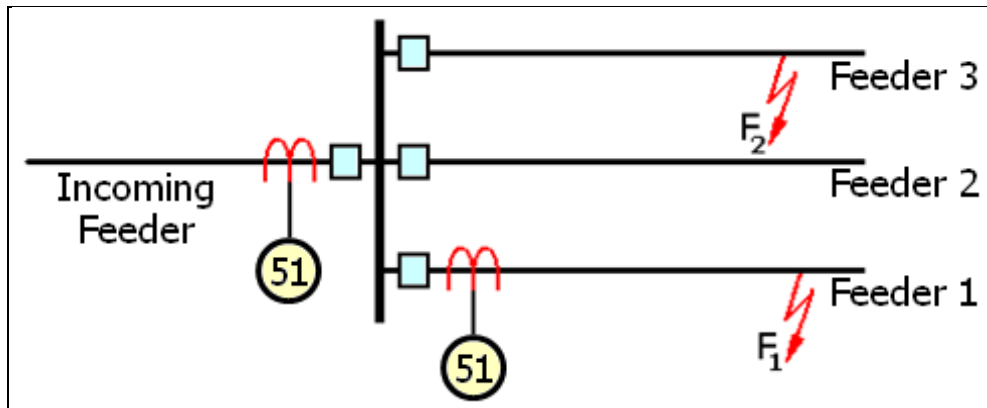
Fig. 1.2-18 Cascaded Faults on Different Outgoing Feeders

SUMMARY

- The Induction Disc Type Relay operates on a principle similar to that of an induction motor or Watt-Hour meter.

- In the Induction Disc Type Relay, the aluminum disc rotates between the pole faces of an electromagnet, which produces the sweeping flux necessary to cause rotation of the disc.

- The relay operates by torque derived from the interaction of fluxes produced by an electromagnet with those from induced currents in the plane of the rotating Aluminum disc.

FORMULAE

Torque expression: $T = K V I \cos \theta$

Where K is a constant, θ is the angle between voltage and current.

$N_P / N_S = I_S / I_P$

GLOSSARY

Inverse characteristic: Opposite relationship

Shaded pole: Part of iron core banded with a small closed cupper coil

Damping magnet: Piece of magnet used to slow down the disc

Instantaneous: Fast operation without delay

Operating torque: Tendency to rotate due to interaction of two forces shifted apart

REVIEW EXERCISE

Circle the correct answer that completes each of the following:

1. The Induction disc Relay operates on the principle of _____
    a) Fleming left hand rule   b) Fleming write hand rule
    c) Induction motors   d) Ohms low

2. To make disc of the induction disc relay rotate with constant speed, _____.
    a) The tension of the spring must be increased.
    b) Series of holes graduated in size and spacing must be provided.
    c) The tension of the spring must be decreased.
    d) All of above.

3. The main contact of induction disc type relay is made of _____.
    a) Copper.   b) Steel.
    c) Aluminum.   d) Silver.

4. The disc of induction disc type relay is made of _____.
    a) Copper.   b) Steel.
    c) Aluminum.   d) Silver.

5. Which of the following has least relay operating time?
    a. Extremely inverse time delay characteristics.   b. Very inverse time delay characteristics.
    c. Inverse time delay characteristics.   d. Instantaneous O/C unit.

6. The target in the induction disc relay is reached _____.
    a. Just as seal-in unit picks up.   b. After 35 sec.
    c. After 20 sec.   d. After 10 sec.

7. The time of contact closing of O/C time relays is _____ to the current.

    a) Directly proportional.   b) Inversely proportional.

    c) Either (a) or (b).   d) None of above.

8. Instantaneous relays may use ……………………………………………

    a. Plunger type relay.   b. Clapper type relay.

    c. Induction cylinder relay.   d. All of above.

9. An example of time delayed relay is ……………………………………

    a. Plunger type relay.   b. Clapper type relay.

    c. Induction disc type relay.   d. All of above.

10. In the induction disc relay, the moving contact is attached to:

    a. The disc.   b. Spiral spring.

    c. The pivot.   d. Damping magnet.

11. Induction disc relay coil operates with:

    a) AC   b) DC

12. In the induction disc overcurrent relay, the current setting is adjusted from:

    a) Time dial   b) Tap block

    c) Seal-in unit   d) Series resistance external the relay

13. Match the components listed below with the numbers on the induction disc O/C relay of Fig. 1.2-19.
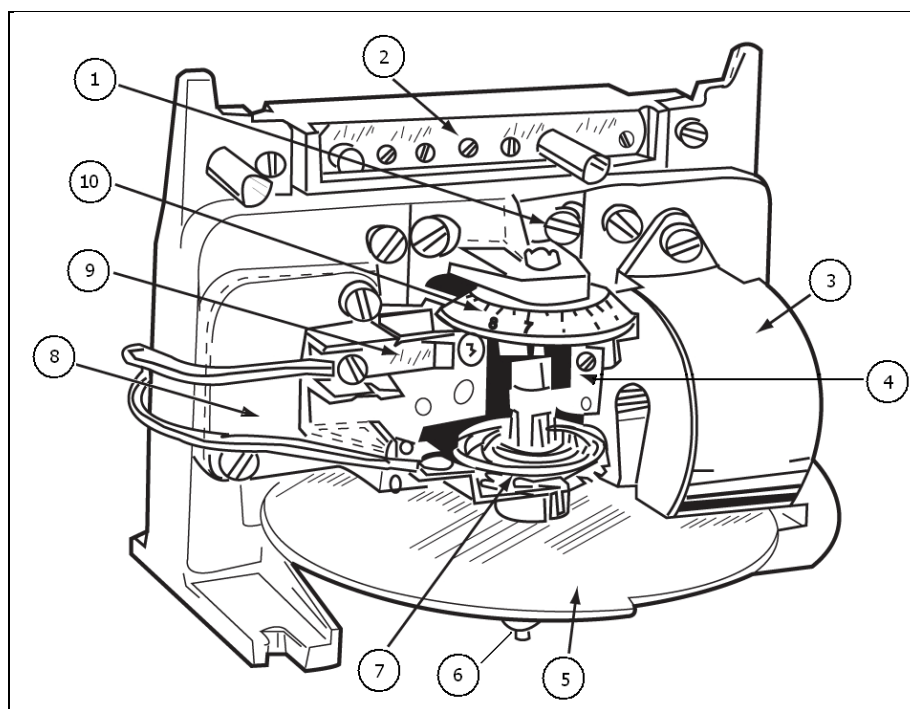
Fig. 1.2-19

1		Damping magnet
2		Spiral spring
3		Moving contact
4		Disc
5		Time dial
6		Magnet plugs
7		Jewel bearing
8		Tap block
9		Stationary contact
10		Coil

14. For the following circuit using time-current characteristics, determine the over-

15. Current relay time delay before tripping the breaker. The primary current is 6000A and O/C relay setting is at 10A tap with the time dial setting position at (0.4).
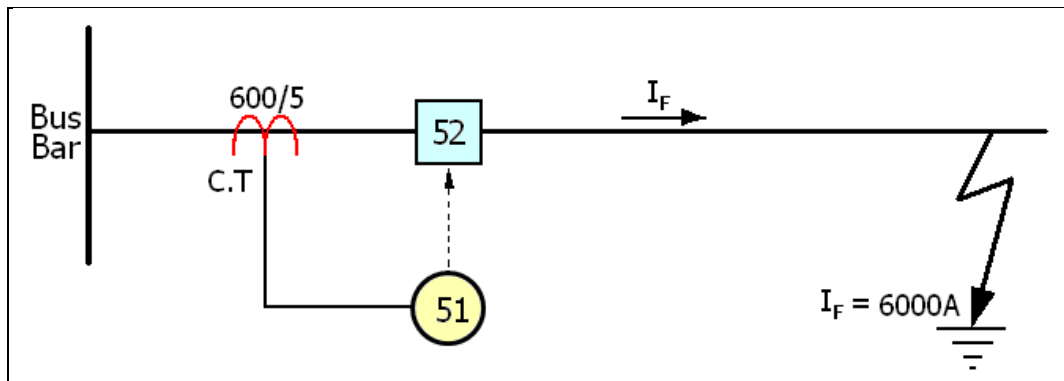
Fig. 1.2-20
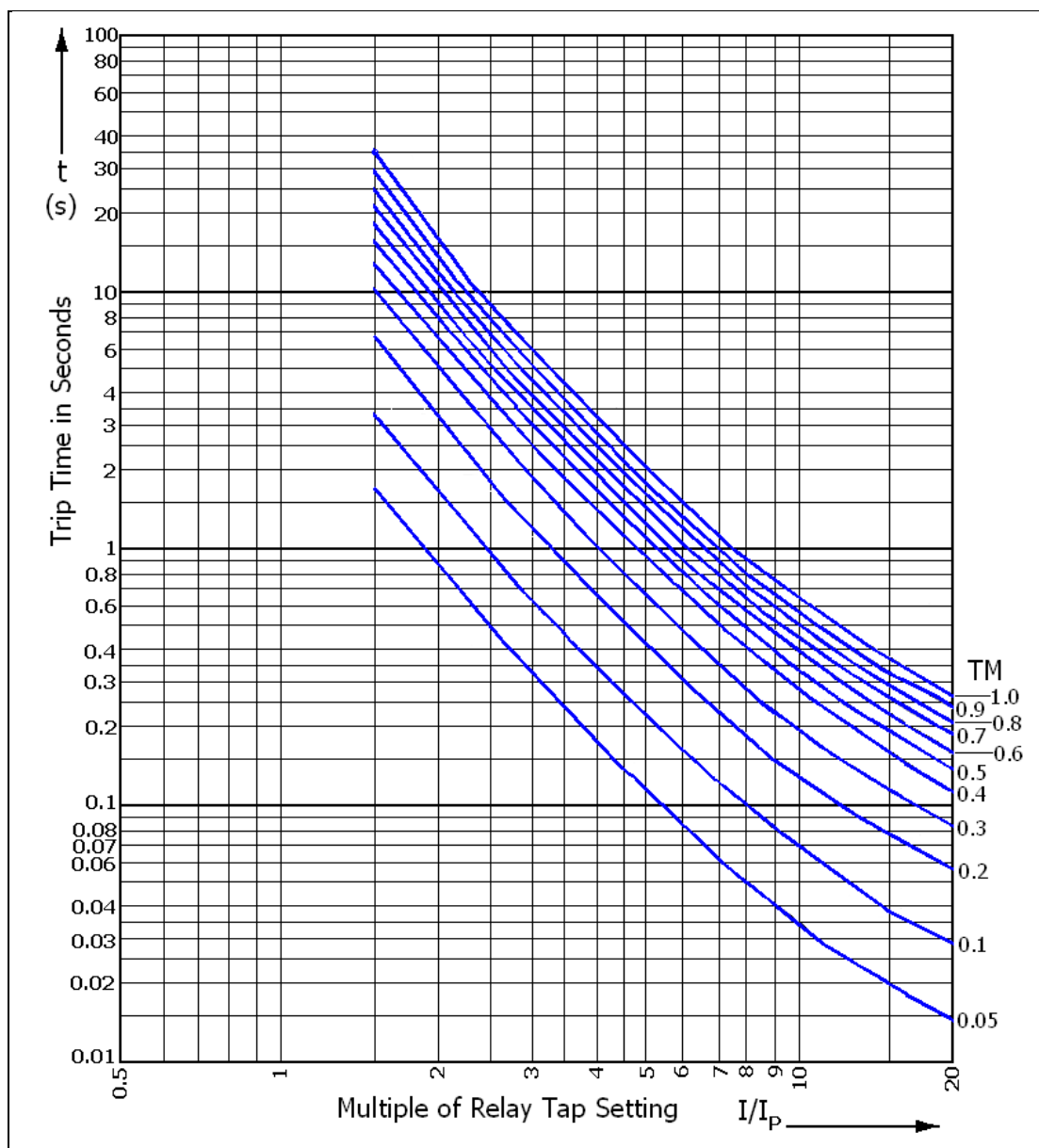
Fig. 1.2-21 Time-current Diagram for Extremely Inverse

16. Fill-in the blanks:

a. The two types of over-current relays are …….…..……...… and …….….…….…

b. The function of shading poles is: …………………………………..……..…....

c. The spiral spring is used to: …..

17. Turning the time dial of the Induction Disc Type Relay to a higher number opens the ………………………... so that it takes longer time to close them.

18. On the time-current characteristics shown below, list the names of the curves A, B, C & D.

	Description	
A		
B		
C		
D		
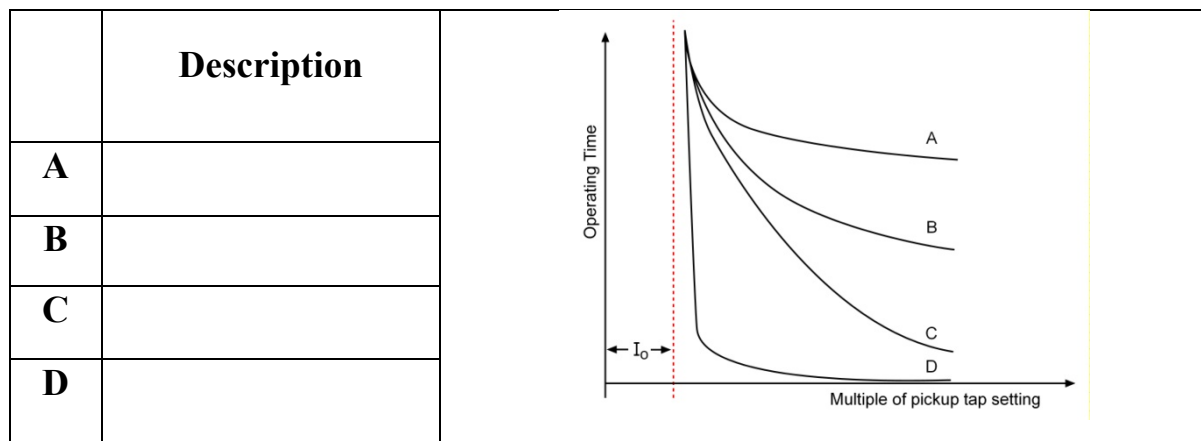
Fig. 1.2-22

19. In the circuit shown below, list devices indicated by the device function numbers:

Device Number	Description
50-1	
51-1	
52	
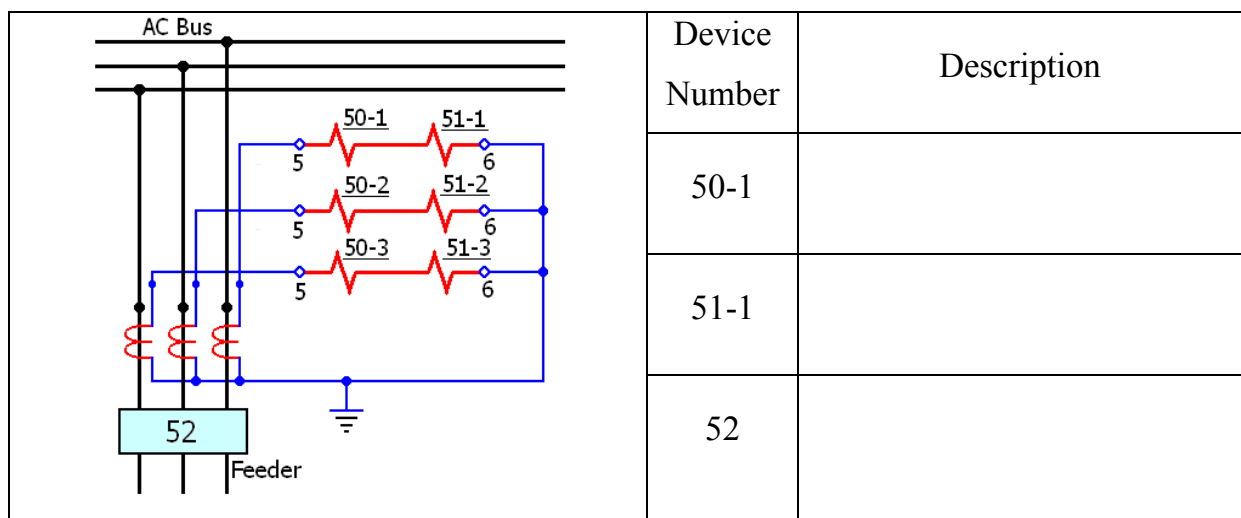
TASK 1.2-1

DEMONSTRATION FOR INDUCTION DISC RELAY

OBJECTIVE

Upon completion of this task, the participants will be able to:

- Demonstrate the parts of induction disc type relay.

TOOLS, EQUIPMENT & MATERIALS

- Induction disc overcurrent relay (any type).
- Relay tool kit
- Relay instruction manual
- Personal safety equipment as recommended in relay workshop.

PROCEDURE

Look at the induction disc relay and identify the following:

1. Identify damping magnet and target unit.
2. Identify stationary and moving contacts.
3. Identify seal in target tap selector screw and top pivot.
4. Identify tap selector block and instantaneous unit range selection link.
5. Identify instantaneous unit adjustable core, and time dial.
6. Identify the disc.
7. Identify damping magnet and shield.
8. Read the relay nameplate and determine the required information.
9. Compare the nameplate information with the relay manual data.

Fig. 1-1 Induction Disc Relay

| (a) Front View | (b) Rear View |
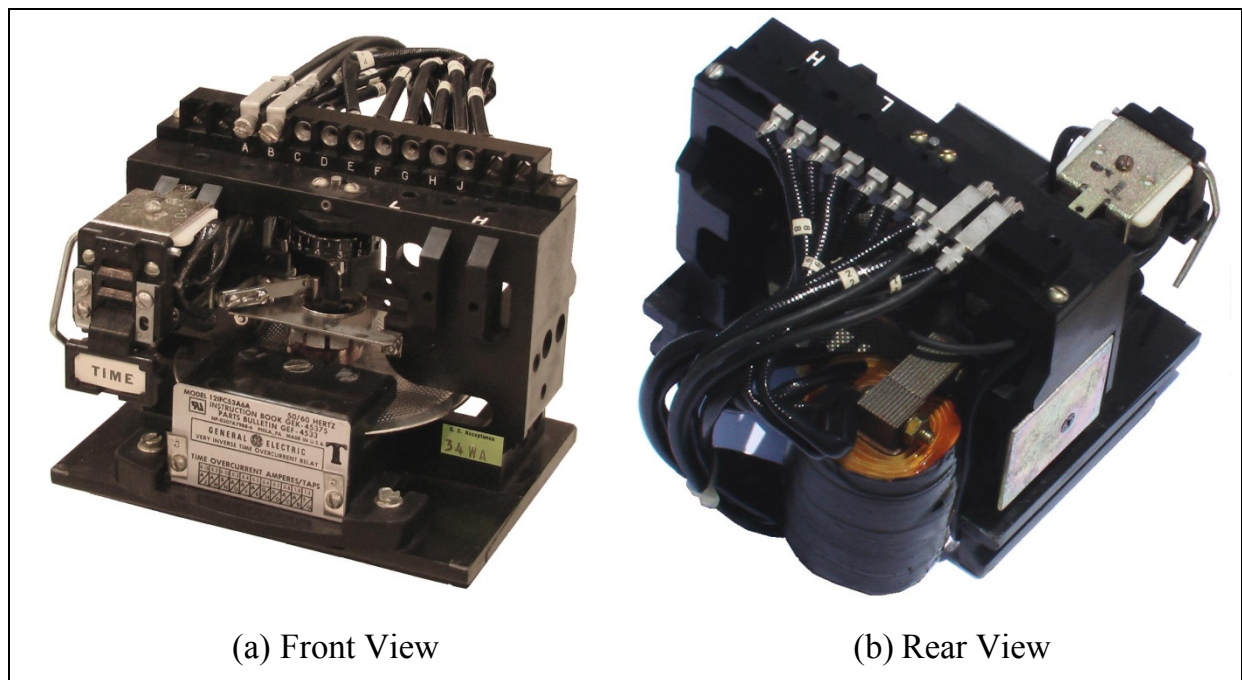
Fig. 1-2 Front & Rear Views for Induction Disc Relay

TASK 1.2-2

CHECKING FOR VERY INVERSE TIME OVERCURRENT RELAY

OBJECTIVES

Upon completion of this task, the participants will be able to:

- Check the pick-up for induction disc overcurrent relay type IFC-53A.

- Determine the reset factor (drop-out ratio).

- Check seal-in unit operation.

- Check the trip time for different current values.

TOOLS, EQUIPMENT & MATERIALS

- Induction disc very-inverse time-overcurrent relay type (GE IFC-53A)
- Relay instruction manual
- Secondary injection test set (any current source)
- AC ammeter
- Personal safety equipment as recommended in relay workshop.

PROCEDURE

OBJECTIVE 1: CHECKING PICK-UP FOR RELAY TYPE IFC-53A

1. From Table 2-1 select the operating current at (A & B) to operate the relay at 1 ampere.

2. Adjust the plug bridge of the tap block at position (A & B).

0.15A	0.2A	0.25A	0.3A	0.4A	0.5A	0.6A	0.7A	0.8A	1.0A	1.2A
A & J	A & H	B & H	A & G	A & F	A & E	G & H	A & D	A & C	A & B	F & G

Table 2-1

---

3. Connect the circuit shown in Fig. 2-1.

4. Gradually increase the current from zero, until the disc starts to move.
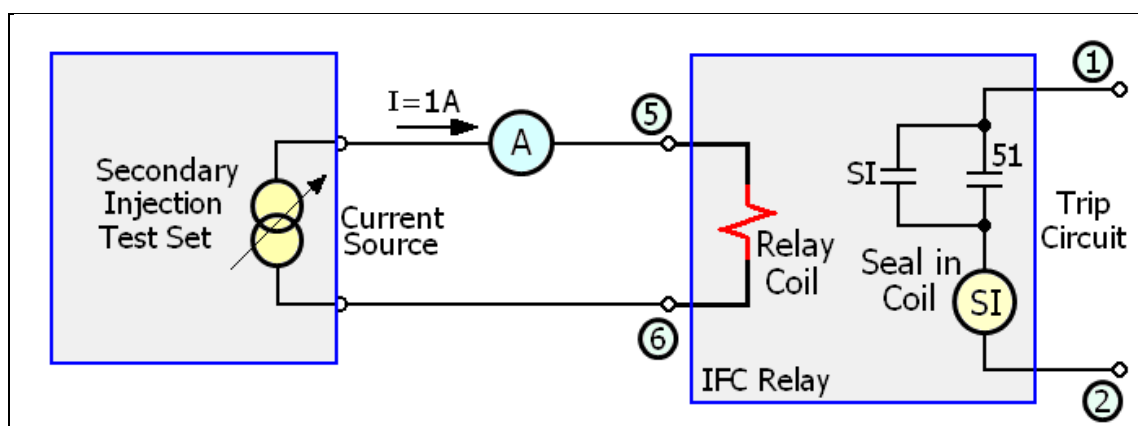
Fig. 2-1

5. Stop increasing current, look at the ammeter reading, and record its value.

6. $I_{PICK-UP}$ = ………………………………………………..ampere

7. Check the relay pick-up value with the relay current setting of the tap block.

8. You should find that the pick-up result agrees with the relay current setting, within a tolerance of ±3 % as recommended in the relay manual.

9. Gradually, decrease the injection current until the relay disc starts to return.

10. Record the current when the disc starts to return.

11. $I_{DROP-OUT}$ = ………………………………………………..ampere

OBJECTIVE 2: CHECKING RESET FACTOR (DROP-OUT RATIO)

18. Calculate reset factor (Drop Out Ratio) for the induction disc relay:

   % Drop Out Ratio = ($I_{DROP-OUT}$ / $I_{PICK-UP}$) x 100 = ...

19. A good drop out ratio, should be more than 90%

20. Return the current source to zero and shut down supply.

OBJECTIVE 3: CHECKING SEAL-IN UNIT PICK-UP

1. Connect the circuit shown in Fig. 2-2.
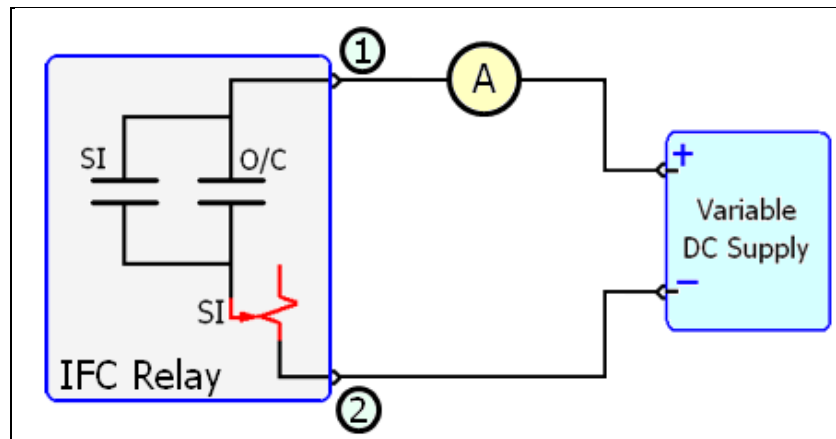
Fig. 2-2 Testing the Seal-in Unit

2. Adjust the time dial setting at zero position to insure that overcurrent contact closed.
3. Adjust the current selector of the seal-in unit at 0.2 A.
4. Carefully increase the DC output current of the supply until the SI contact closes.
5. Record the ammeter reading.

I_{SI} = ………………………………………….A dc

Note 1: Seal-in unit of the used relay has two options for current selector.

- 0.2 A option for using with auxiliary relay.
- 2.0 A option for using with trip coil directly.

Note 2: This test should be done before trip time test to insure that the time dial setting is restored.

OBJECTIVE 4: CHECKING TRIP TIME FOR RELAY TYPE IFC-51K

1. On the relay terminal block, select the position (A & B) for 1 ampere setting as indicated in table 2-1.
2. Adjust time dial setting at position (3).

3. Connect the circuit shown in Fig. 2-3.

4. Connect the timer-off posts of the tester to the relay contact.
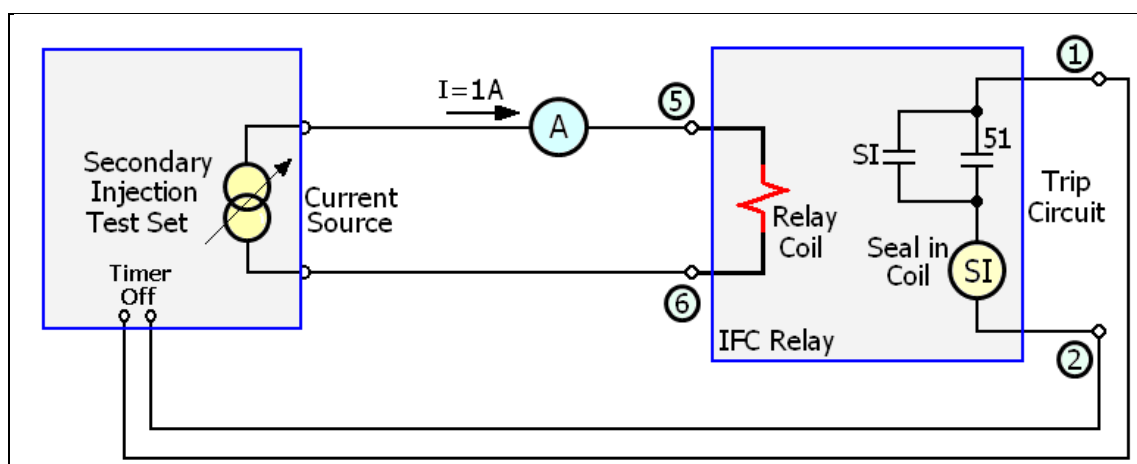
Fig. 2-2

5. Adjust the current to 2A, reset the timer, and start to inject the current to the relay.

6. Note the relay disc when it starts to move slowly, the timer counts then stop counting when the contact closes.

7. Timer record (trip time) = ………………………..seconds

8. Compare this value with the determined trip time on the characteristic curve of the relay shown in Fig. 2-3.

9. They must be equal within a tolerance of ±7 % as recommended in the relay manual.

10. Repeat steps 5 to 9 with injection current of 5A.

11. Note that disc rotates faster than in the last operation and the timer records a time smaller than the last record.

12. Timer record = ………………………..second

13. Compare the two time records of the two cases.

14. Return the current to zero, then switch-off the injection set.
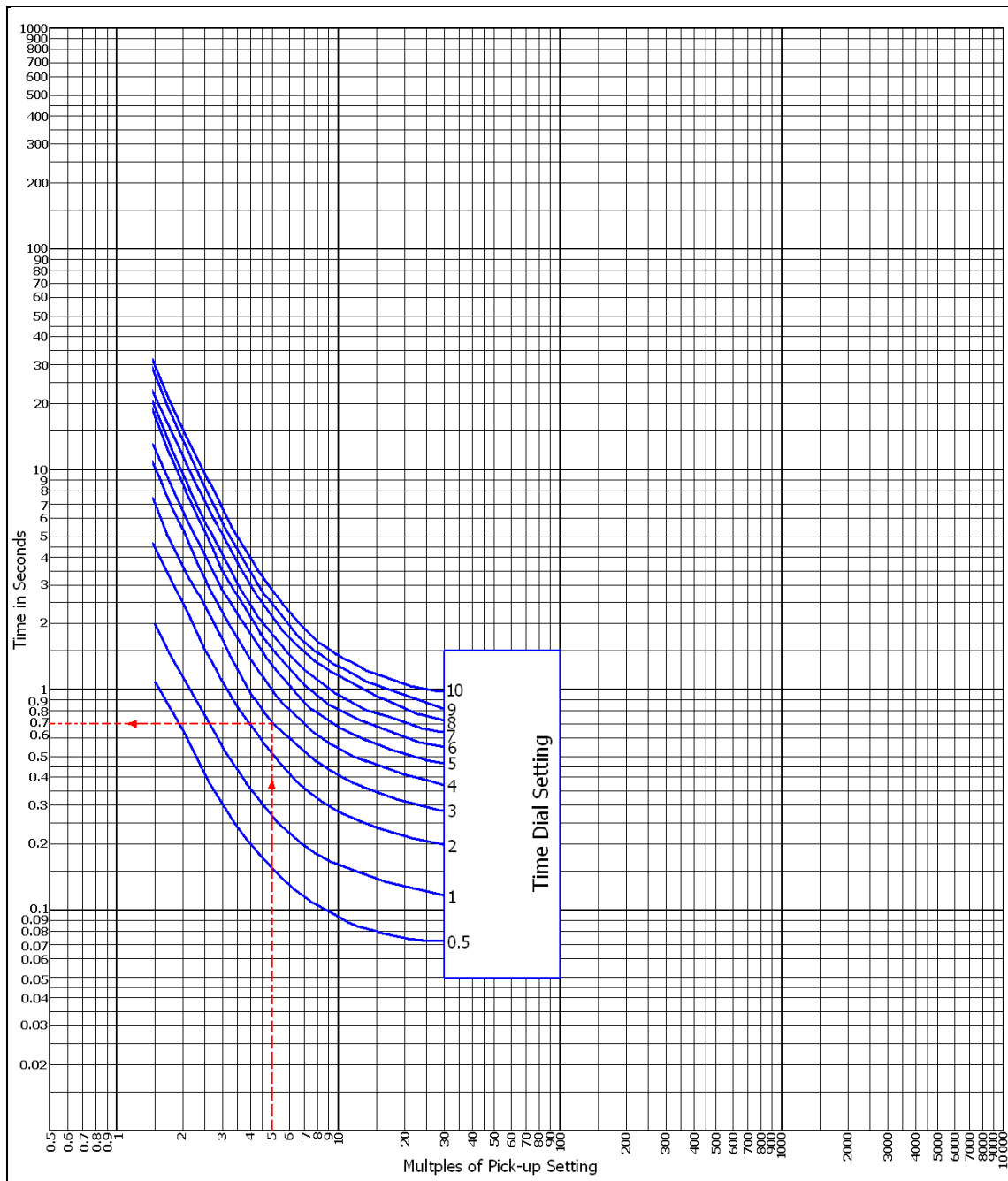
Fig. 2-3

CONCLUSION

As the current increases, the operating point on the curve gives less time to close the trip circuit and vice versa.

LESSON 1.3

VOLTAGE RELAYS

LESSON 1.3

VOLTAGE RELAYS

OVERVIEW

This lesson discusses the construction and application of induction disc relay in over/under voltage protection. It spotlights on the setting and operating characteristics of the electromagnetic induction disc overvoltage relay, type IAV, as an example.

OBJECTIVES

Upon completion of this lesson, the trainees will be able to:

- Identify the construction of induction disc voltage relay.

- Demonstrate the operating characteristics of induction disc voltage relay.

- Perform the adjustment and calibration of voltage and time setting for IAV type relay.

Task 1.3-1: Checking for induction-disc over-voltage relay.

INTRODUCTION

Induction disc voltage relay is an example for single input quantity for the induction disc relay unit. It may be used as over or under voltage protection application. The voltage relay is designed to de-energize the power circuit whenever voltage falls below or rises above a predetermined value. Over voltage relay has the opposite operation of the under voltage.

OVER /UNDER VOLTAGE RELAY

The relay types used for overcurrent and undercurrent can be designed for over voltage or under voltage when the actuating quantity is voltage instead of current, with some modifications in the relay design. This type of protective relays are designed to give an alarm or trip whenever the voltage applied to their operating coils reaches some predetermined value. When a delay time is required for co-ordination with another protective device, it can be done by adjusting time dial of the relay unit.

Single-phase voltage relays are used extensively in voltage regulation, checking voltage difference between sources, shutting down or preventing the operation of machines with low voltage and other similar functions.

FUNCTION AND APPLICATION

Overvoltage relays are used in a variety of applications for switching or alarming.

The applications through special potential transformer connections are also common. Thus, they can be used as ground detectors on a delta system. The voltage coil can be tuned with a series capacitor to block the third harmonic and used as a ground detector for an AC generator armature circuit.

Under voltage relays are generally used to detect harmful, abnormal low voltage on a system. They can also be used to transfer to a standby source, trip a load off-line or simply to give an alarm. The designer specifies a tap setting representing a percent of

normal voltage, a time dial position, and a specific type of relay with an operating curve so as to coordinates with other relays.

OPERATING PRINCIPLES

Voltage relay construction of an electromagnetic type, as shown in Fig. 1.3-1, is very similar to that of an overcurrent relay. Components on a voltage relay serve the same purpose as those of an overcurrent relay. The major difference is in the operating coil. An overcurrent relay's operating coil is wound with a few turns of thick wire. Those of a voltage relay are wound with many turns of fine wire.
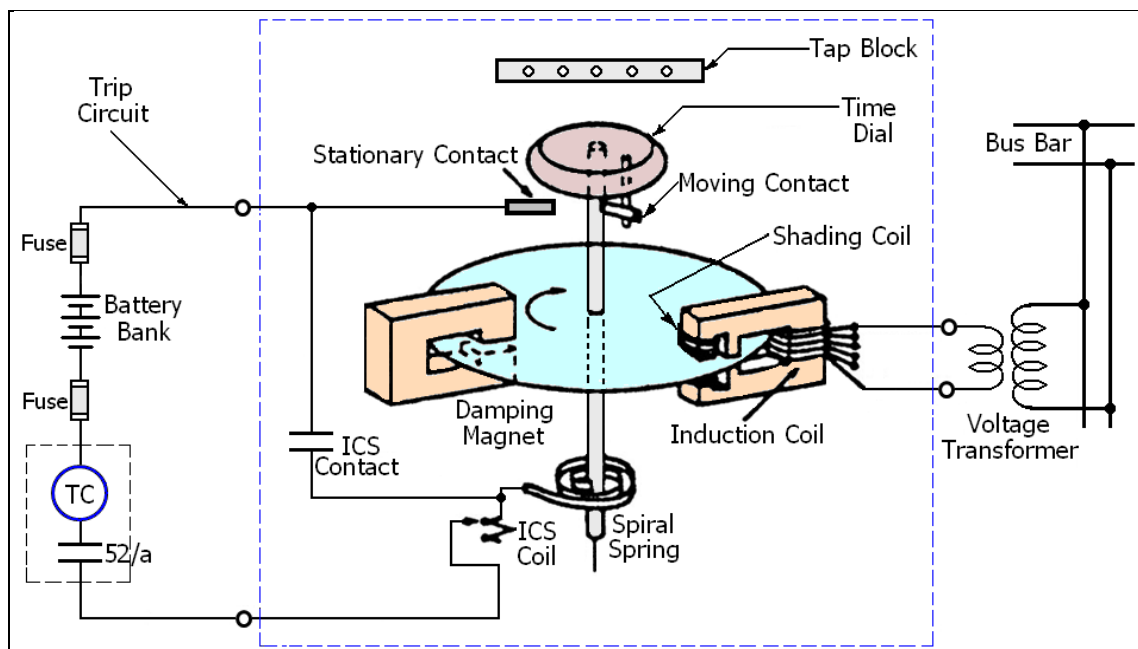
Fig. 1.3-1 Construction of Voltage Relay

The voltage relay has tap block to select the voltage setting such as 70, 90, 100, 105, and 110 as a minimum pick-up voltage. Operation of the voltage relay states that two fluxes are induced into an aluminum disc producing two forces, which results in torque to rotate the disc. The developed torque is proportional to the amount of magnetic flux induced into the disc, which also is directly proportional to the voltage that appears on the primary of the potential transformer that the relay is connected to.
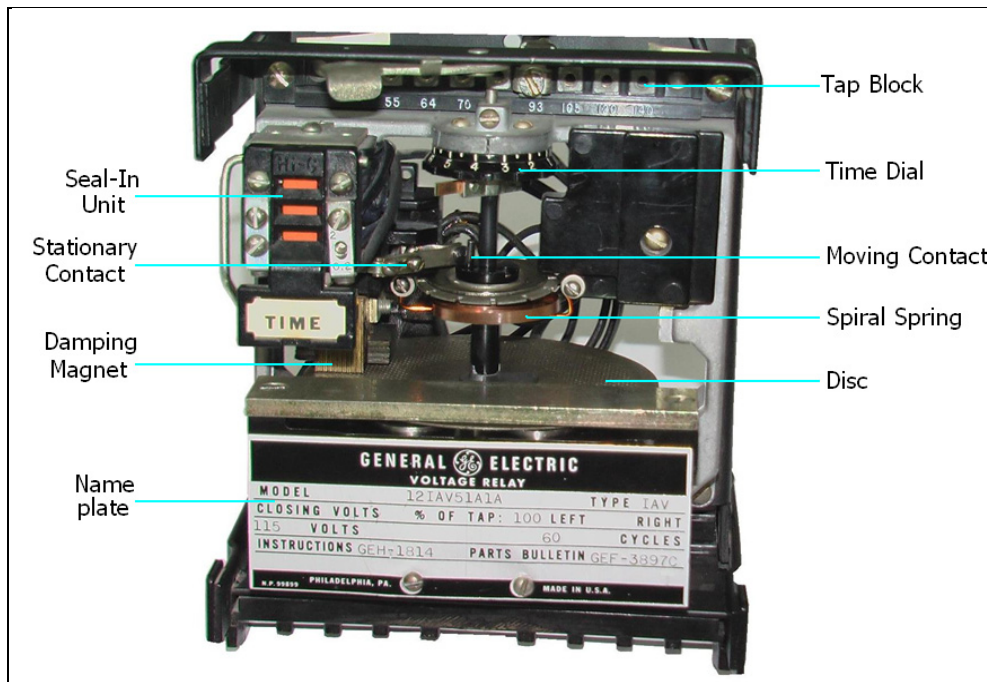
Fig. 1.3-2 Voltage Relay Type IAV

OVERVOLTAGE RELAY TYPE IAV

The device function number of over voltage relay is (59); some types can be used as voltage indicators to show if the supply voltage exists or not. In addition, it can be used to detect over voltage.

(a) AC Circuit   (b) DC Circuit
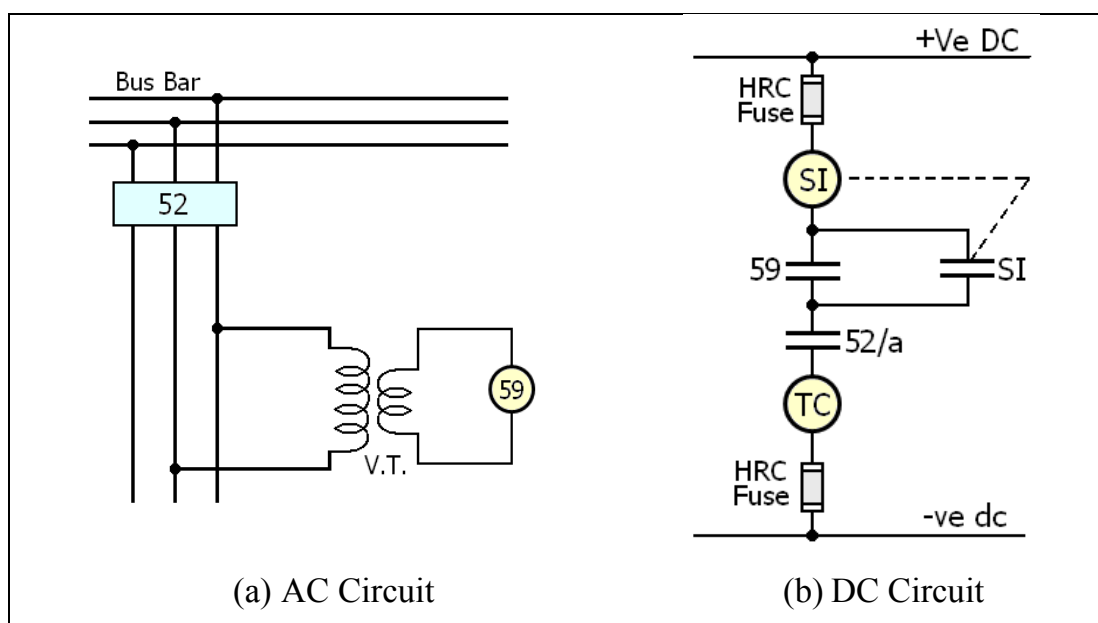
Fig. 1.3-3 Connection Diagram of Over Voltage Relay

For generator, it is a standard practice to provide overvoltage protection. A sudden loss of load may result in over speed and overvoltage. Figs. 1.3-4 and 1.3-5 show an application for overvoltage and earth fault protection for generator.

(a) AC Circuit   (b) DC Circuit
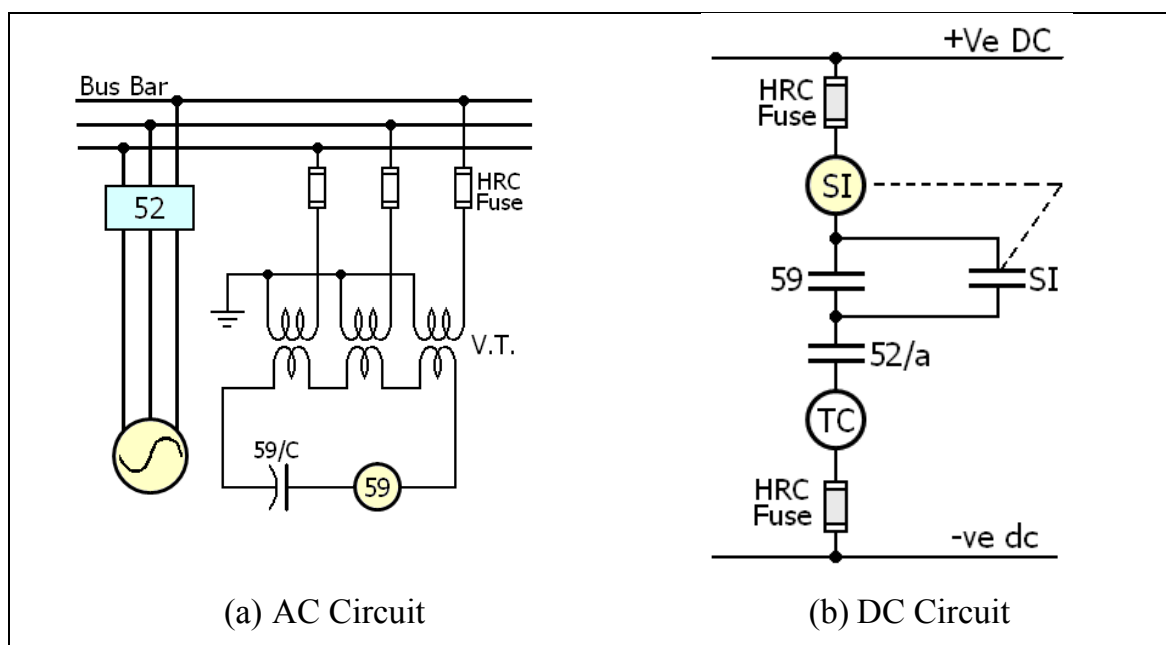
Fig. 1.3-4 Generator Protection against Earth Fault

(a) AC Circuit   (b) DC Circuit
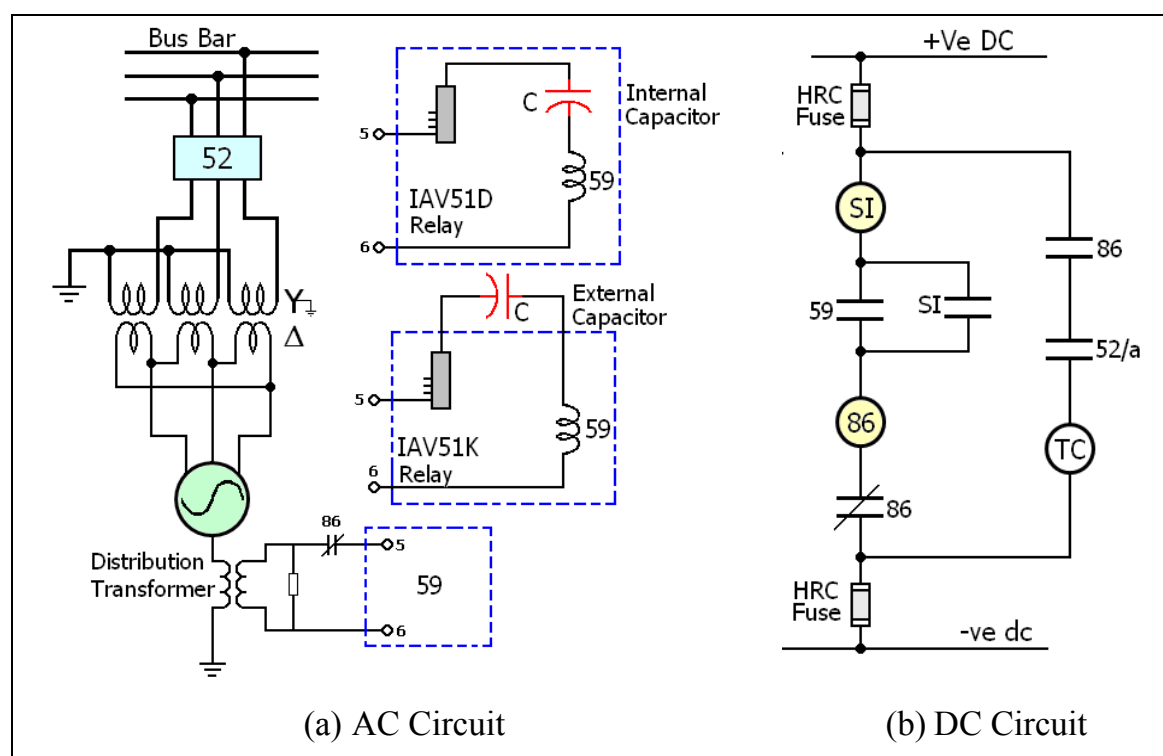
Fig. 1.3-5 Connection of Over Voltage with Lockout Relay

The capacitor 59/C is used as harmonic filter for the leakage current (zero sequence current) inside the delta connection of the voltage transformer secondary. It converts leakage current to voltage applied to the relay.

The lockout relay 86 is an electrically operated and hand or electrically reset auxiliary relay. It is operated upon the occurrence of abnormal conditions to maintain associated equipment or devices out of service until it is reset.

EXAMPLE 1.3-1

For the circuit shown in Fig. 1.3-6, the relay voltage tap setting is 90V, the relay rating is 115V, and time dial is 6. If the voltage reaches 135V, what is the trip time of the relay?
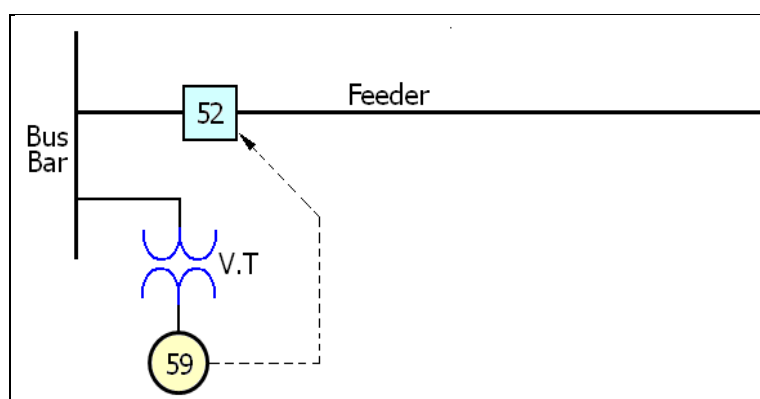
Fig. 1.3-6

SOLUTION

Percentage of tap voltage = (135 /90) x 100 = 150%

Use the voltage-time characteristic curves of Fig. 1.3-7 to determine the tripping time as follow:

1- From the characteristic curves select the percentage value of 150%
2- Go up vertically until the intersection with the curve of time dial 6
3- Go horizontally left to get the trip time of 6.5 seconds
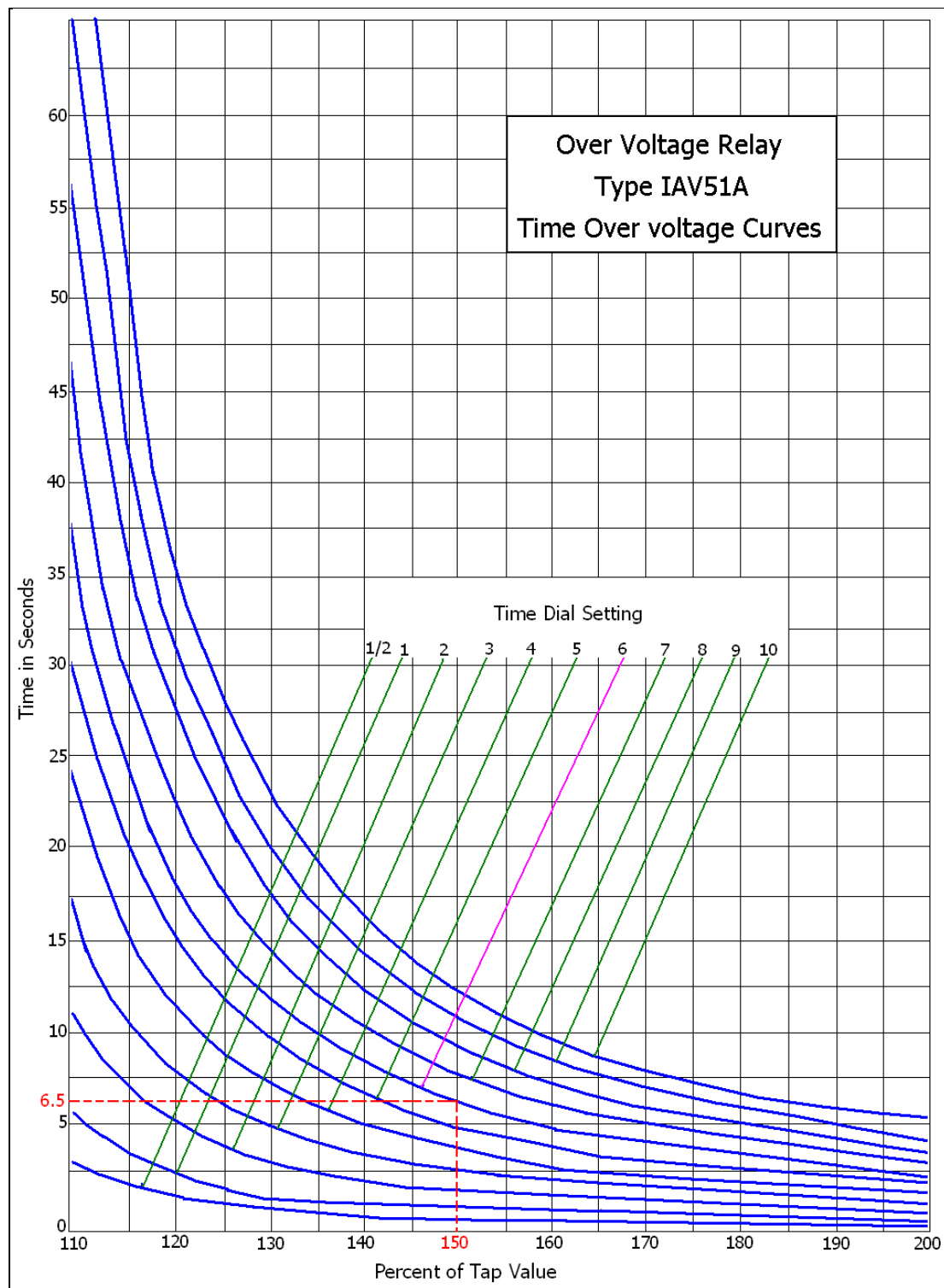
Fig. 1.3-7

LOCK-OUT RELAY (LOR)

The function of lock-out relay is to prevent energizing the protected equipment after tripping by the main protection before acknowledge and clearing the fault.

The LOR contacts shown in Fig. 1.3-8a are normally closed in the reset position. To command the lock-out relay to trip (Fig. 1.3-8b & c), S_1 (protection trip contact) is closed. This completes the circuit across the LOR trigger solenoid, which causes the device to snap to the trip position. It locks into this position and remains there indefinitely.

One NO contact of LOR (Fig. 1.3-8d) is used to complete the CB trip circuit and NC contact may be used to block the CB closing circuit.

When this happens, the LOR contact opens. The unit will stay locked-out in the trip position until manually reset. The condition of the lock-out relay is visible by the hand location and a mechanical target (black for reset, orange for trip).
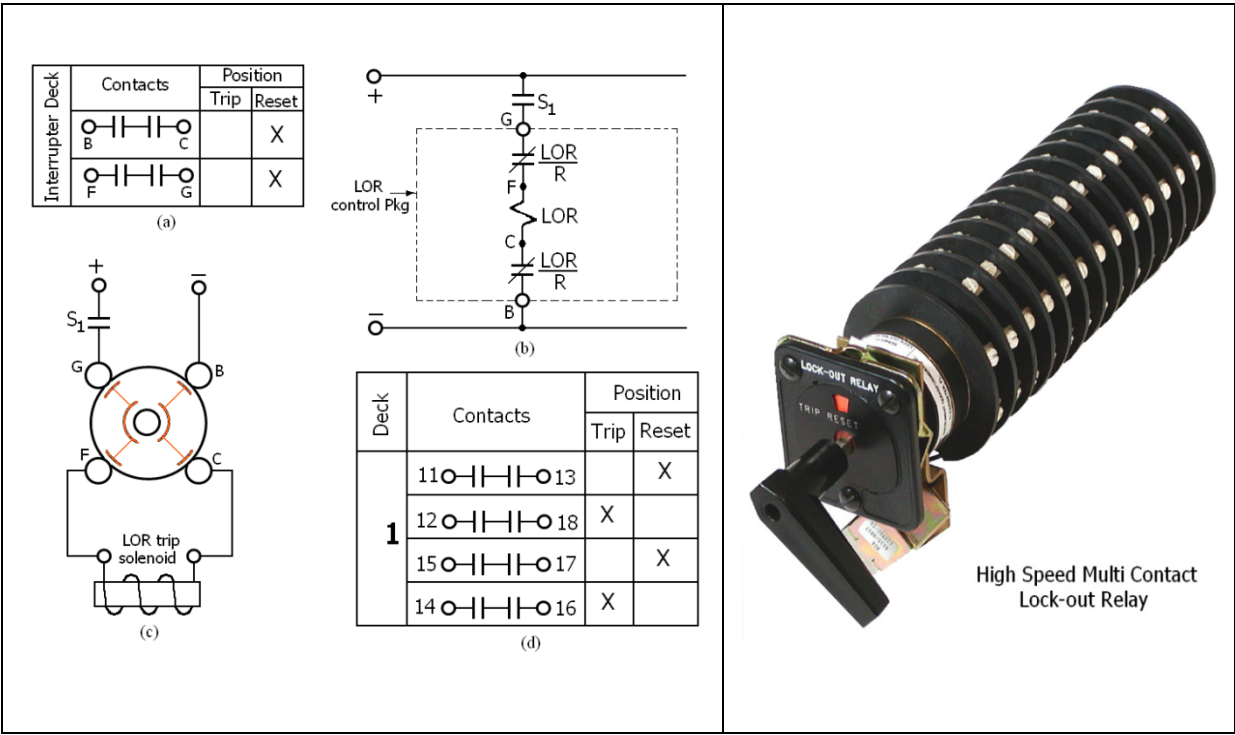
Fig. 1.3-8 Manual Reset Lock Out Relay (LOR)

SUMMARY

- Induction disc overvoltage relay is an example for single input quantity for an induction relay, which is fed from voltage transformer.

- Overvoltage relay always has NO contact and high resistance relay coil.

- Under voltage relay always has NC contact and high resistance relay coil.

- Overvoltage relay may be used to protect generator against voltage increase.

- Overvoltage relay may be used to protect generator against earth fault.

- At the application of earth fault protection, series filter capacitor is needed to filter harmonics due to leakage current.

- In the IAV-51D relay, the capacitor is built in inside the relay package.

- In the IAV-51K relay, the capacitor is connected externally.

- Generally IAV relay is adjusted for voltage and time through tap block and time dial respectively.

GLOSSARY

Filter capacitor:	An electric component used for harmonic elimination.
Seal-in unit:	An auxiliary relay built in inside the relay used for self holding for the trip circuit.
Drag magnet:	A damping magnet helps the disc to rotate stably.

REVIEW EXERCISE

Circle the letter a, b, c or d that correctly completes the statement and follow the directions to answer the other questions:

1. Low voltage supply causes motors to ....

   a) Draw less current.   b) Draw more current.

   c) Increase the speed.   d) Neither (a)' nor (b).

2. The over voltage may happen because of ……………………………

   a) Inductive loads on short T.L.   b) No load or light loads on long T.L.

   c) Earth fault occurring.   d) All of the above.

3. As the voltage drops, the AC motors must be switched off …………………

   a) By under-voltage relay.   b) Instantaneously.

   c) By over-voltage relay.   d) Then switch on.

4. Indicating contactor switch (seal-in) relays is ....type.

   a) Induction disc.   b) Induction cylinder.

   c) Clapper.   d) Balanced beam.

5. Range of over / under-voltage relays type IAV-51A is ……………

   a) 55-140 V.   b) 200-350 V.

   c) 40-100 V.   d) 30-90 V.

6. For under voltage relay, the contacts must be ……………

   a) Normally open.   b) Normally close.

   c) Limit switches.   d) Auxiliary switch.

7.   Voltage relay coil must have ....

a) Very low resistance and low number   b) Very high resistance and high
   of turns.   number of turns.

c) Very low resistance and high number   d) Very high resistance and low number
   of turns.   of turns

8.   For the over voltage relay, the contacts must be ……………

 a) Normally open   a. Normally closed.

 b. Limit switches.   c. Auxiliary switch.

9.   Draw an ac circuit of an overvoltage relay, showing the connection of its coil with
     VT and CB.

10. Draw a dc circuit of an overvoltage relay, showing the relay contacts, seal in coil,
    contact, and trip coil of CB.

11. For the circuit shown in Fig. 1.3-9, the relay voltage tap setting is 105V, the relay
    rating is 115V, and time dial is 5. If the relay voltage reaches 142V, determine the
    trip time of the relay, using type IAV-51A and its characteristics is shown in Fig.
    1.3-10.
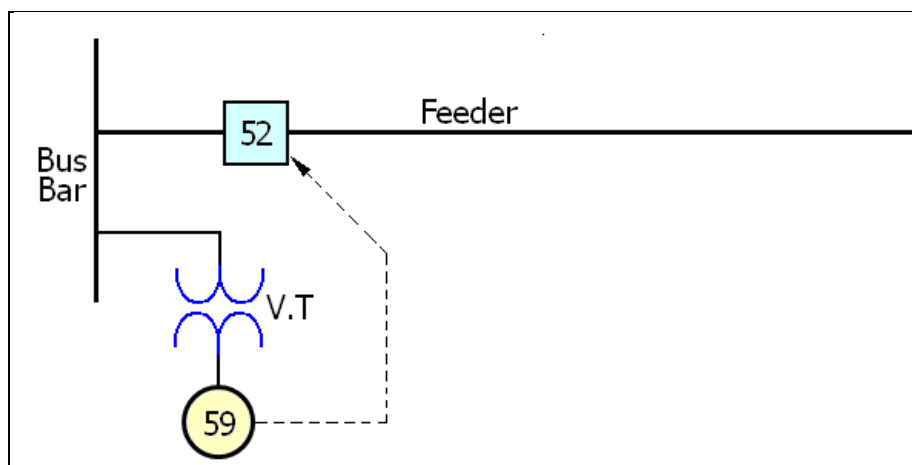
Fig. 1.3-9
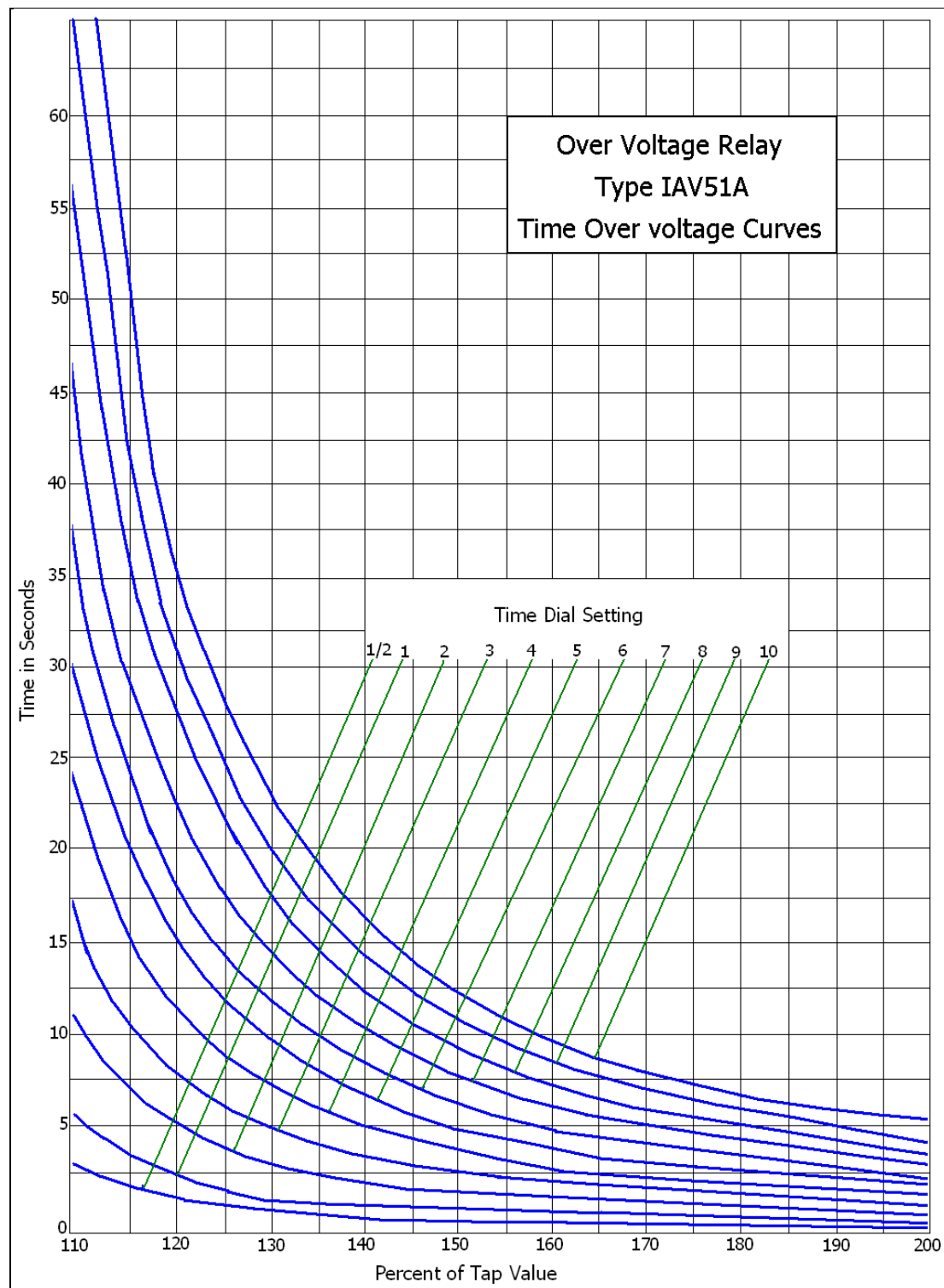
Fig. 1.3-10

TASK 1.3-1

CHECKING FOR INDUCTION DISC OVER VOLTAGE RELAY

OBJECTIVES

Upon completion of this task, the participants will be able to:

- Identify the parts of IAV-51A induction disc voltage relay

- Check pick-up value for IAV-51A induction disc voltage relay

- Check reset factor (drop-out ratio)

- Check trip time for IAV-51K induction disc voltage relay

TOOLS, EQUIPMENT & MATERIALS

- Induction disc voltage relays (GE IAV-51A & GE IAV-51K type).
- Relay instruction manual
- Secondary injection test set (any voltage source type).
- AC voltmeter.
- Personal safety equipment as recommended in relay workshop.

Note objectives 1, 2 & 3 of the task are applied on over voltage relay type IAV-51A. Objective 4, of the task is applied on earth fault relay type IAV-51K.

PROCEDURE
OBJECTIVE 1: IDENTIFICATION OF THE VOLTAGE RELAY TYPE IAV

1. Remove the relay from the casing carefully.
2. Identify and read the nameplate of the voltage relay unit.
3. Identify and inspect the tap block and which position the plug is set to.
4. The tap block position is set for one of the following voltages:

55V, 64V, 70V, 93V, 105V, 120V, & 140V

5. Identify and inspect the time dial in the voltage relay.

6. The time dial is set for one of the following positions: 1/2, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 & 11.
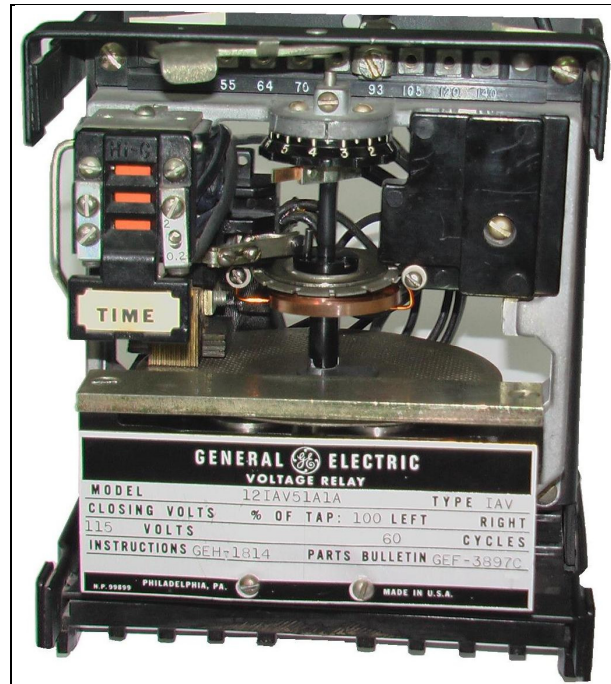
Fig. 1-1 Induction disc voltage relay (GE IAV-51A type)

7. Identify and inspect the control spring assembly.

8. Identify and inspect the disc shaft.

9. Identify and inspect the damping (drag) magnet.

10. Identify and inspect the following parts:

- Relay coil

- Stationary and moving contacts

- Indicating contactor switch (ICS)

OBJECTIVE 2:

CHECKING PICK-UP VALUE FOR VOLTAGE RELAY TYPE IAV-51A

1. Adjust the plug of the tap block at 100V.
2. Connect the circuit, as shown in Fig. 1-2.
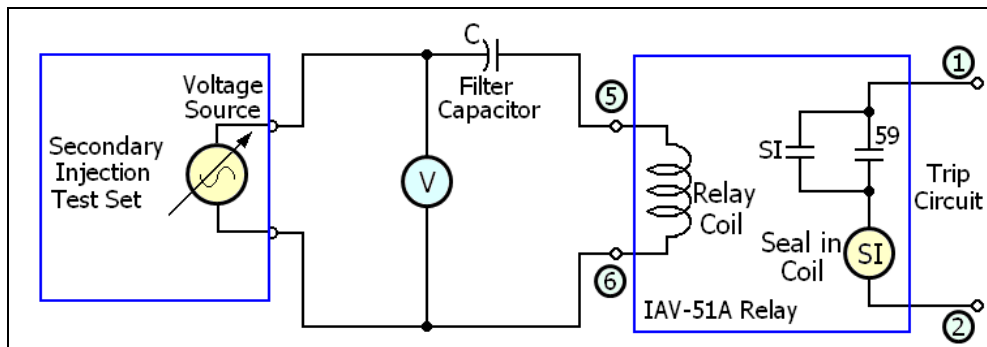
Fig. 1-2

3. Connect the power supply and start with zero output voltage.
4. Gradually increase the voltage until the disc start to move.
5. Stop increasing the voltage, record the voltmeter reading.

    $V_{PICK-UP}$ = ………………………..

    Check the relay pick-up value with the relay voltage setting of the tap block.

    You should find that the pick-up result agrees with the relay voltage setting, within ±5% error as per the relay manual.

OBJECTIVE 3: CHECKING RESET FACTOR (DROP-OUT RATIO)

6. Calculate reset factor or % Drop Out Ratio for the induction disc voltage relay type IAV-51A:

    % Drop Out Ratio = ($I_{DROP-OUT}$ / $I_{PICK-UP}$) x 100= ....

Note a good drop out ratio, which % Drop Out Ratio is more than 90%

7. Return the source voltage to zero and shut down the injection test set.

OBJECTIVE 4: CHECKING TRIP TIME FOR THE VOLTAGE RELAY TYPE IAV-51K

1. Connect the circuit as shown in Fig. 1-3
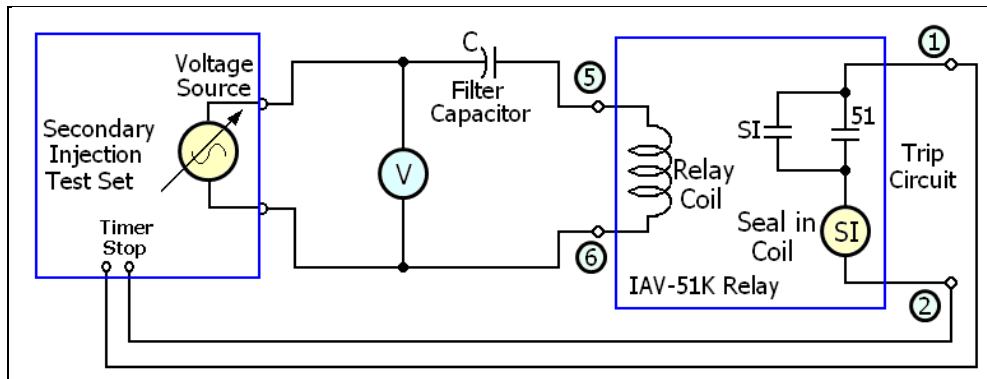
Fig. 1-3

2. Select the setting data from table 1-1

3. Rated voltage is 67V, tap voltage setting is 5.4(A), and time dial setting = 5

RELAY TYPES	VOLTAGE RATING	TAP**SETTING	VOLT-AMPS	POWER FACTOR	WATTS
60 - Cycle Burdens Rated Voltage					
IAV51D	345	A(28)	41.5	0.37	15.5
		B(42)	35.0	0.62	21.6
		C(70)	23.9	0.85	20.3
		D(112)	13.6	0.95	12.9
IAV51K	67	A(5.4)	34.0	0.31	10.5
IAV52K		B(7.5)	31.0	0.52	15.9
		C(12.5)	23.1	0.77	17.7
		D(20	16.0	0.9	14.4
	115	No Taps	24.2	0.21	5.0
IAV52C	199	No Taps	32.0	0.31	9.9
	345	No Ta s	41.5	0.37	15.5
1AV51D	115	A(10)	36.8	0.34	12.6
		B(15)	30.8	0.62	19.0
		C(25)	20.3	0.86	17.4
		D(40	12.7	0.95	12.0
IAV51D	199	A(16)	25.4	0.28	7.0
		B(24)	23.1	0.5	11.5
		C(40)	17.8	0.74	13.3
		D(64)	12.4	0.88	11.0

Table 1-1
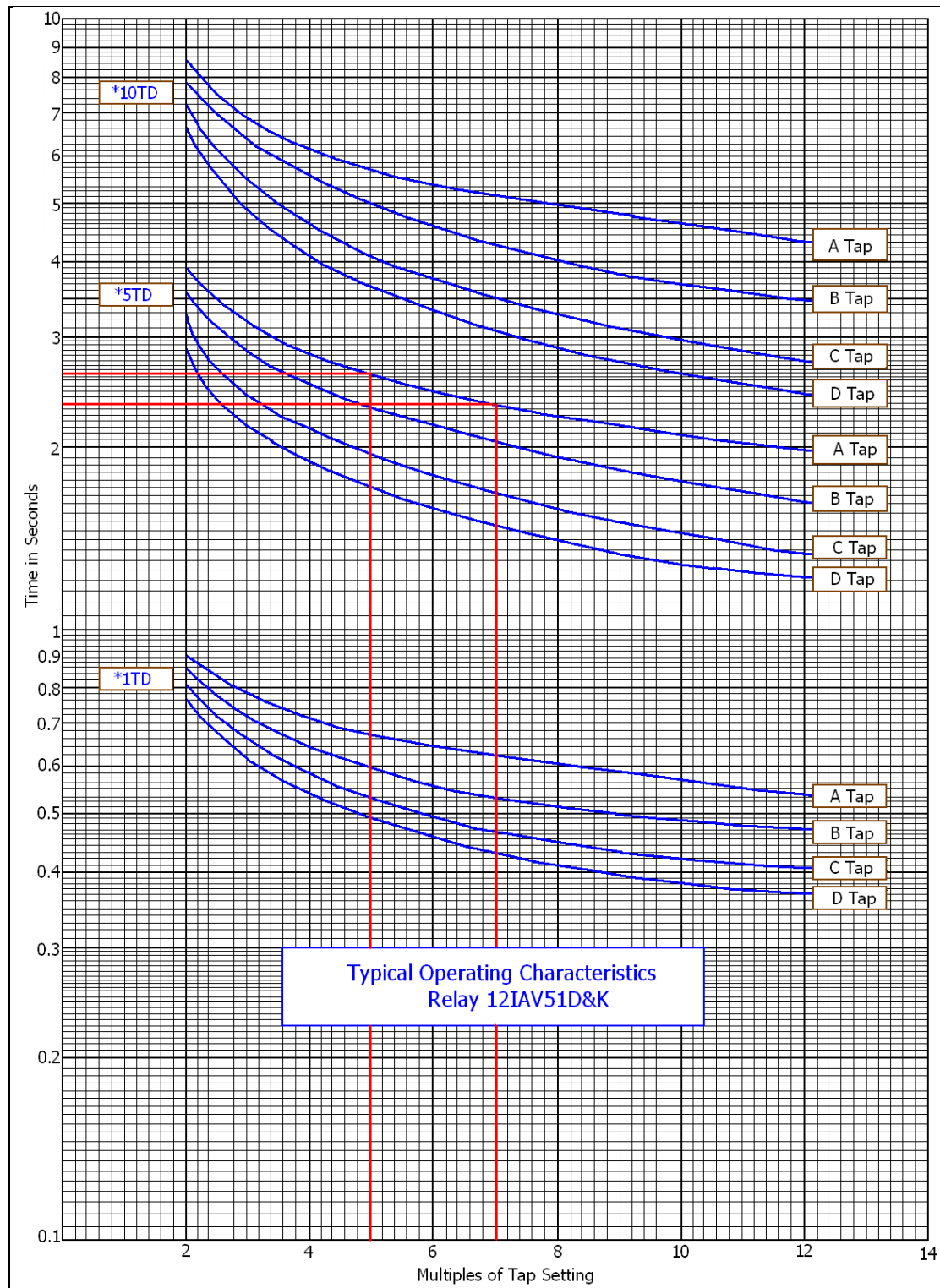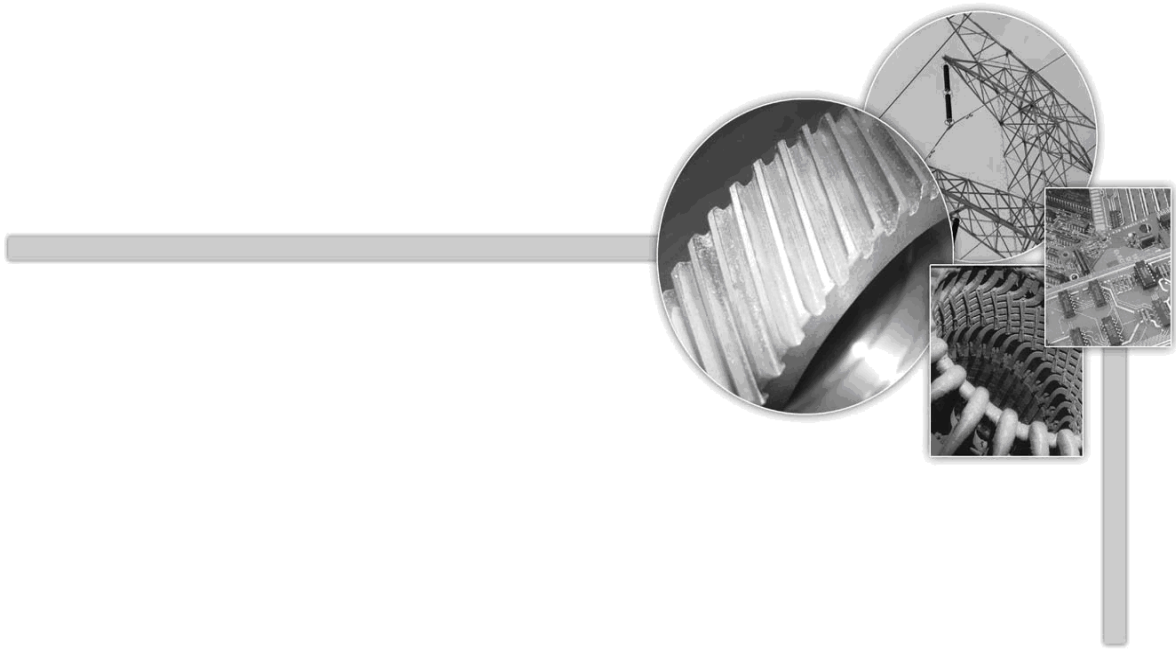
Fig. 1-4

4. Assume that earth fault results in a voltage that reaches 27V.

5. Calculate the multiple of tap setting = 27 /5.4 = 5

6. Adjust the tester voltage output at 27V.

7. Start voltage injection and note the recorded tripping time.

   Trip Time = ……………………………..Seconds

8. Use the relay characteristic curves in Fig. 1-4 to determine the trip time.

9. On the characteristic curves, select multiple of tap sitting at 5.

10. Go up until the intersection with (A) tap curve of 5TD group.

11. From the intersection go left to get the trip time.

12. Trip Time in this case = 2.6 Seconds

13. You should find the trip time on the characteristic curves agrees with the timer record, within ±15% error as per the relay manual.

14. Change the tester voltage output to 37.8V

15. Calculate the multiple of tap setting = 37.8 /5.4 = 7

16. Adjust the tester voltage output at 37.8V

17. Start voltage injection and note the recorded tripping timer

    Trip Time = ……………………………..Seconds

18. On the characteristic curves, select multiple of tap sitting at 7.

19. Go up until the intersection with (A) tap curve of 5TD group.

20. From the intersection go left to get the trip time.

21. Trip Time in this case = 2.3 Seconds

22. Return the voltage to zero and shutdown the power supply.

CONCLUSION

As the voltage increases from 27V to 37.5V, the trip time decreases from 2.6 seconds to 2.3 seconds,. According to the inverse characteristics between voltage value and its tipping time.

LESSON 1.4

DIRECTIONAL RELAY

LESSON 1.4

DIRECTIONAL RELAY

OVERVIEW

This lesson discusses the theory and applications of directional element in the overcurrent and earth fault protection. Directional element is represented as double input quantities, normally voltage and current. It discusses two types of electromechanical directional units, induction disc and induction cylinder directional units.

OBJECTIVES

Upon completion of this lesson, the trainee will be able to:

- Identify the importance of directional unit in the protection system.
- Describe the theory and operation of electromechanical directional relay.
- Demonstrate the connection and application of directional relay.
- Demonstrate the parts and connection of directional relay type IRD.

Task 1.4-1: Demonstration for directional overcurrent relay.

INTRODUCTION

Directional relay is an example for double input quantities -. The application of electromechanical induction disc unit protective relay gives improved performance characteristics for directional overcurrent, distance, reverse power, etc.

Directional relays are used to obtain directional sensitivity of the fault current to make appropriate decision about producing trip signal. For example, in the directional overcurrent relay, when the overcurrent unit senses fault, the relay operates according to the direction of current flow. For good selectivity, we often need the relay to operate for current flow in one direction only. This is achieved by fitting directional elements (device number 67) to the overcurrent relay, as shown in Fig. 1.4-1.
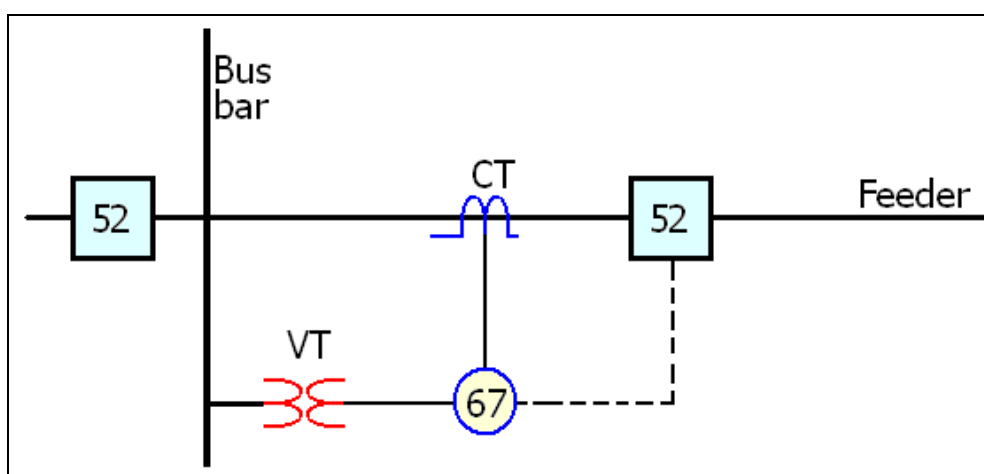
Fig. 1.4-1: Directional Overcurrent Relay

In the simple arrangement shown in Fig. 1.4-1, the directional element receives reference voltage from the VT and current is measured by the CT of the protected line. In normal operation, the phase angle of the current may be up to, say 20 degrees lag. However, if the direction of current flow reverses, then the phase angle will change by 180 degrees. This very large difference is easy for the relay to detect and activate the directional element.

The directional element controls tripping by superimposing its operation on that of the overcurrent relay. You remember that the time overcurrent relay is fitted with a shorted shading coil on one leg of the electromagnet. This is to provide the driving

force. In one method of directional control, the shorting coil is fitted with a contact, which is operated by the directional element. When current flow is in the **tripping** direction, this contact remains closed and the overcurrent relay can operate. However, if current flow reverses, then the directional element opens the contact, thereby preventing operation of the time overcurrent relay. Similarly, the directional element also operates a contact in the instantaneous relay tripping circuit to allow tripping only when current flow is in the designated tripping direction.

Directional relays are required for applications where it is desirable to allow tripping for current flow in only one direction, i.e., a directional power relay functions when the real power component (watts) flowing in a circuit exceeds a preset level in a specified direction.

APPLICATIONS OF DIRECTIONAL RELAY

1. **Source Power Flow Control:** On systems having in-plant generation operating in parallel with the utility supply, a reverse power relay sensing the incoming power from the utility can be set to detect when the generator begins to supply power to the utility and give alarm and trip to disconnect the utility link.

2. **Anti-motoring of Generators (Reverse Power):** This relay is used to detect the flow of power into a generator that has not been disconnected from the system with the turbine shutdown.

3. **Directional Overcurrent and earth fault Protection:** It is a combination of overcurrent unit and directional unit.

INDUCTION DISC DIRECTIONAL UNIT

The directional unit, as shown in Fig. 1.4-2, has two separate electromagnets. The upper electromagnetic core has winding on its middle limb, connected to the secondary of potential transformer P.T. The lower electromagnetic core has winding connected to the secondary of CT through tap block and plug bridge to control the

current coil. The developed torque on the disc is affected with the two electromagnets proportional to voltage, current and the angle between them.

Torque = K . V . I . Cos θ
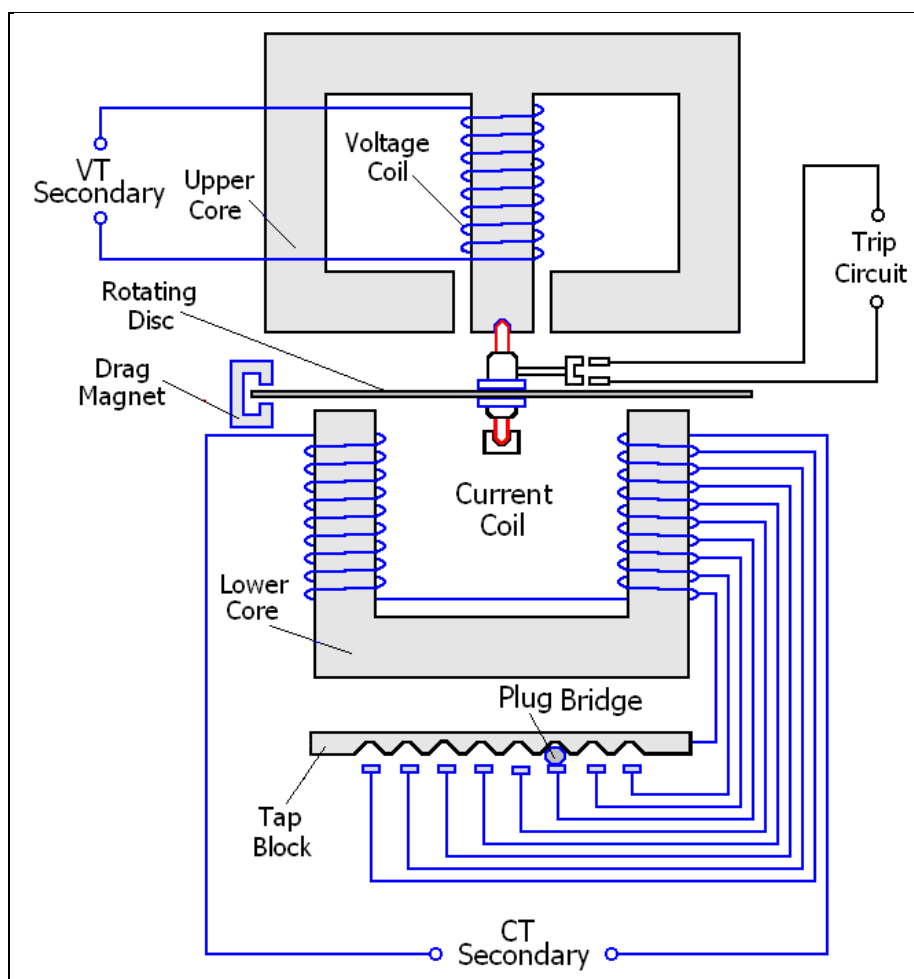
Fig. 1.4-2: Induction Disc Directional Unit (reverse Power Relay)

Since voltage is used to polarize the directional unit, its pick-up current is dependent on the magnitude of the voltage and the phase angle between the current and the voltage. The particular phase angle at which the pick-up current is at minimum is called the "angle of maximum torque."

When the power flows in the normal direction, the torque developed on the disc assisted by the spring tends to turn away the moving contact from the fixed trip circuit contacts. A reversal of current reverses the torque produced on the disc and when this is large enough to overcome the control spring torque, the disc rotates in the reverse

direction and the moving contact closes the trip circuit. The relay can be made very sensitive by having a very light control spring so that a very small reversal of power will cause the relay to operate.

Such relays are very suitable for protection of parallel feeders. When fault occurs on the feeder, voltage falls to a low value by which relay may become inoperative. This shortcoming may be overcome by compensating the relay secondary winding on the lower magnet. The compensating winding ampere-turns on the lower magnet opposes the ampere-turns produced by the current coil. Therefore, turns of current coil will have to be appropriately increased. When the voltage falls due to the fault, the resultant ampere-turns provided by the windings on the lower electro-magnet increase, compensating the reduced ampere-turns provided by the voltage coil.

DIRECTIONAL OVERCURRENT RELAY

Induction type directional overcurrent relay shown in Fig. 1.4-3 is a combination of non-directional overcurrent relay as that mentioned in the last lesson and the reverse power relay unit as that shown in Fig. 1.4-2, which has a current coil and voltage coil providing directional features to the relay.
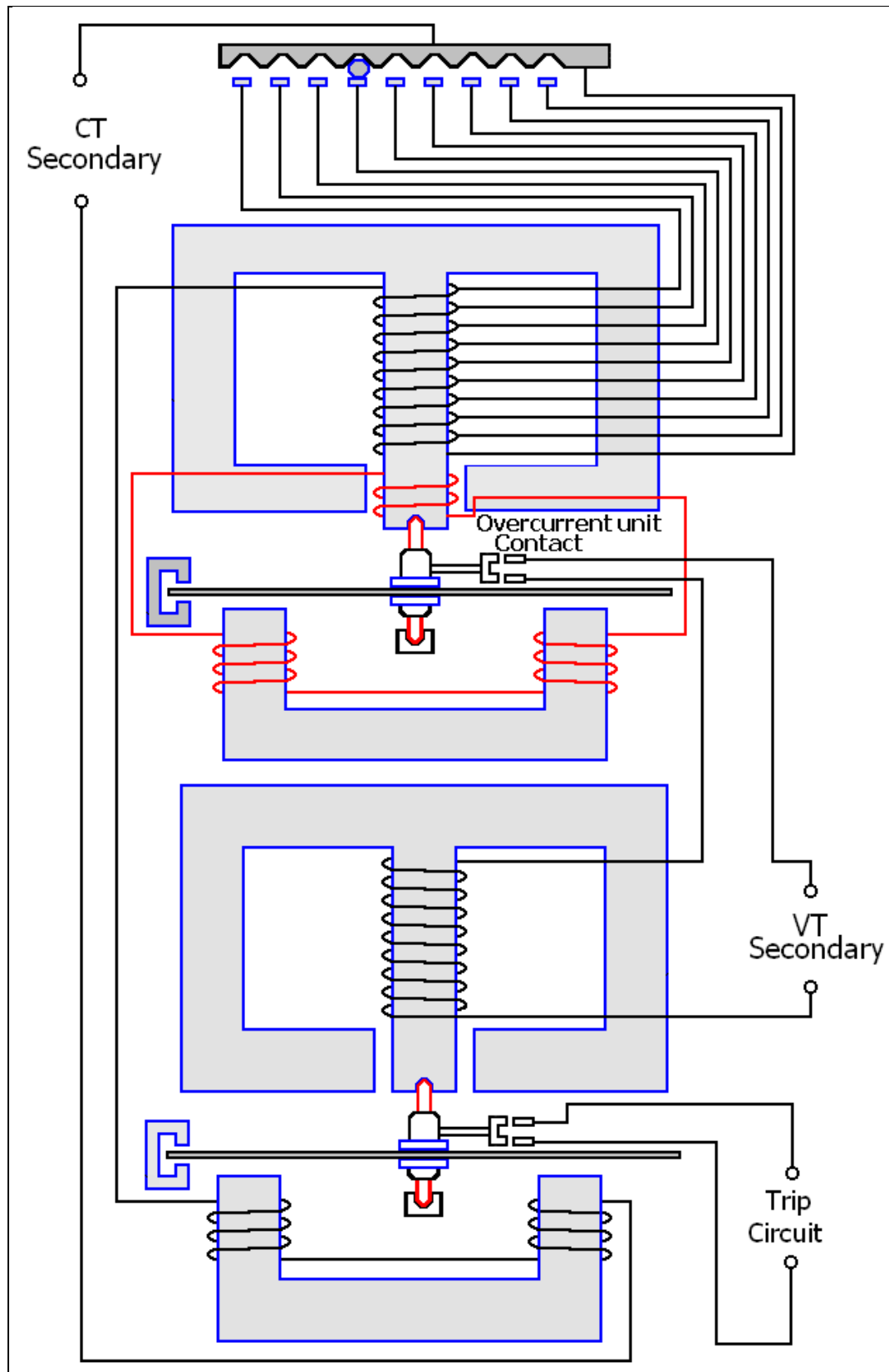
Fig. 1.4-3: Induction Type Directional Overcurrent Relay

As mentioned previously, in a two-element directional relay, one element operates on directional current, and the other on overcurrent. The contacts of the two elements may be connected in two different ways. In one case, each element operates independently and the contacts of the elements are connected in series as done for instantaneous overcurrent (Fig. 1.4-4). This is called directional supervision.
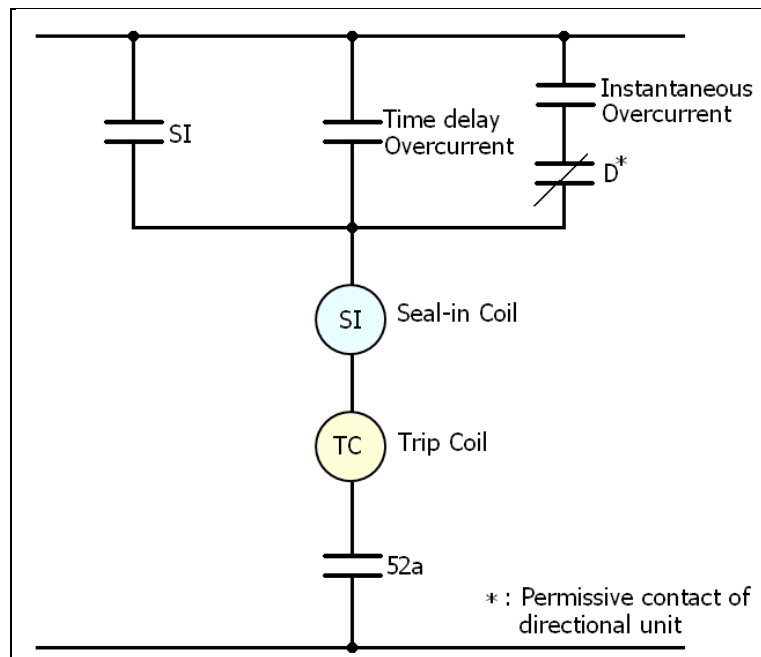
Fig. 1.4-4 Typical Tripping Circuit Directional Relay

In the other case, the contact of the directional element actuates the overcurrent element, and the contact of the latter is in the breaker trip circuit. With this second type of connection, the relay is known as a "directional controlled overcurrent relay" as shown in Fig. 1.4-5.

When the power flows in normal direction, the disc of the reverse power relay does not move. But as soon as there is a reversal of current, the disc starts rotating and completes the circuit for overcurrent or earth fault element. That permits this element operation and a torque is set up on the disc and the action closes the trip contacts, thereby enabling the circuit breaker to be tripped. The directional element is made as sensitive as possible to ensure positive operation - even 2% of the power in the reverse direction can operate it. A plug bridge is mounted to adjust the current setting.
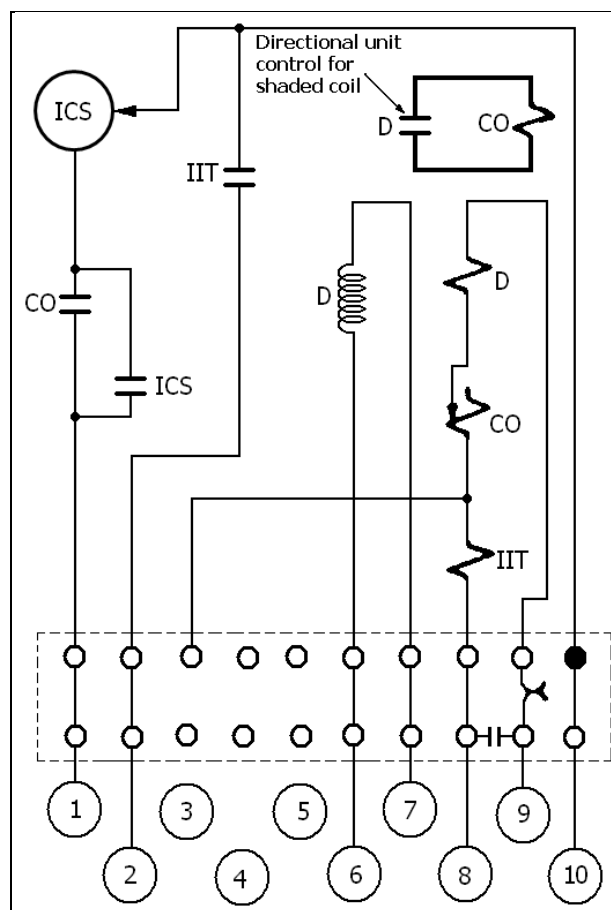
Fig. 1.4-5 Directional Unit Control for Shaded Coil

The directional overcurrent relay operates only when each of the following conditions is verified:

a.   The direction of current is in the selected direction.

b.   Current in the selected direction exceeds the pre-set value.

c.   Excessive current (greater than the pre-set value) persists for a duration longer than its time setting.

INDUCTION CUP (CYLINDER) DIRECTIONAL UNIT

Fig. 1.4-6 shows one common type of directional relay - the induction cylinder type. The aluminum or copper cylinder takes up a stationary position, depending upon the fluxes developed in the electromagnet. One of the coils receives input from the reference voltage or current, while the other is receiving input from the CT of the protected circuit.
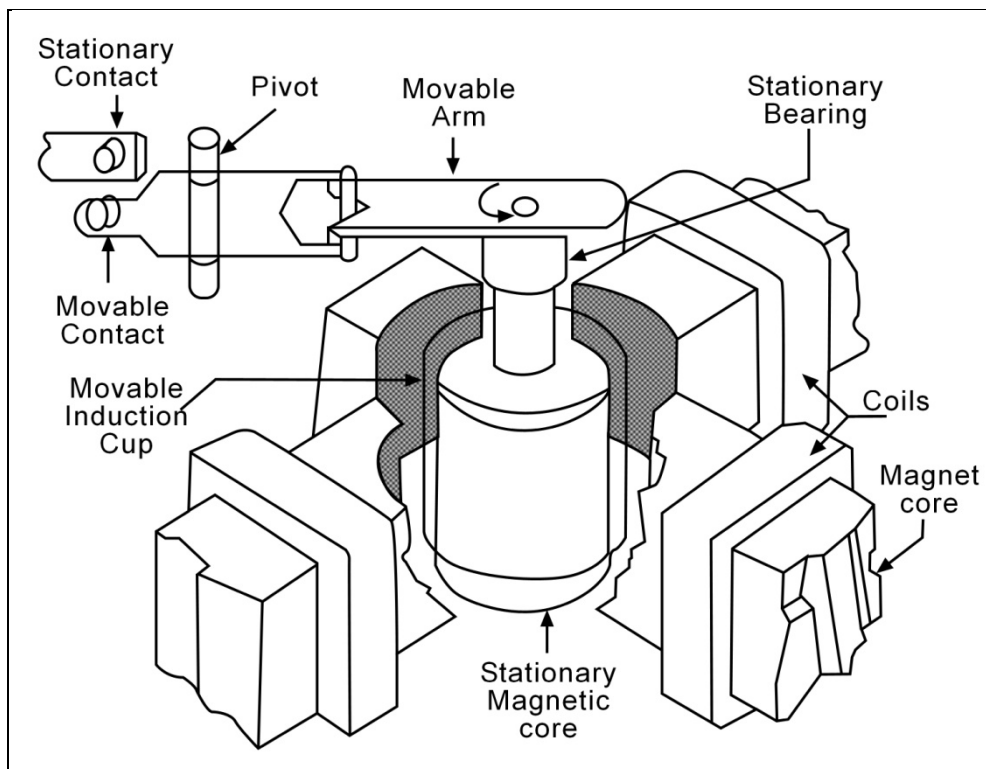
Fig. 1.4-6 Induction Cup Relay Element

When current flow is in the selected tripping direction, the two fluxes position the cylinder so that the contacts allow tripping. Now, if the flow of primary current reverses, then the aluminum cylinder immediately takes-up a new position and in this case the contact opens the shading coil circuit. This will prevent rotation of the time overcurrent disk and prevent the relay from undesired operation. It will also open the instantaneous relay tripping circuit.
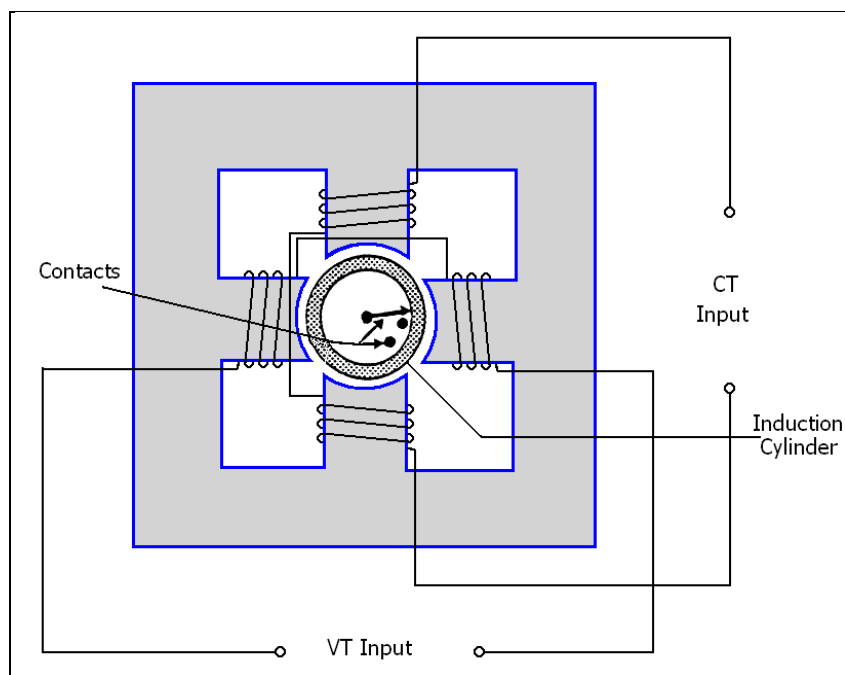
Fig. 1.4-7 Connection Diagram of Directional Relay Induction Cylinder Type

The actual tripping and blocking directions can be reversed by simply changing the polarity of one of the connections. Clearly, the directional element plays a very important role in coordination and selectivity of system protection schemes. Fig. 1.4-7 shows the connections of the induction cup unit.

EXAMPLES OF DIRECTIONAL RELAYS

Relays type IRD-9 (Westinghouse made) are ground directional overcurrent relays, used for the protection of transmission lines and feeder circuits. Both the time overcurrent and instantaneous overcurrent units are directionally controlled. The type IRD-9 relay is a dual polarized relay, which can be polarized from a potential source, from a local ground source or from both simultaneously.

1) Stationary Contacts

2) Stationary Contact-
Pressure Spring

3) Magnetic Adjusting Plugs

4) Upper Bearing Screw

5) Moving Contact

6) Spring Adjuster Clamp

7) Current Bias Vane
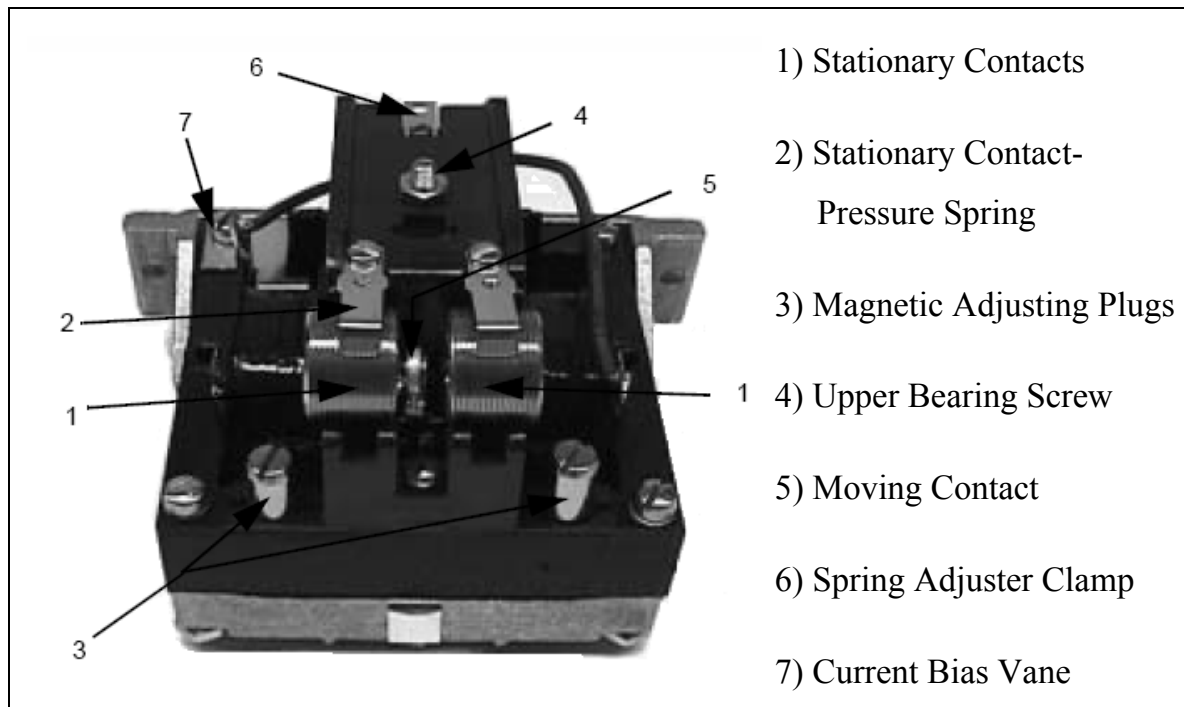
Fig. 1.4-8 Directional Unit

1) Tap Block

2) Time Dial

3) Control Spring Assembly

4) Disc

5) Stationary Contact Assembly

6) Magnetic Plugs

7) Permanent Magnet
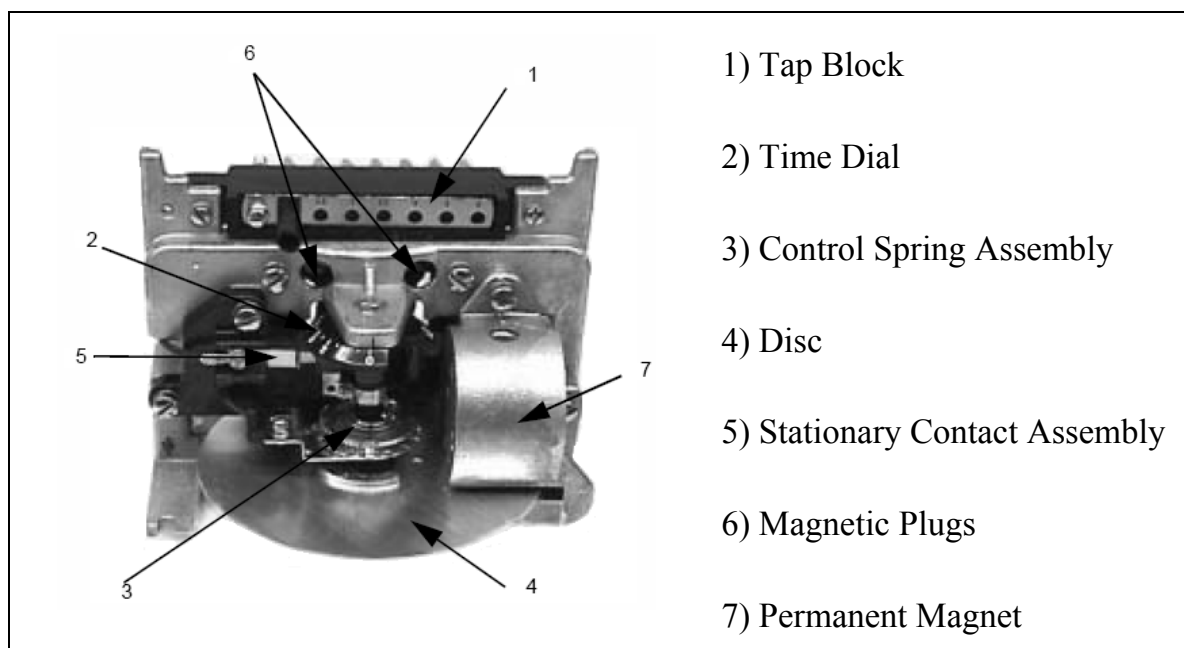
Fig. 1.4-9 Time Overcurrent Unit

(a) Front View	(b) Rear View
1-Instantaneous Overcurrent Unit	2- Current Polarized Directional Unit
3-Voltage Polarized Directional Unit.	4- Time Overcurrent Unit
5-Indicating Contactor Switches	6- Auxiliary Switch
7-Varistor	8- Saturating Transformer
9-"E" type Electromagnet	
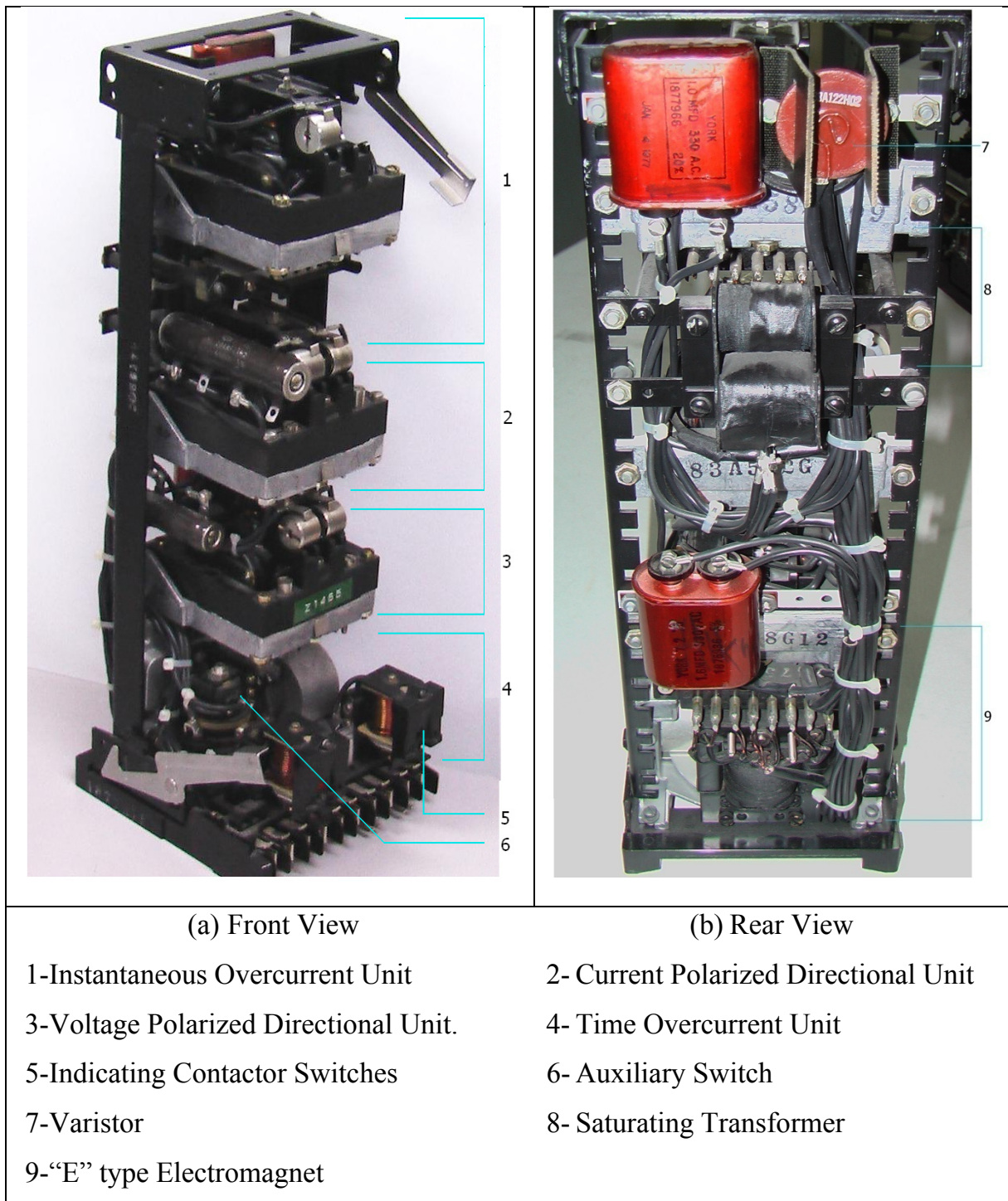
Fig. 1.4-10 Directional Relay Type IRD-9

The various types of relays consist of a directional units (D), an auxiliary switch (CS-1), a time-overcurrent unit (CO), an instantaneous overcurrent unit (I), an instantaneous overcurrent unit transformer, and two indicating contactor switches: ICS/I and ICS/T. The principal components of the relays and their locations are shown in Fig. 1.4-8 through Fig. 1.4-10.

TIME OVERCURRENT UNIT (CO)

Fig. 1.4-9 shows time overcurrent unit with **contactor indicating switch units** (ICS/I, ICS/T). Indicating contactor switch is clapper type device.

DIRECTIONAL UNIT (D)

The directional unit is a product of induction cylinder type unit operating on the interaction between the polarizing circuit flux and the operating circuit flux. Mechanically, the directional unit is composed of four basic components: A die-cast aluminum frame, an electromagnet, a moving element assembly, and a molded bridge.

AUXILIARY SWITCH (CS-1)

The auxiliary switch is a small solenoid type DC switch. A cylindrical plunger, with a silver disc mounted on its lower end, moves in the core of the solenoid. The operation of the CS-1 switch is controlled by the directional unit (D) which in turn directionally controls the time-overcurrent unit (CO). When sufficient power flows in the tripping direction, the CS-1 switch operates and bridges the lag coil of the time-overcurrent unit (CO) permitting this unit to operate.

INSTANTANEOUS OVERCURRENT UNIT (I)

The instantaneous overcurrent unit is similar in construction to the directional unit. The time phase relationship of the two air gap fluxes necessary for the development of torque is achieved by means of a capacitor connected in series with one pair of pole windings.

The normally closed contact of the directional unit is connected across one pair of pole windings of the instantaneous overcurrent unit as shown in the internal schematics. This arrangement short-circuits the operating current around the pole windings; preventing the instantaneous overcurrent unit from developing torque. If

the directional unit should pick up for a fault, this short circuit is removed, allowing the instantaneous overcurrent contact to commence closing almost simultaneously with the directional contact for high speed operation.

SATURATING TRANSFORMER

This transformer is of the saturating type for limiting the energy to the instantaneous overcurrent unit at higher values of fault current and to reduce CT burden.

CONNECTIONS

Fig. 1.4-11 shows the internal circuit and external connections of the IRD-9 relay for ground fault protection.
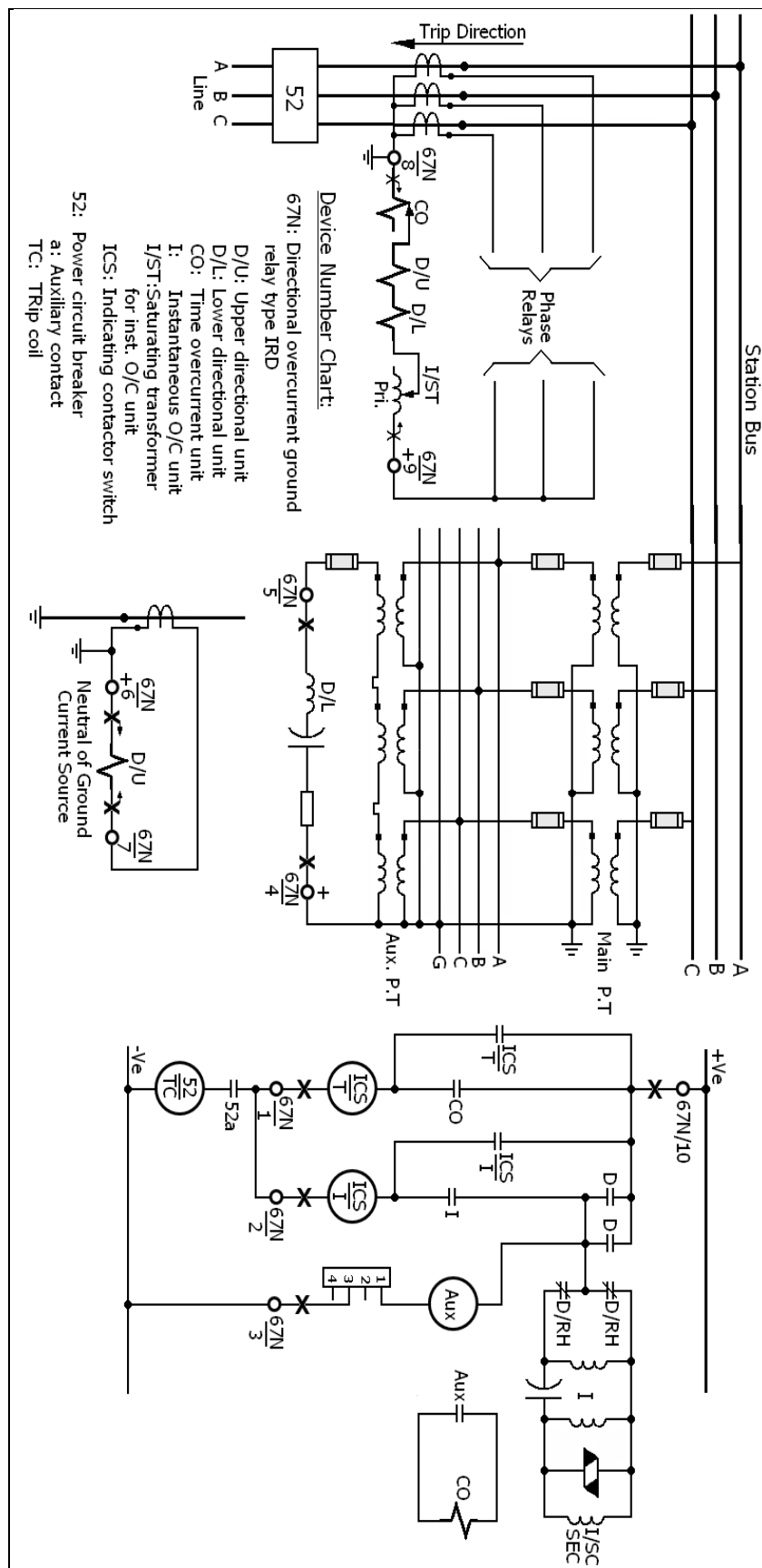
Fig. 1.4-11 External Schematic of the IRD Relay for Ground Fault Protection

SUMMARY

- Directional relay is a double input quantities, current and polarized voltage or current.

- Directional relay may take the form of induction disc or induction cylinder unit.

- The directional relay may be used in distance, and reverse power (anti-motoring) protection.

- Directional overcurrent relay has two series contacts, one of the overcurrent and the other of the directional unit.

- The pick up of the directional unit depends on the produced torque magnitude and angle to rotate the relay disc or the relay cup.

FORMULAE

Torque $T = K \cdot V \cdot I \cdot \cos \theta$

    V = reference polarized voltage from VT

    I = Current from CT

    K = constant

    θ = the angle between V & I

REVIEW EXERCISE

Circle the letter a, b, c or d that correctly completes the statement:

1. Directional units are used ……………………………………………
    a. For protection by themselves only.
    b. With O/C relays.
    c. With impedance distance relays.
    d. All of the above.

2. The directional unit is ……………………………………………….
    a. Voltage polarized.
    b. Current polarized.
    c. Both (a) and/ or (b).
    d. Neither (a) nor (b).

3. Directional time O/C relay will operate in case of ……………..
    a. The direction of current is in predetermined direction.
    b. The current in the selected direction exceeds the present value.
    c. Excessive current (greater than the pre-set value) persists for a duration as per time settings.
    d. All of the above.

4. When directional elements are included in a relay, the directional contacts will close when:
    a. Current in the directional element coil exceeds a minimum value.
    b. Power flow is in the predetermined direction.
    c. Potential is removed from the directional element.
    d. None of the above.

5. The directional overcurrent relay is reliable to protect ………………………
    a. Radial systems.

    b. Ring systems.

    c. Both (a) and (b).

    d. Neither (a) nor (b).

6. For the directional unit of relay IRD, match the names with the numbers on the drawing shown below:

- Current Polarized Directional Unit

- Voltage Polarized Directional Unit

- Instantaneous Overcurrent Unit and Saturating Transformer

- Time Overcurrent Unit

- Auxiliary Switch

- Indicating Contactor Switches
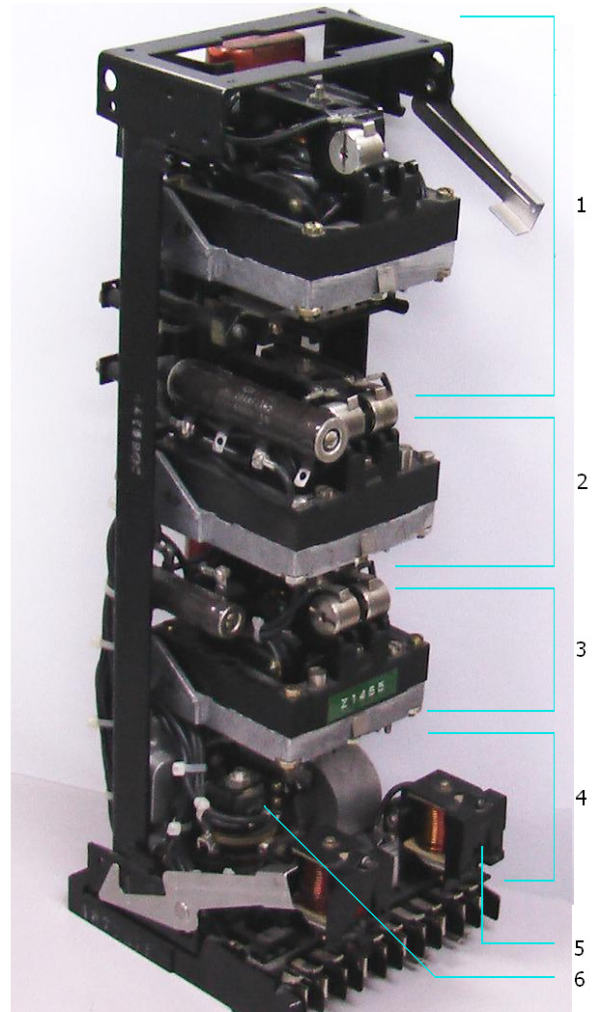
Fig. 1.4-12

7. For the time O/C unit in relay IRD-9, match the names with the numbers on the drawing shown below:

- Time Dial

- Magnetic Plugs

- Disc

- Permanent Magnet

- Tap Block

- Control Spring

- Stationary Contact
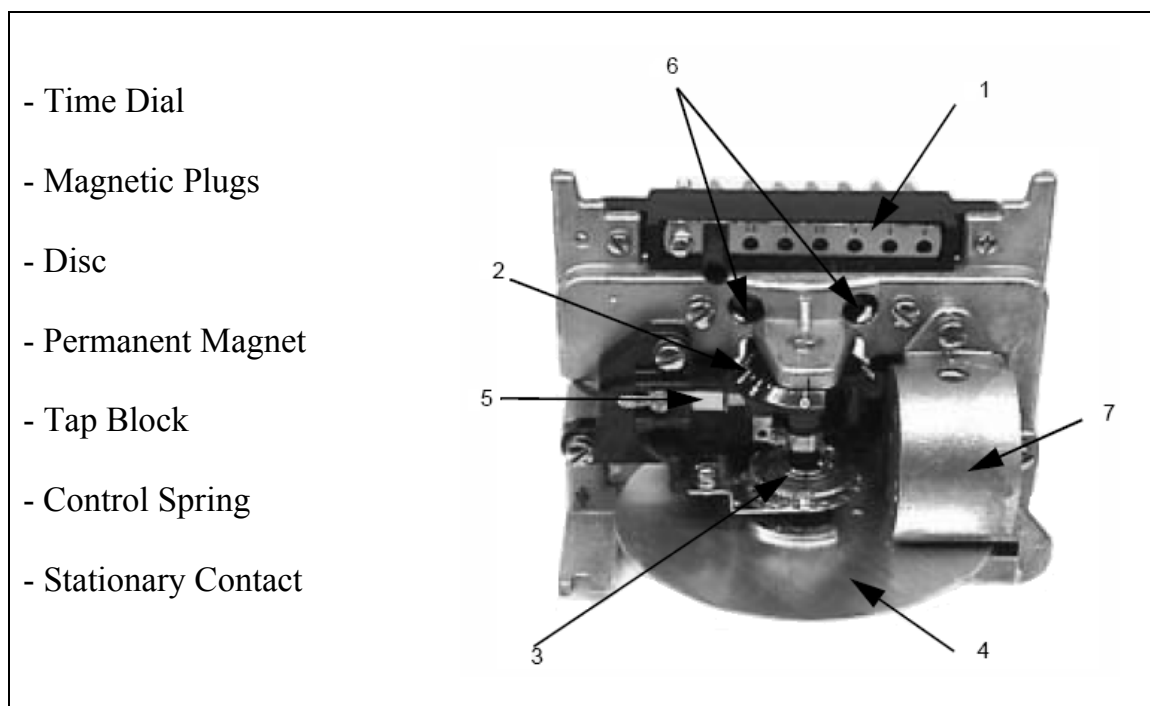
Fig. 1.4-13

8. Study the control circuit diagram of Fig. 1.4-14 and match the following:

(a)   Overcurrent contact

(b)   Seal in relay

(c)   Circuit   breaker   auxiliary   contact.

(d)   Trip coil.

(e)   Directional contact.
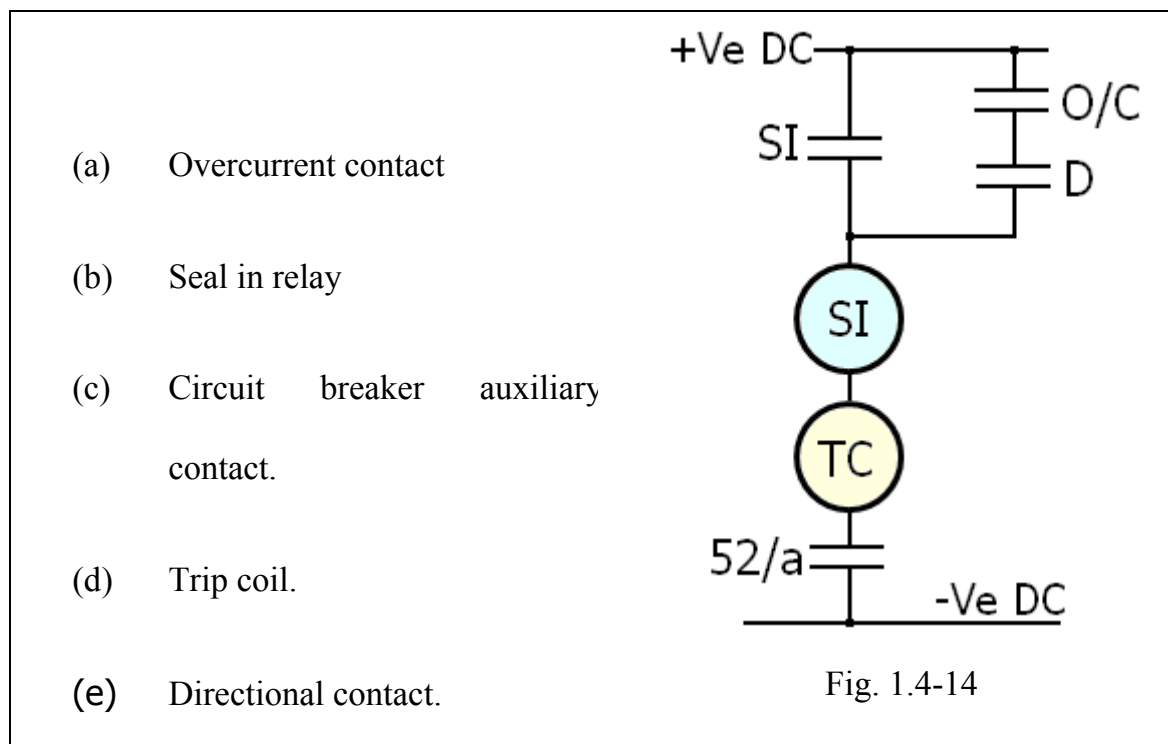
Fig. 1.4-14

9. Add a timer to the circuit in the suitable location.

10. Study the circuit shown in Fig. 1.4-15 and answer the following:
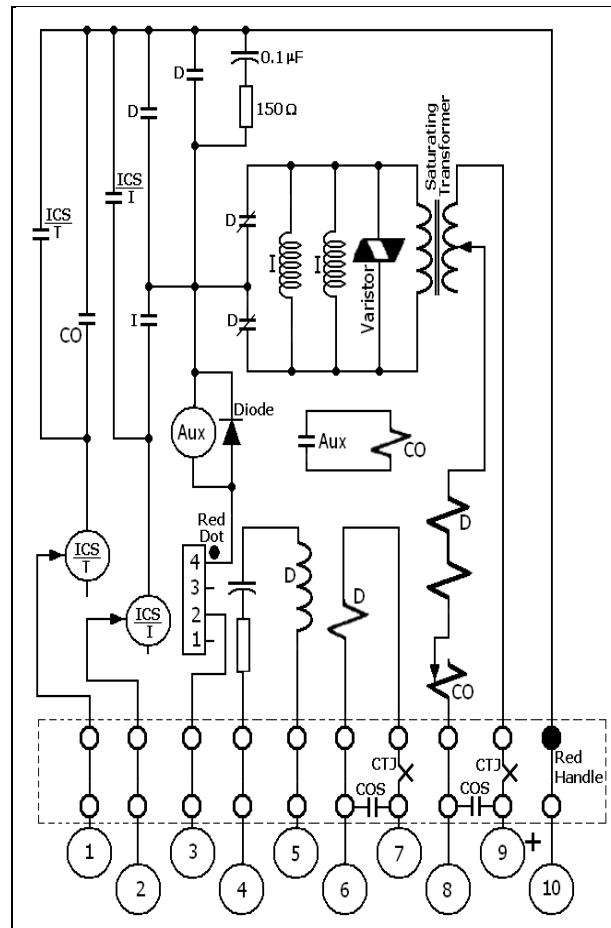
Fig. 1.4-15

a) Identify the current terminals, and voltage terminals.

b) What is the purpose of chassis operated switches and red handle?

c) What is meant by the (+) mark?

d) What is the purpose of the varistor?

Task 1.4-1

DEMONSTRATION FOR DIRECTIONAL O/C RELAY

OBJECTIVES

Upon completion of this task, the participants will be able to:

- Demonstrate and describe the relay parts.

TOOLS, EQUIPMENT & REQUIREMENTS

- Electromagnetic directional overcurrent relay (IRD-9 type).
- instruction manual of the relay
- Personal safety equipment as recommended in relay workshop.

PROCEDURE

1. Read the relay nameplate carefully to know the specifications.
2. Identify and inspect instantaneous O/C unit and saturating transformer.
3. Identify and inspect the directional unit for the following items:
- stationary contacts
- stationary contacts pressure spring
- magnetic adjusting plugs
- upper bearing screw
- moving contact and cylinder condition
- spring adjuster clamp
4. Identify and inspect time overcurrent unit for the following items:
- tap block
- time dial
- control spring assembly
- disc

- stationary contact assembly

- magnetic plugs

- permanent magnet

5. Identify and inspect indicating contactor switch.
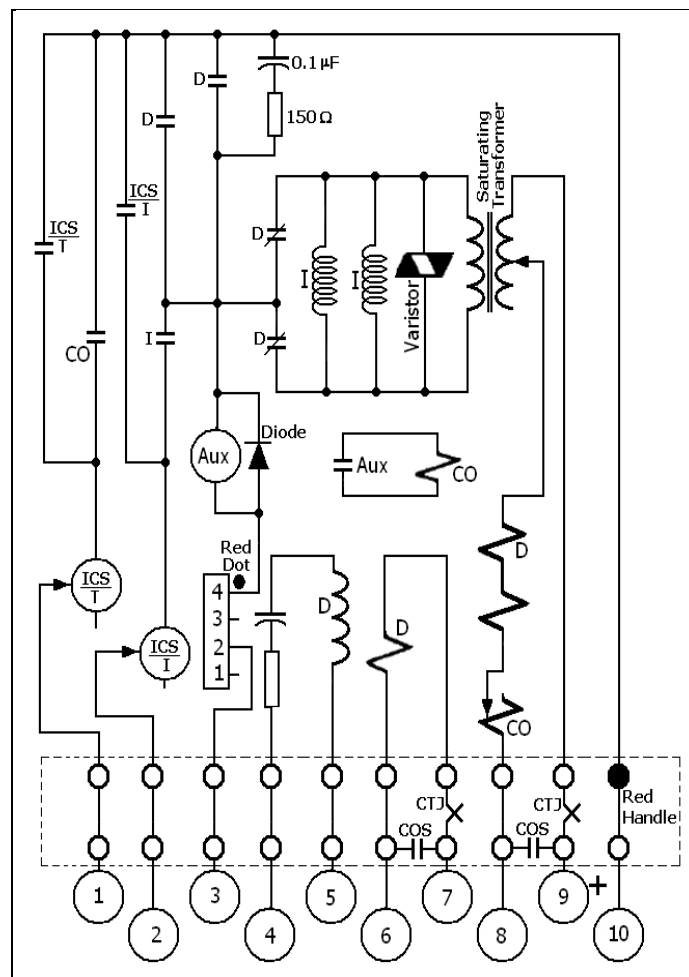
Fig. 1-1 Directional Relay IRD-9 Connection Diagram

ICS /T: Indicating contactor switch for time delayed unit (right front view)

ICS /I: Indicating contactor switch for instantaneous unit (left front view)

Aux: Auxiliary switch (CS-1 or TR-1)

D: Directional unit

I: Instantaneous overcurrent unit

CTJ: Current test jack

CO: Indicating unit

Varistor: Electronic component for protection against surges

COS: Chassis operated shorting switch
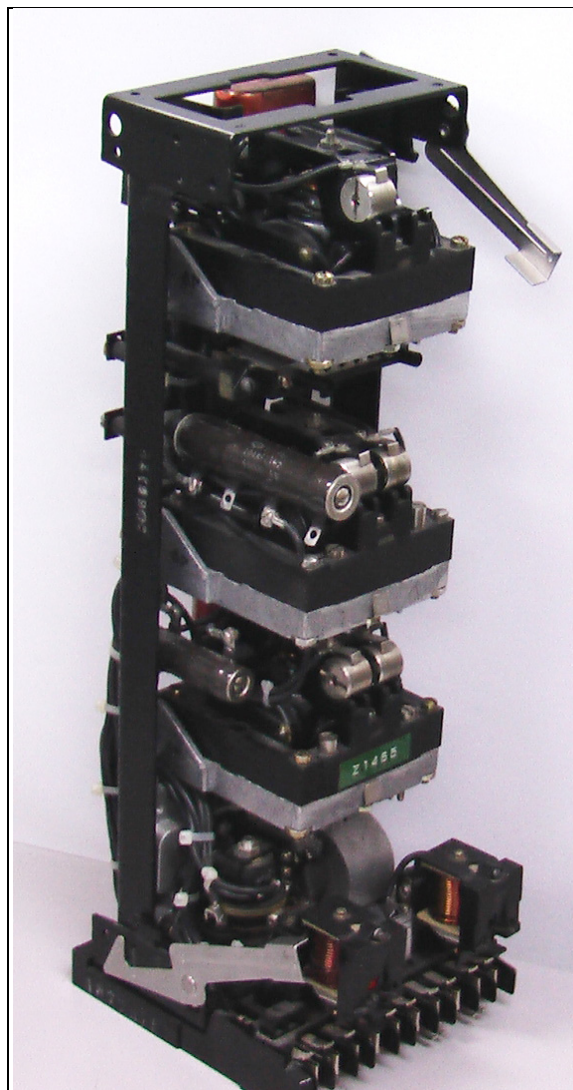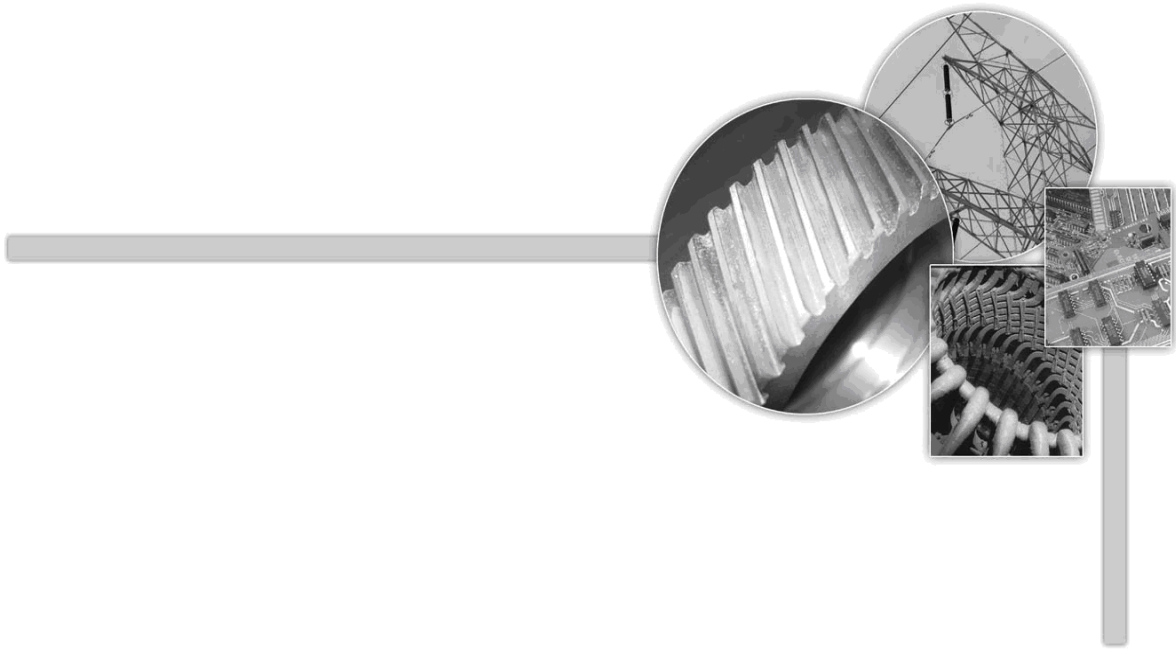
Fig. 1-2 Directional Relay IRD-9 Front View

LESSON 1.5

FREQUENCY RELAY

LESSON 1.5
FREQUENCY RELAY

OVERVIEW

This lesson discusses the deviations of the power system frequency, due to large change in loads that are unacceptable for the network and the response of frequency relays to keep system frequency stable.

OBJECTIVES

Upon completion of this lesson, the trainee will be able to:

1. Describe the effect of low frequency on the system, generators and turbines.
2. Describe the function of frequency relays and load shedding.
3. Describe the construction of induction disc frequency relays.
4. Describe the construction of induction cup frequency relays.
5. State applications of under/over frequency relays.

Task 1.5-1: Demonstration and operation of induction cup frequency relay.

INTRODUCTION

Frequency protective relays are important to protect electrical machines and plants/substations against adverse effects in the event of deviations in the rated speed of generators (e.g. vibration, heating, etc.), this protection detects and records frequency fluctuations in the power system, and disconnects certain loads according to the thresholds set. It can also be used for the purposes of system decoupling, and thus improves the availability of in-plant power generation.

The frequency protection function is implemented via voltage input V. From the sampled voltage, the frequency is measured after various filter functions. Some frequency relays operate over a wide frequency range (25-70 Hz). And implemented optionally for over frequency or under frequency on a multi stage basis; each stage can be individually delayed. The frequency stages can be blocked either via the binary input (in case of static or numerical relays) or by an under voltage stage.

OVER FREQUENCY

Over frequency results from the excess generation and it can easily be corrected by reduction in the prime mover power output with the help of the governor or manual control.

UNDER FREQUENCY

Under frequency occurs due to overload, or decrease in generation under the load requirements. The power system survives only if we drop the excess loads so that the generator output becomes equal to or slightly greater than the connected load. If the load increases beyond the generated power, the frequency will drop and load need to be shed down to restore the balance between the generation and the connected load. The rate at which frequency drops, depends on the time, amount of overload and on the load and generation variations as the frequency changes. Frequency decay occurs within seconds so it is impossible to be corrected manually. Therefore automatic load

shedding feature needs to be applied. These schemes drop loads in steps as the frequency drops. Generally load shedding drops 20 to 50% of load in four to seven frequency steps. Load shedding scheme trips the substation feeders (or even the whole substation) to decrease the system load. Generally, automatic load shedding schemes maintain the balance between the load connected and the generation.

The present practice is to use the under frequency relays at various load points so as to drop the load in steps until frequency returns to normal. Non-essential load is removed first when reduction in frequency occurs. The setting of the under frequency relays is based on the most probable condition depending upon the worst-case possibilities. During the overload conditions, load shedding must occur before the operation of the unit (turbine-generator) under frequency relays. In other words, load must be shed before the generators trip or turbines shutdown.

FREQUENCY RELAYS

A frequency relay is a device that functions on a predetermined frequency setting - either under or over normal system frequency or rate of change of frequency. When it is used to function on a predetermined value below nominal frequency, it is generally called an under-frequency relay, and when it functions on a predetermined value above nominal, it is called an over-frequency relay. Both functions are often included in the same case, but are utilized for different purposes.

EFFECT OF LOW FREQUENCY AND LOAD SHEDDING

When the load of power system suddenly exceeds the available generating capacity, load shedding is needed otherwise the generators begin to slow down as they attempt to drive the excessive load. As the speed slows down, the frequency decreases below normal (60 Hz) and the system voltage decreases.

Further, the drop in frequency may endanger generation itself. The thermal generating plant is quite sensitive to even 5% frequency reduction. The output of power plants depends on motor driven auxiliaries. As system frequency decreases, the power output

of the auxiliaries begins to fall off rather rapidly and this in turn further reduces the energy input to the turbine - generator. The situation thus has a cascading effect, with a loss of frequency leading to a loss of power, which can cause the frequency to deteriorate further and the entire plant may soon face a serious trouble.

OVER & UNDER FREQUENCY EFFECTS ON GENERATORS

Over frequency is less of concern than under frequency for a generator because an over frequency condition results from excess generation. It can be corrected by a reduction in power output via the governor or manual controls. Increased shaft speed during an over frequency event will improve cooling, thus increasing generator load-carrying capabilities.

- One concern is that the 105% limit on terminal voltages could be exceeded.
- The terminal voltage of a generator operating under control of the manual regulator would raise proportional to frequency.
- Under frequency is caused by excess load and cannot be corrected locally.
- The speed reduction reduces generator ventilation and with it load-carrying capability.
- Typically, generators can operate down to 95% rated speed for hours if the output voltage is reduced proportional to speed and terminal voltage is limited to rated to avoid over-excitation.
- From 95 to 90% rated speed, both output voltage and current should be reduced in proportion to speed, thus reducing output capability by the square of the speed reduction.

LOW FREQUENCY EFFECTS ON STEAM TURBINE

Steam turbines are more adversely affected by off-frequency operation than are the generators they drive. A key feature of turbine blade design is assuring that the blades are not damaged by mechanical resonance. Mechanical resonance produces

high vibratory stress that can cause fatigue cracking and eventual blade failure. Resonance occurs when a natural frequency of a blade coincides with vibration.

Each turbine blade has natural frequencies that vary with the physical dimension of the blade. Short blades in the high pressure and intermediate pressure stages of the turbine can be designed to withstand a resonance condition. This is not practical for the long thin blades in the last few rows of the low pressure stage. These low-pressure-stage blades determine the turbine ability to fall in off frequency operation.

The manufacturer of specific turbine must provide short time limits for over or under frequency operation.

An example of limitation for one manufacturer is shown in table 1.5-1

% CHANGE IN FREQUENCY	FREQUENCY RANGE IN Hz	EFFECT ON THE BLADE
1%	59.4 – 60.6	No adverse effect on blade life
2%	58.8 – 61.2	Potential damage in about 90 min
3%	58.2 – 61.8	Potential damage in about 10 to 15 min.
4%	57.6 – 62.4	Potential damage in about 1min.
5%	57 - 63	Damage could occur within few seconds.

Table 1.5-1

These withstand limits are not typical; limits vary dramatically among manufacturers. Fatigue damage is cumulative. Blade vibration is a concern when the turbine is under load not during startup or shutdown. The minimum load at which steam flow is sufficient to cause damage is usually around 5%.

There are three correcting factors for the frequency deterioration:

- Spending the restored energy in the rotating parts (inertia) but it is not enough.

- Governor operation but it cannot immediately correct the situation due to its slow mechanical response.

- Load shedding.

It is obvious that the only way to save a system from complete collapse in such circumstances is to shed load to restore the balance between load and generation. Load shedding is performed by frequency relays. Frequency relays for this application must be independent of the voltage and be very accurate.

It is highly desirable to apply under-frequency relays whenever the loads are supplied either exclusively by local generators or by a combination of local generation and utility tie, as shown in Fig. 1.5-1.
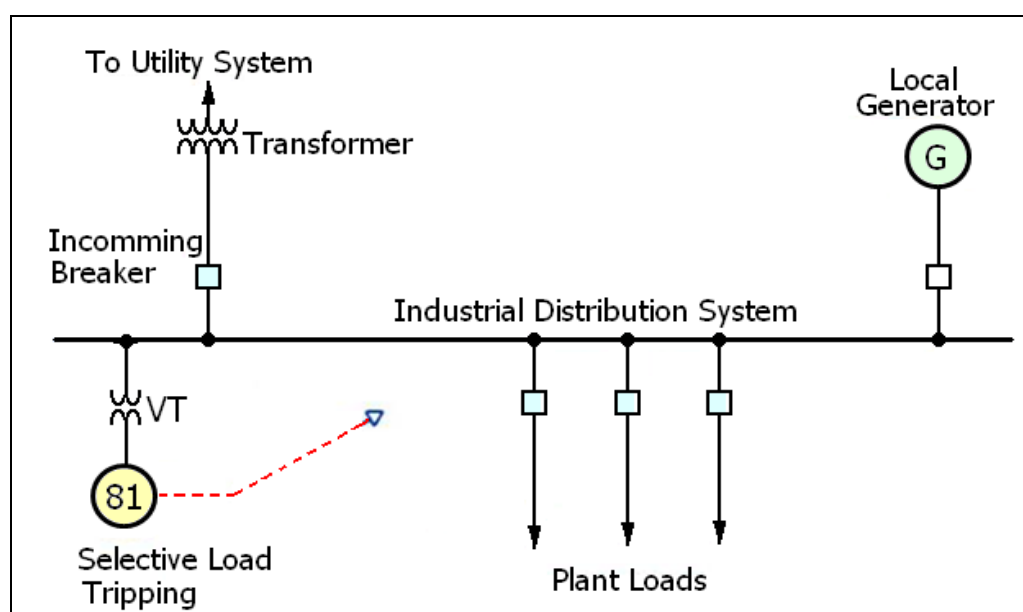
Fig. 1.5-1 Frequency Relay Connection in the Power System

When a major generator drops off line unexpectedly in a system, supplied only by local generation, the under-frequency relay(s) automatically open(s) plant load breaker(s) so the load matches, or is less than, the remaining generation. Otherwise, moderate-to-severe overloads on the remaining generator(s) could force the plant into a blackout before the operator can react. When the utility disconnects a plant system that has local generation (Fig. 1.5-1), the under-frequency relay(s) automatically open(s) plant load breaker(s) so the load matches, or is less than, the local generation. The under-frequency relay operates at a specific (preset) frequency below nominal to trip off a predetermined amount of load so the most critical load will remain running with the available generation. More than one under-frequency relay may be used to permit a number of steps of load shedding, depending on the severity of the overload.

For instance, X% of the load may be removed at 59.5 Hz, Y% of the load removed at 59 Hz, and Z% of the load removed at 58.5 Hz for a three-step load shedding scheme. The number of load shedding steps, the amount of load shed at each step, and the frequency settings for each step should be determined by a systems study.

In addition, it is necessary to assign a priority to each load, so the load will be removed on a priority basis, with the lowest priority loads being removed first.

OVER FREQUENCY

Over-frequency relays are often applied to generating units. These relays protect against over-speed during start-up or when the unit is suddenly separated from the system with little or no load. Relay contacts sound either an alarm or shutdown the unit (turbine- generator).

EXAMPLE FOR APPLYING FREQUENCY RELAY

Load shedding is performed in up to seven stages as per table 1.5-2:

Stage Number	Frequency Operation Hz
1st stage	59.6
2nd stage	59.57
3rd stage	59.50
4th stage	59.3
5th stage	59.1
6th stage	58.9
7th stage	58.7

Table 1.5-2

There are a BSP in AL-HASSA area called South Hofuf, it feeds five stations called Hamidiah, Khaladiyah, Jishah, Rawdah, and Idwa as shown in Fig. 1.5-2.
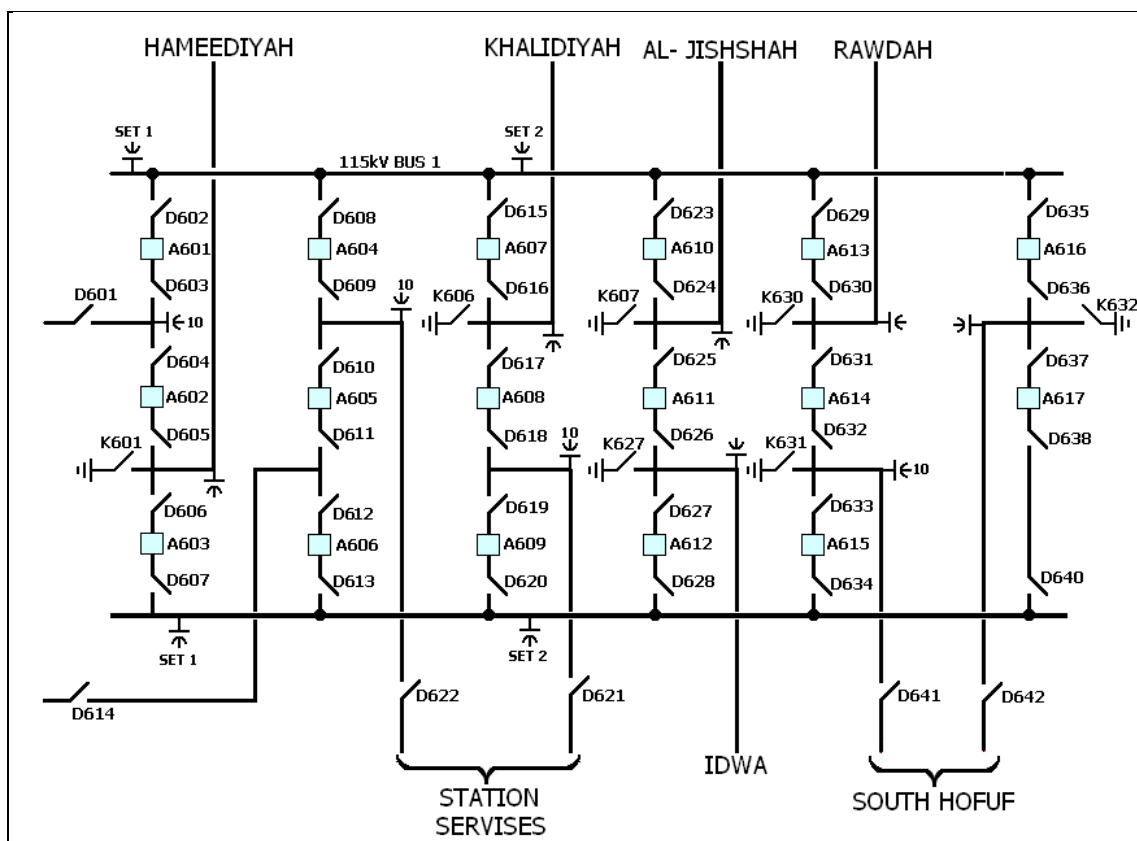
Fig. 1.5-2 Single Line Diagram for S. Hofuf BSP

These stations are disconnected according to the setting table 1.5-3.

	AREA	SETTING	ACTION
S. Hofuf	IDWA	58.9 HZ	A611 & A612
	RAWDAH	58.9 HZ	A613 & A614
	HAMEEDIYAH	**58.7 HZ**	**A602 & A603**
	JISHAH	59.1 HZ	A610 & A611
	KHALADIYAH	58.9 HZ	A607 & A608

Table 1.5-3

The load shedding of the five substations, IDWA, RAWDAH, HAMIDIAH, JISHAH and KHALADIYAH is performed at frequency setting of 58.9, 58.9, 58.7, 59.1 & 59.9Hz respectively as indicated in the table.

Note that each substation should be completely disconnected from any feed at the same preset frequency as in S. HOFUF. For example, Hameediah is fed from two stations S. Hofuf and Abu Ghanumah as shown in Fig. 1.5-3 Abu Ghanumah substation is fed from S. Hofuf and Mahasen PSP as shown in Fig. 1.5-4. So Abu Ghanumah should be shed from Mahasen PSP at the same frequency (58.7 HZ) as per Table 1.5-4.

	AREA	SETTING	ACTION
MAHASEN. BSP	MUTAIRIFI LINE	58.9 Hz	A616 & A617
	HAJER LINE	58.9 Hz	A617 & A618
	NEW SANG LINE-1	58.7 Hz	A605 & A606
	HASSA COMM. LINE	58.7 Hz	A611 & A612
	ABU GHANIMAH LINE	**58.7 Hz**	**A619 & A620**
	NEW SANG LINE-2	58.7 Hz	A601 & A602
	NUZHA LINE	58.9 Hz	A607 & A608
	H.H.O SHIP LINE	58.9 Hz	A613 & A614

Table 1.5-4
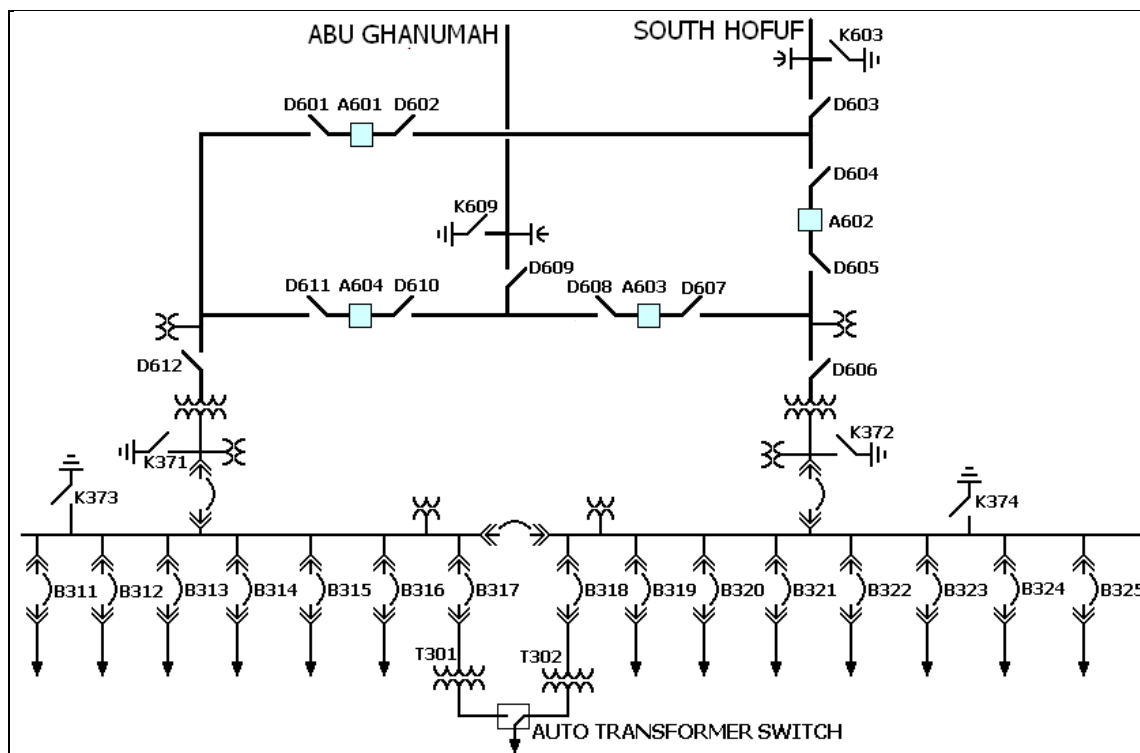
Fig. 1.5-3 Single Line Diagram for Hameediah Substation
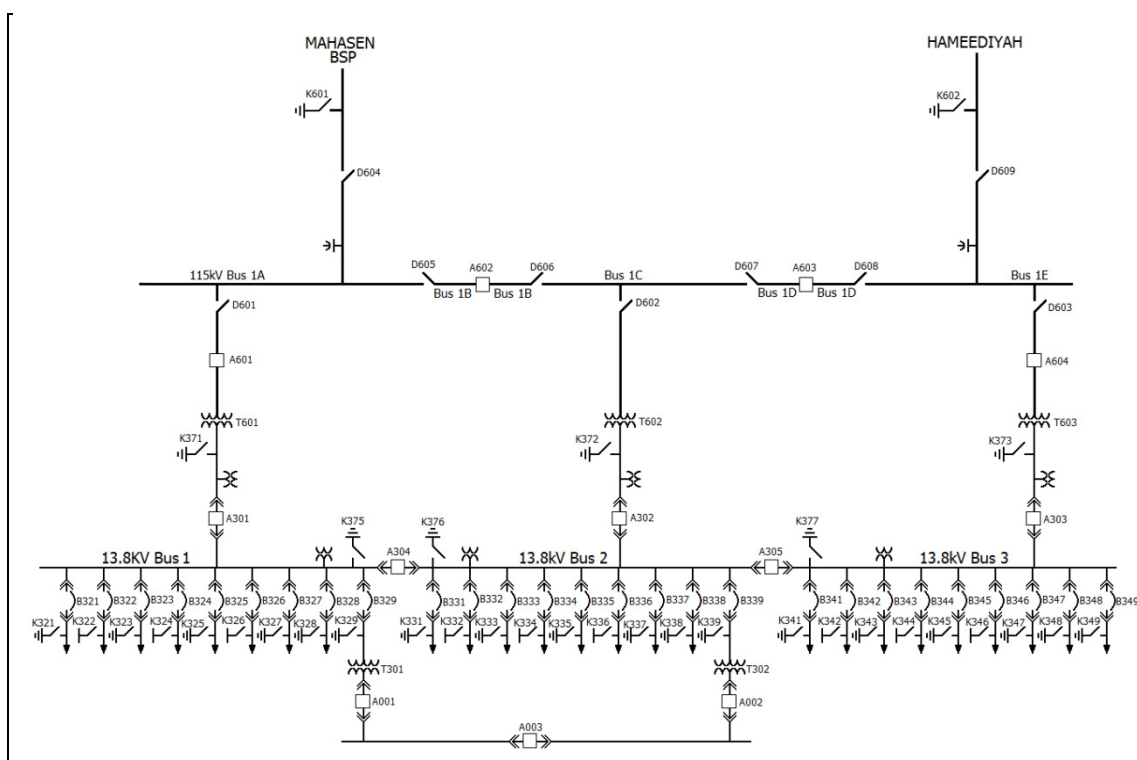
Fig. 1.5-4 Single Line Diagram for Abu Ghanimah Substation

If the load shedding program could not restore the frequency and the frequency deteriorates and reaches 57 Hz, an under frequency relay will shutdown the unit to protect turbine as discussed before.

CONSTRUCTION OF FREQUENCY RELAYS

Different types of frequency relays according to design are available as follows:

- Electromagnetic frequency relays, they may be induction disc or induction cup (cylinder) relay unit.
- Static frequency relays.
- Numerical frequency relays.

INDUCTION DISC FREQUENCY RELAY

The induction disk relay is subjected to two AC fluxes whose phase relationship changes with frequency to produce contact opening torque above the frequency setting and closing torque below it.

A time-dial is used to adjust the initial contact separation that determines the operating time for a given applied frequency. The greater the rate at which the frequency drops, the faster the relay operates for a given time dial setting. The induction disk under-frequency relay is accurate to within 0.1-02 Hz and is designed for applications where high tripping speed is not essential.

The relay operating mechanism consists of a two-pole electromagnetic driving element, and an operating disc fitted with trip contacts. One of the electromagnet poles is located above the operating disc and the other pole below the disc. A spiral control spring, mounted on the operating disc shaft, acts to hold the disc and trip contacts fully open when the relay is de-energized.

When an out-of-tolerance frequency condition occurs, the fluxes produced by the upper and lower poles of the driving elements are shifted out-of-phase inducing a driving torque on the operating disc. This driving torque causes the operating disc to rotate in a direction to close the trip circuit contacts.

The out-of-phase fluxes between the upper and lower poles are the result of an internal capacitor connected in series with the lower pole. An adjustable resistor is connected in series with the pole that does not have the capacitor for adjusting minimum operating frequency.

Operating principle of the relay is based on the angular displacement of the lines of flux produced by the upper and lower electromagnet poles. A shift in phase angle of current in one pole with respect to current in the other pole is the result of a capacitor wired in series with one of the poles. The capacitor will cause the angular displacement of the fluxes to vary as system frequency changes. This out-of-phase flux condition causes a driving torque on the relay operating disc to either open or close the trip circuit contacts.

INDUCTION CUP UNDER FREQUENCY RELAY

Induction cup is more accurate and faster than the induction disk model. The operating principle is the same as the induction disk relay. Two AC fluxes, whose phase relationship changes with frequency, produce contact-closing torque in the cup unit when the frequency drops below the setting.

The under-frequency relay (using induction cup) has eight potential coils acting on an induction cup. The coils are connected in two groups of four coils in series, E_1 and E_2 as shown in Fig. 1.5-5. Coils E_1 passes current I_1 through capacitor (C), and coils E_2 passes current I_2 through adjustable resistor R. The coils are designed so that current I_1 lags current I_2 at the normal frequency of 60 cycles, and the fluxes of the two currents produce a torque that keeps contact (81/b) closed.
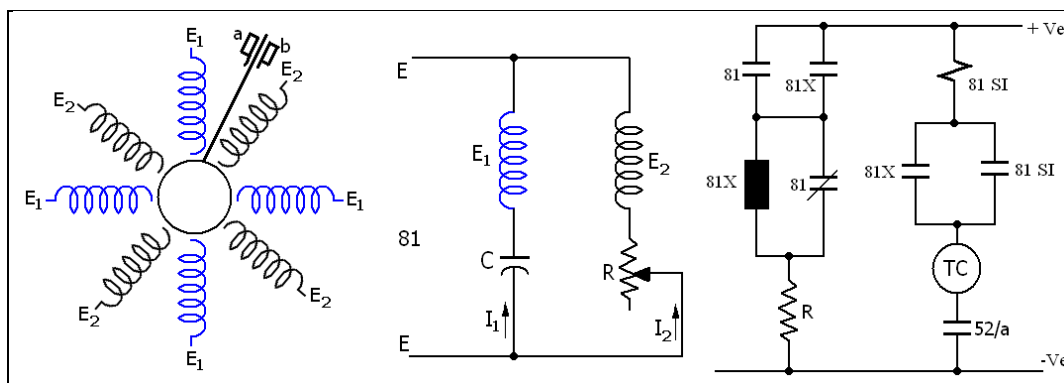
Fig. 1.5-5 Under-Frequency Relay Control Circuits

81/a: NO contact closes when frequency relay operates.

81X coil: Auxiliary relay energizes when 81/a contact closes and 81/b opens.

81/SI: Seal-In unit

81X NO contact: operates to self hold the relay signal

81/b: NC contact opens when frequency relay energizes.

When the frequency decreases, the phase-angle of Current (I_1) shifts clockwise at a greater rate than the phase-angle of Current I_2. If the decrease in frequency is enough to make current (I_1) lead current (I_2), there will be a torque reversal of the induction cup, and the (81/a) contact closes, as shown in Fig. 1.5-6.

Auxiliary relay (81X) introduces a time delay of about six cycles. The contacts have a fixed initial separation; the greater the rate of frequency declines, the faster the contacts close. The contacts may close in as little as 6 cycles after application of the under-frequency potential. Because phase shifts in the AC potential supply due to faults or fault clearing may cause incorrect operation, at least 6 cycles intentional delay should be added before tripping. The frequency accuracy of this type of relay is about $\pm$ 0.1 Hz.
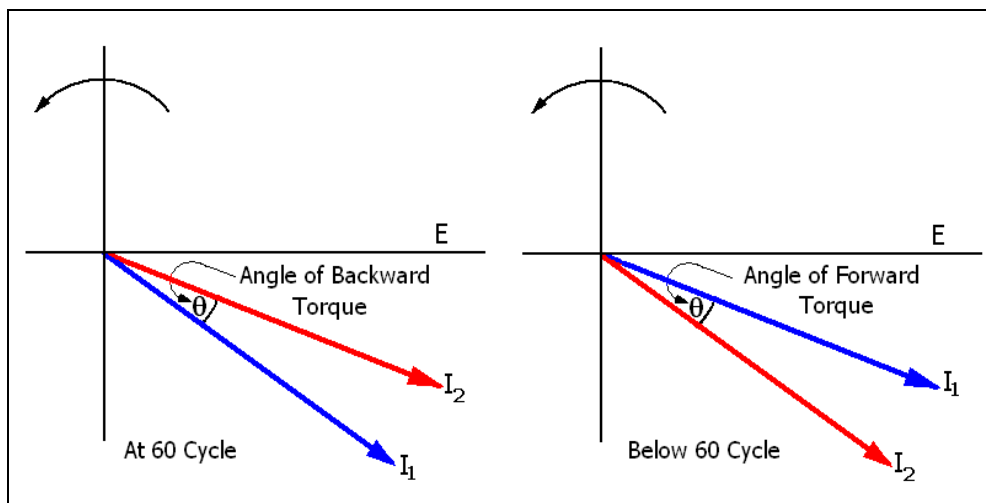
Fig. 1.5-6 Relations of Current Vectors

SUMMARY

- Over frequency occurs due to excess in generation over the load requirements.
- The solution for the over frequency is to decrease the generation power to be equal or slightly more than loads.
- Under frequency occurs when the generation power is insufficient to meet load requirements.
- The solution for under frequency is to shed the loads in steps.
- Frequency relay is fed from voltage transformer.
- The relay operation depends on the produced torque in the induction cup unit due to the shift between two fluxes.
- Capacitor C is used to produce shift in current due to change in frequency.

GLOSSARY

Load shedding: Load disconnecting.

Worst case: Maximum undesired scenario

Generation balance: Generation power is equal to the load requirements

Generation capability: The ability to feed any load size at any time

BSP: Bulk Supply Point

REVIEW EXERCISE

Circle the letter a, b, c or d that correctly completes the statement:

1.   Frequency relay always needs:

   a) Only one VT   b) Three CTs & three VTs

   c) Three CTs   d) Three VTs

2.   The frequency relay device function number is:

   a) 21   b) 81

   c) 68   d) 51

3.   The output of under frequency relay may:

   a) Trip the generator   b) Activate the back-up protection

   c) Enter the shunt reactors   d) Make load shedding

4.   The over frequency results when:

   a) The   loads   greater   than   b) Sudden   outage   of   the   loads
      generated power   occurs

   c) A ground fault occurs   d) Voltage drop due to a leak in the
                                                   excitation current occurs

5.   The under frequency results when:

   a) The loads are greater than   b) Sudden outage to loads
      generated power

   c) A ground fault occurrence   d) Voltage drop due to a leak in the
                                                   excitation current

6.   The electromagnetic frequency relay may use ………… type unit:

   a) Plunger   b) Induction disc

   c) Clapper   d) Balanced beam

7.   Answer True or False:

   a) Load shedding is performed when frequency changes either say from 60 H$_Z$ to 60.3 H$_Z$ or, from 60 H$_Z$ to 59.2 H$_Z$

   b) Load shedding is urgent when the generated reactive power becomes more than the load requirements

   c) Load shedding relay is an under frequency one

   d) Load shedding relay trips the assigned feeder CB's one after another separated with definite time grading

8.   For the circuit shown in Fig. 1.5-7, what is the purpose of the break contact of **81** in parallel with **81X** coil?
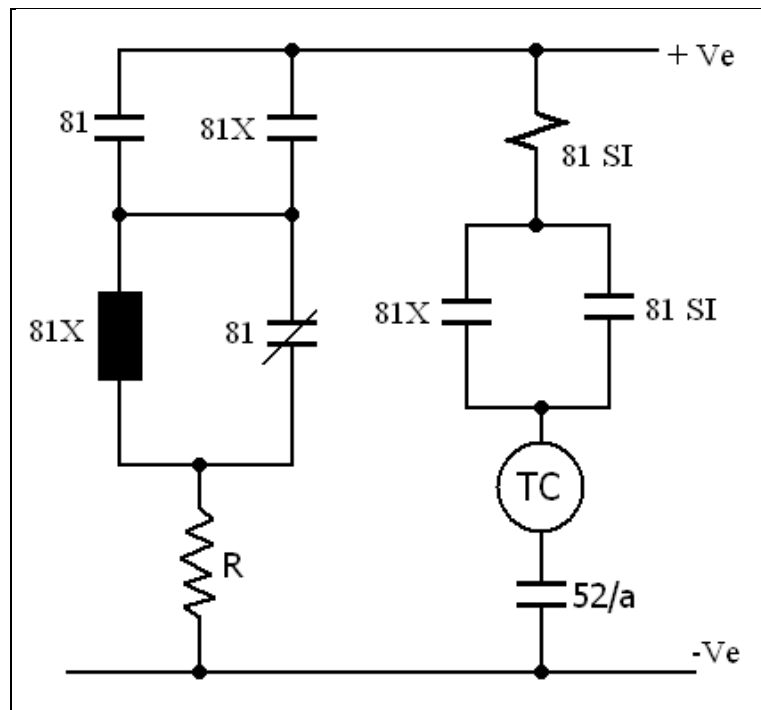
Fig. 1.5-7

9.   The function of resistor R in Fig. 1.5-8 is to:

   a) Protect the trip coil

   b) Prevent short circuit when contact 81 is closed

   c) Protection for 81X coil

   d) Protection for seal-in unit

For the under frequency relay AC circuit shown in Fig. 1.5-8, answer the following questions:
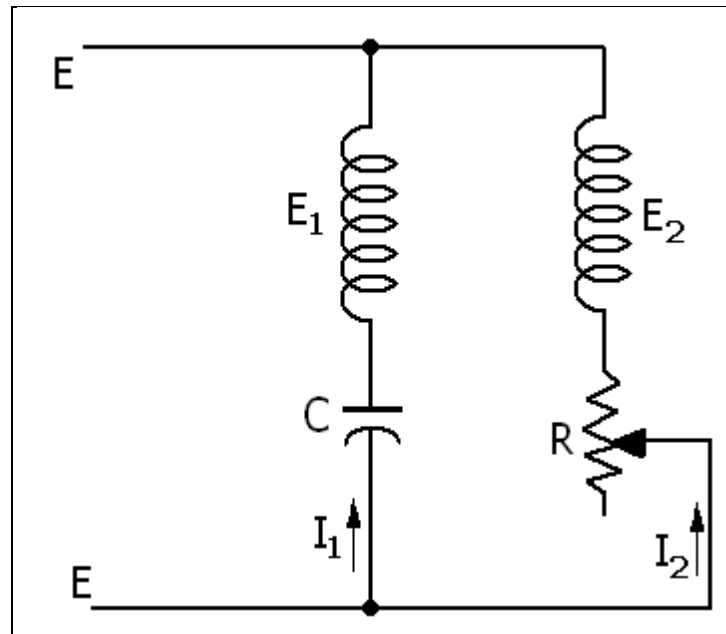
Fig. 1.5-8

10. What is the function of capacitor C?

   a) Let I_1 lead I_2 at 60 Hz   b) Let I_1 lag I_2 at 60 Hz

   c) Let I_1 lead I_2 at low frequency   d) Let I_1 lag I_2 at low frequency

11. What does feed (E-E) terminals?

   e) DC source   f) Current transformer

   g) Voltage transformer   h) Auxiliary contact of CB

12. What is the effect of varying the resistor R?

   a) Change the over frequency setting   b) For adjusting minimum operating frequency

   c) Change the relay time delay   d) Change Phase angle between I_1, I_2

13. At under frequency condition, I_1 (lead / Lag) I_2

TASK 1.5-1

IDENTIFICATION AND OPERATION TEST FOR FREQUENCY RELAY TYPE FM2

OBJECTIVES

Upon completion of this task, the participants will be able to:

1.   Identify the frequency relay type Fm2.

2.   Read the relay setting and Perform the pick-up test for the frequency relay.

TOOLS, EQUIPMENT & REQUIREMENTS

-    Electromagnetic frequency relay (Fm2 type).

-    instruction manual of the relay.

-    Frequency test set.

▪   Personal safety equipment as recommended in relay workshop.

PROCEDURE FOR OBJECTIVE 1

1. Read the relay nameplate carefully to know the specifications of the relay.

2. Identify and inspect the frequency relay for the following items as in the manual:

- Contact bar

- Tension spring

- Moving contact

- Contact pressure spring

- Fixed contact

- Seal in unit

- Auxiliary relay timer adjustment

- DC terminals

- AC voltage terminals

3. Read the circuit diagram of the frequency relay (Fig. 1-1) and determine the DC terminals & AC voltage terminals.
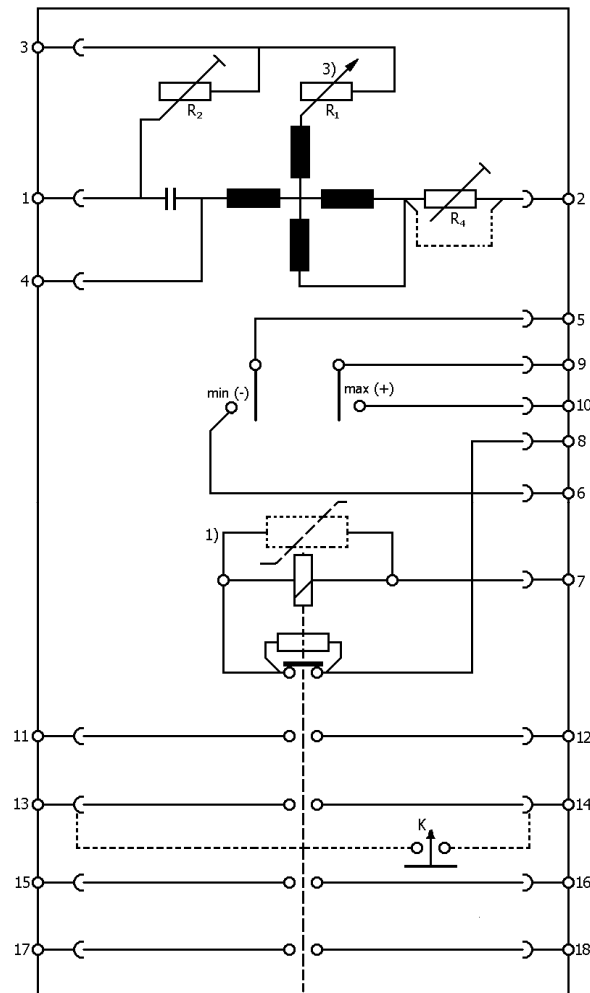
Fig. 1-1 Internal Circuit and Terminal Diagram

PROCEDURE FOR OBJECTIVE 2

1. Be familiar with the frequency test set controls.
2. Connect the frequency test set to the relay as shown in Fig. 1-2.
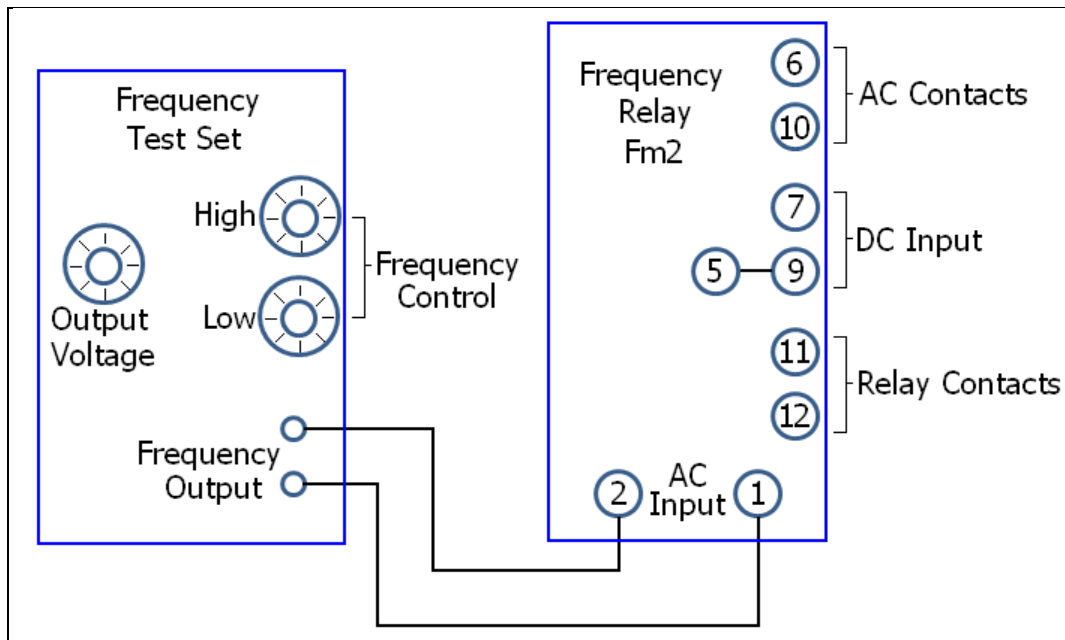
Fig. 1-2 Connection between Frequency Relay and Frequency Test Set

3. Suppose the required over and under frequency settings are 61.5 & 58.5Hz respectively

4. Adjust the base setting as 60Hz.

5. Adjust the relay setting to 2.5% for both over and under.

6. Calculate the operating frequencies for over and under cases as follows:

   Over frequency operating point = 60 + (2.5 x 60) / 100 = 61.5Hz

   Under frequency operating point = 60 - (2.5 x 60) / 100 = 58.5Hz

7. For under frequency test, gradually decrease the frequency output until the relay operates (the moving contact moves to the left).

8. Compare the pick-up value of the under frequency with the required setting in step 3, they should be equal.

9. Gradually increase the frequency output until the over frequency operates (the moving contact moves to the right).

10. Compare the pick-up value of the over frequency with the required setting in step 3, they should be equal.
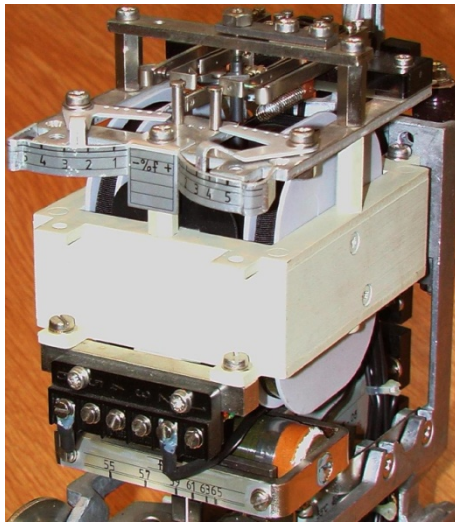
Fig. 1-3 Front View for
Frequency Relay type Fm2

Fig. 1-4 Frequency Test Set
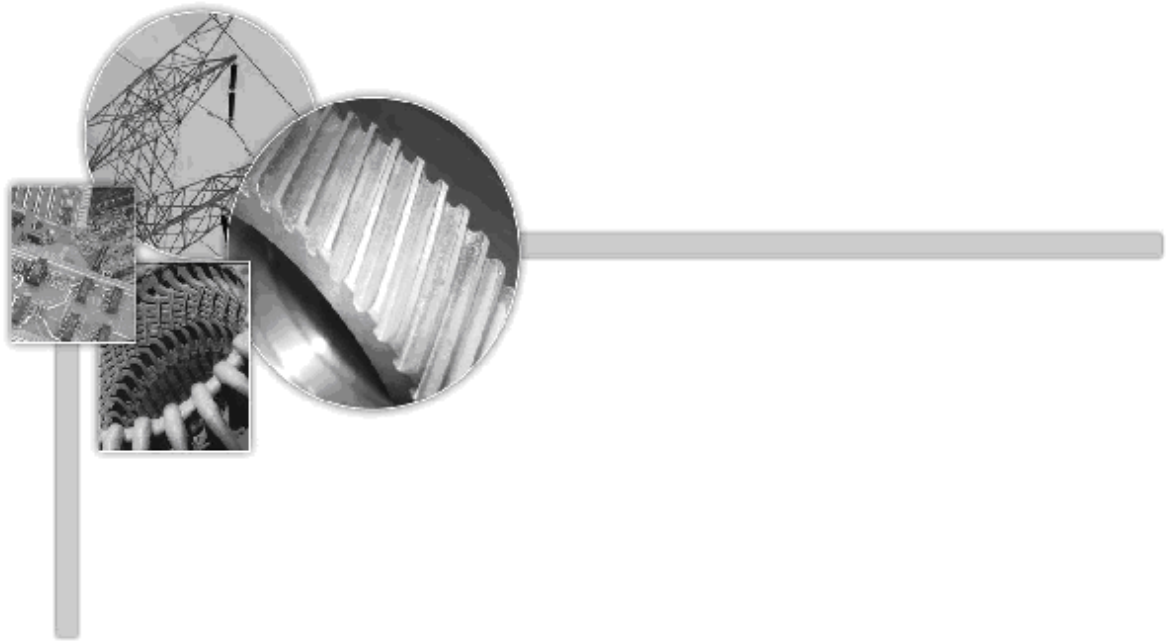
UNIT 2

TYPES OF MAIN PROTECTION SCHEMES

UNIT 2

TYPES OF MAIN PROTECTION SCHEMES

OVERVIEW

In this unit, the trainees learn about the main protection schemes for different system equipment, such as differential, distance, out-of-step, and breaker failure.

OBJECTIVES

Upon completion of this unit, the trainees will be able to:

- Identify the differential protection scheme.

- Demonstrate the distance protection scheme.

- Illustrate the breaker failure protection.

- Demonstrate the out-of-step relaying.

LESSON 2.1

DIFFERENTIAL PROTECTION

LESSON 2.2

DIFFERENTIAL PROTECTION

OVERVIEW

Differential relay is used as the main protection for power system equipment, such as generators, bus bars, transformers, and motors. It can discriminate between internal and external faults.

OBJECTIVES

Upon completion of this lesson, the trainee will be able to:

- Describe the operating principles of percentage differential relays.
- Identify the application and function of percentage differential relays.
- Demonstrate the parts of percentage differential relay type CA.

Task 2.2-1: Identifying and inspection for the percentage differential relay.

INTRODUCTION

The percentage differential relay (device # 87) is usually the first choice for protection of such items as generators, transformers, buses and large motors. Its main components are a differential operating coil, restraining coils, trip contacts, a harmonic restraint unit, an instantaneous unit, and targets.

Currents are applied to the percentage differential relays from current transformers located on both side of equipment to be protected. Percentage differential relays, operation is based on a percentage difference between the two currents from both sides.

For example, a large generator can be constructed so that both ends of each phase winding are accessible to current transformers. The current flowing out of the same phase can be measured and compared. If they are equal there is no fault; however, if the two currents are not the same, it means that there is a fault. Percentage differential relays are usually classified as high speed relays.

PRINCIPLE OF OPERATION

The differential relay compares the secondary currents of two CT's (Fig. 2.1-1). Current flowing into the first CT is compared with the current flowing out of the second CT. As long as the current leaving the second CT is equal and in phase with the current entering the first CT, the secondary currents will cancel completely across the operating coil.
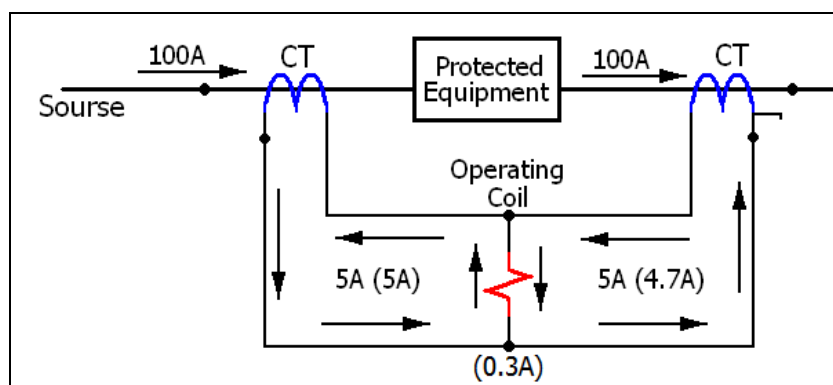
Fig. 2.1-1 Simple Differential Scheme Operation

The zone between the two CT primaries is known as the relay's "zone of protection". The relay will operate only for faults within its zone of protection.

The zone of protection lies between the two CTs. The scheme in Fig. 2.1-1 trips for any unbalance or CT mismatch present as long as the operating current is above pickup. There is no restraining element in this relay to prevent it from operation on very small unbalances. The figure illustrates the problem. The ampere values shown are assuming perfectly matched CT's and external impedance. With 100:5 CT's, if the primary current is 100A, there will be 5 amperes flowing in each CT secondary. Since the two outputs being compared are equal, they cancel completely across the operating coil. Normal system variances and CT ratio mismatches will cause a small current to appear across the operating coil. Refer to Fig. 2.1-1; the values in parentheses are values that may occur during normal conditions (5 and 4.7A). The imbalance (0.3A) appears across the operating coil. The relay would then operate for normal system conditions in this scheme.

To allow for normal unbalances that may occur, a restraint coil is placed in each CT circuit. Restraint coils produce a torque to hold the relay contacts open, while the operating coil torques tries to close the contacts. The coils are connected so that one restraint and the operating coil are in each CT circuit. Fig. 2.1-2 shows the proper connection of the restraint coils with respect to the current transformer polarities.
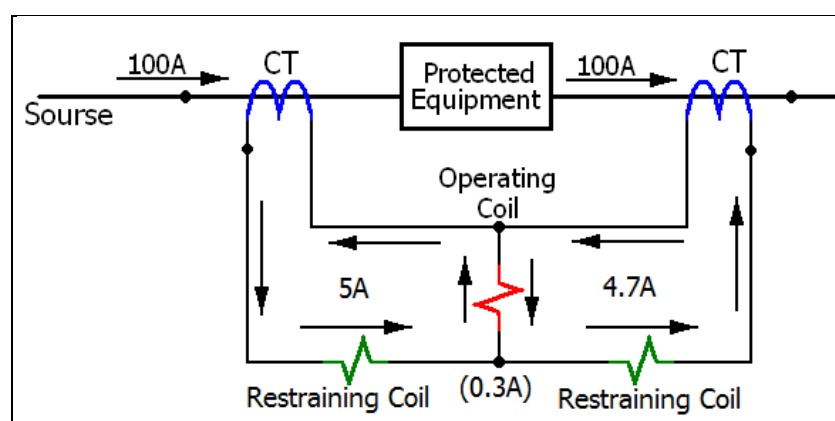
Fig. 2.1-2 Percentage Differential Scheme in Normal Condition

Connections for the restraint coils are extremely important in a differential scheme. The restraint coils must be connected in such a manner that the torque produced on the

relay disc under normal conditions is a summation of the two restraint currents, resulting in maximum restraint torque.

The relative polarity of the current transformers and the direction of primary current flow establish the direction of current flow in the restraint coils. When the current in the restraint coils is in the same direction, both coils induce voltages of the same polarity in the relay disc. These voltages cause eddy currents in the disc, which produce a torque in the same direction, restraining the relay operation.

In the case of external fault, the current in the two restraint coils is also in the same direction and although the current values increased the operating torque cannot overcome the restraining torque, so the relay will not operate (Fig. 2.1-3).
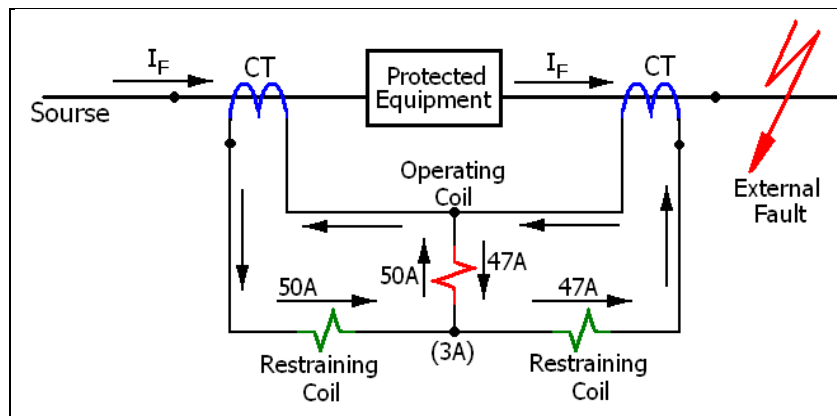
Fig. 2.1-3 Percentage Differential Scheme in External Fault Condition

If the current flowing in one restraint coil is reversed as in the case of internal fault as shown in Fig. 2.1-4, the restraining torque from both coils would tend to cancel out; therefore, the restraint is weakened or cancelled . The more sensitive operating coil will respond to the slightest difference, resulting in a large amount of contact-closing torque. This condition will cause the relay to operate and trip.

When properly connected, the restraint coils will desensitize the relay to high external fault currents and sensitize the relay to internal fault currents. The restraint coils allow a set percentage of imbalance to exist before the relay will respond. In Fig. 2.1-4, the imbalance exists, but the imbalance is great enough to cause the operating coil to overcome the restraint coil's torque.
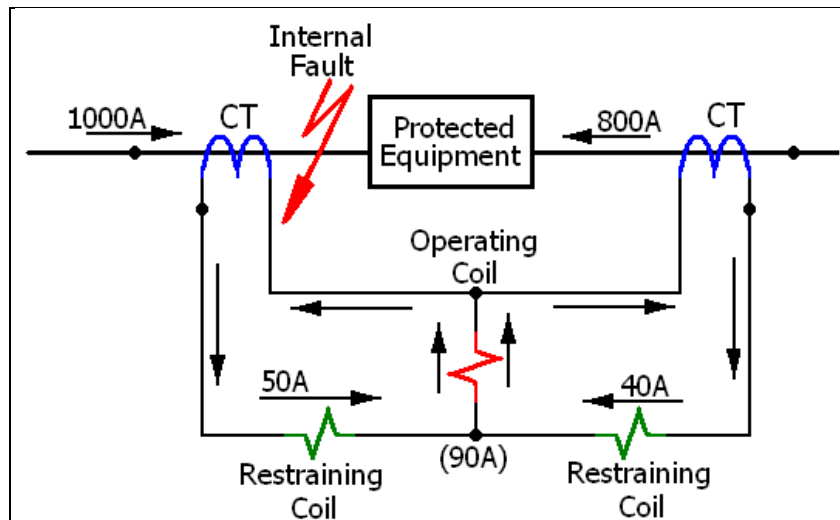
Fig. 2.1-4 Percentage Differential Scheme in Internal Fault Condition fed from both sides

Some differential relays are provided with taps that allow to set the percentage differential (sometimes called slope) from 10 to 50%. Fig. 2.1-5 shows such a family of curves. Another type provides a variable restraint. The slope is built into the relay and may be adjusted by tapping the restraint coil. To determine unbalance, use the following formula:

% unbalance = I_O /I_R(small) x 100

where

I_O = Current in the operating coil

I_R(small) = the smallest of the two restraining currents.
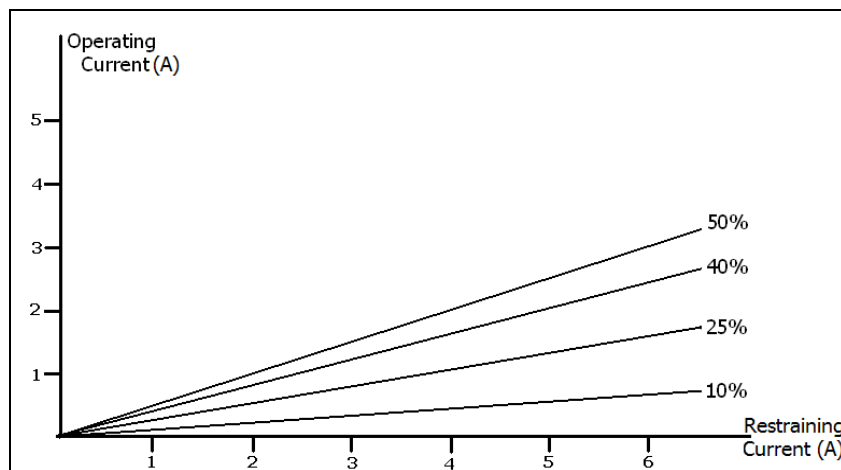
Fig. 2.1-5 Restraint Curves

In Fig. 2.1-1 & 2.1-2, the current in the operating coil is 0.3A. This value is obtained by subtracting the two CT secondary currents: 5 amperes minus 4.7 amperes. The smaller restraint current is 4.7 amperes.

Therefore, % unbalance = (0.3/ 4.7) x 100 = 6.38%

The percent unbalance does not exceed the relay's slope characteristic, which is 10% in this example; therefore, the relay will not operate.

Remember that, the objective of restraint coils is to prevent the relay from false operation for an external fault, which causes a heavy through current. When the fault is internal, there would normally be a large enough differential between the two CTs and sufficient current would flow through the operating coil to overcome the restraint and trips the relay.

When differential relays are used to protect large power transformers, it is usual to fit a harmonic restraint unit into the scheme. This is designed to prevent inadvertent tripping of the differential relay due to transformer in-rush current. This in-rush current may only last for a few cycles, but it could easily provide a false signal to the differential operating coil. During the in-rush period, the harmonic restraint unit opens a contact, which is connected in series with the differential tripping contact; to prevent tripping.

During an external fault condition (outside the relay's zone of protection) the amount of actual primary and secondary currents will increase. The percentage imbalance will change from the percentage obtained during normal conditions. Even though the actual current values change, as long as the percentage imbalance in the system does not exceed the relay's slope characteristic, the relay will not operate. In fact, due to the increased current seen by both restraint coils, more restraining torque is placed on the relay.

During an internal fault fed from one side (Fig. 2.1-6), the amount of torque produced by the operating coil far exceeds the restraint torque, so that the relay operates.
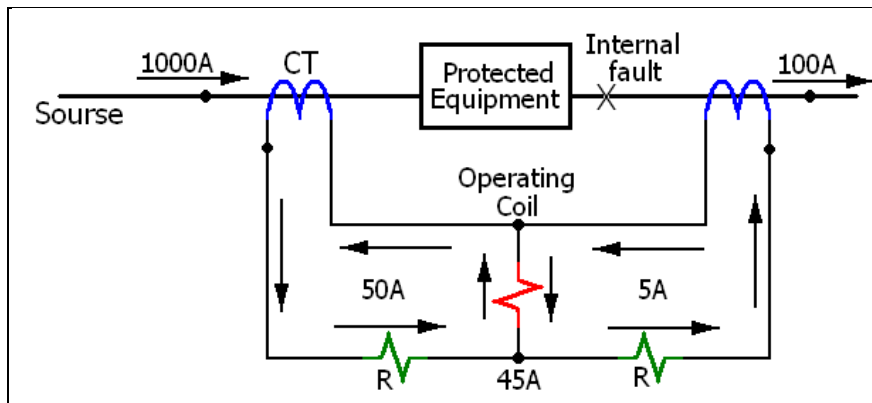
Fig. 2.1-6 Internal Fault Condition, Fed from One Side
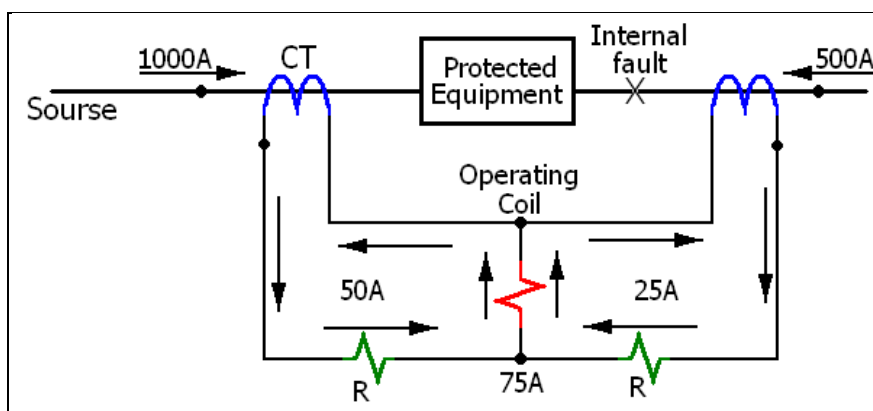
Fig. 2.1-7 Internal Fault Condition, Fed from Two Side

This would reverse the current flow in one side of the differential circuit and cause the currents to sum across the operating coil. In addition, since the current is reversed in one restraint coil, the torque produced by that coil would cancel most of the torque produced by the other restraining coil. The relay would immediately trip for such a condition.

As previously discussed percentage differential relays are polarity sensitive. The CTs must be installed, so that the secondary currents will cancel across the operating coil under normal operating conditions. Note the polarity marks in Fig. 2.1-6 & 7.

If a CT secondary was reversed by mistake, as in Fig. 2.1-8 where the secondary currents would sum across the operating coil instead of canceling and the relay would respond as if an internal fault had occurred.
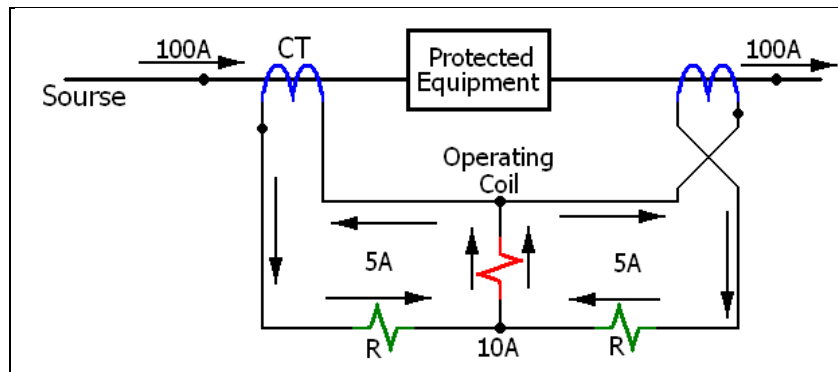
Fig. 2.1-8 Reversed CT Polarities

DIFFERENTIAL RELAY TYPE CA

The type CA percentage differential relay is used extensively for protection of power transformers. A schematic diagram of this relay is shown in Fig. 2.1-9.

2- Current transformer	3- Quadrature windings
4- Secondary winding	5- Operating coils
6- Restraining coils	7- Relay electromagnet
8- Protected equipment	9- Difference current
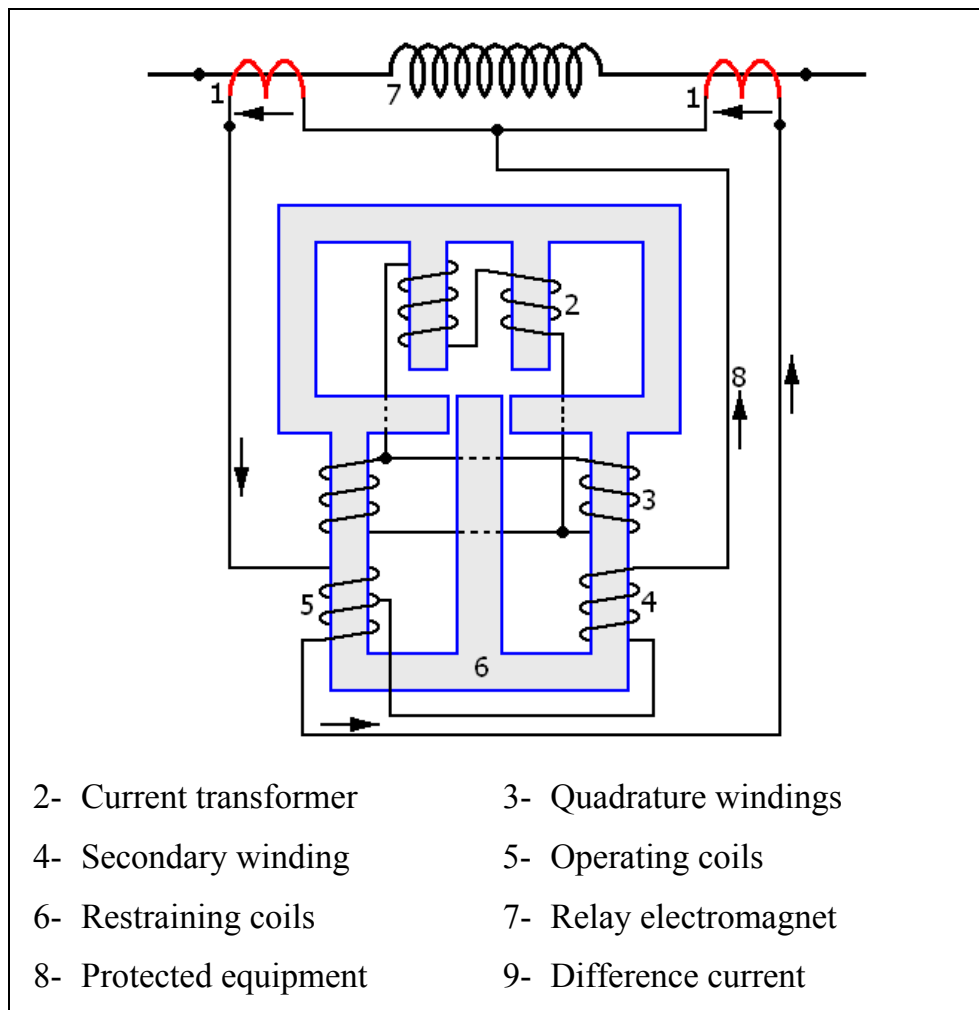
Fig. 2.1-9 Type CA Percentage Differential Relay

CONSTRUCTION OF RELAY TYPE CA

The Westinghouse type CA relay consists of a percentage differential unit and an indicating contactor switch. Principal parts of the relay and their locations are shown in Fig. 2.1-10.
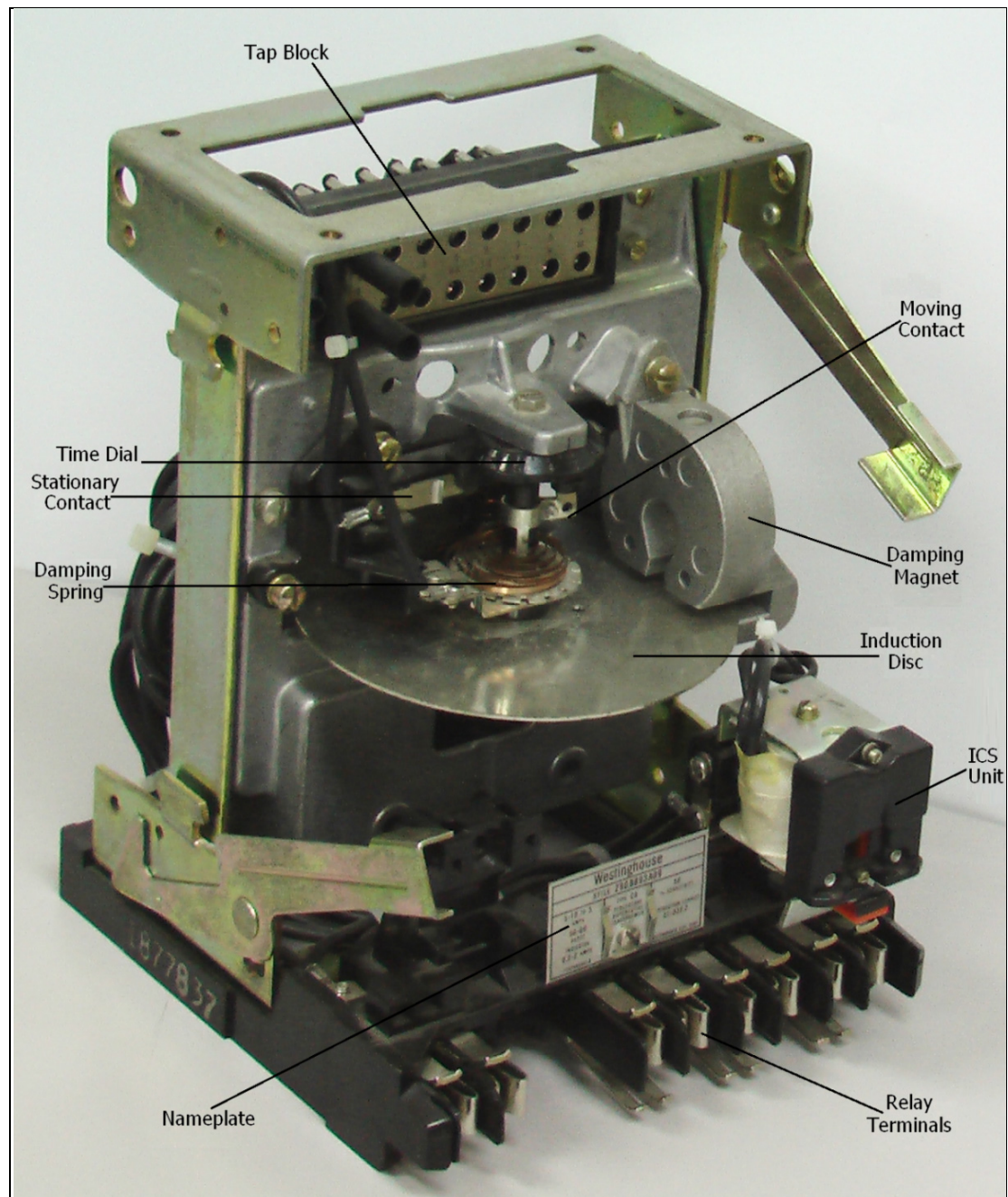
Fig. 2.1-10 Electromagnetic Differential Relay Type CA

(a) Front View   (b) Rear View
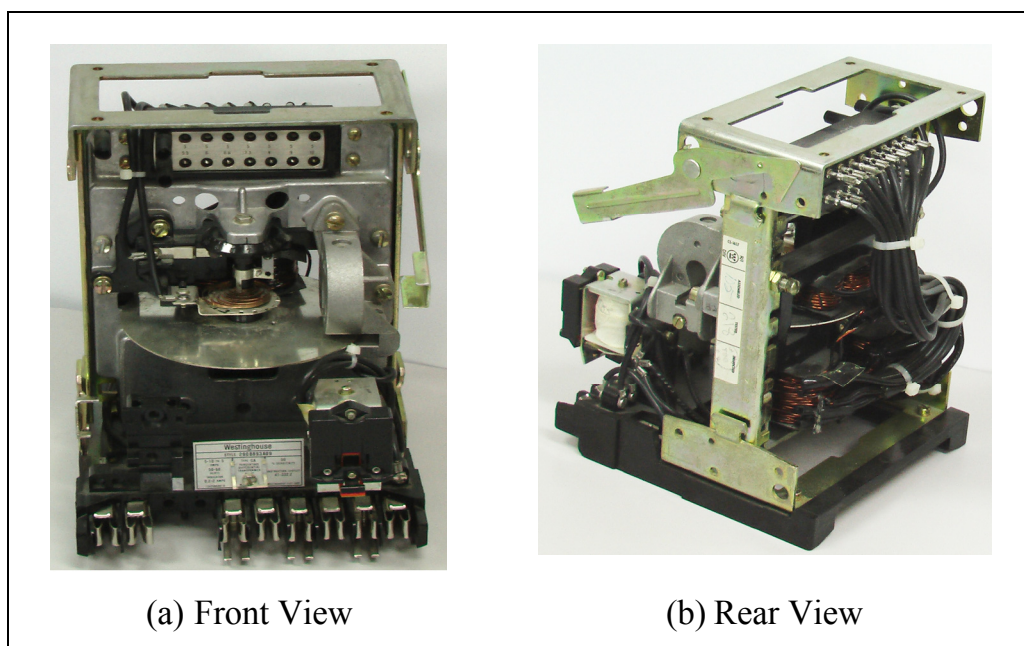
Fig. 2.1-11 Front and Rear Views for Percentage Differential CA Relay

The percentage differential unit is an induction disc unit with an electromagnet that has poles above and below the disc. Two restraint coils are placed on the lower right-hand pole (rear view) and connected in series. Their junction point is connected to the operating coil wound on the lower left hand pole. Transformer windings are wound on both the left- and right-hand poles and are connected in parallel to supply current to the upper pole windings. The upper pole current generates a flux, which is 90° out of phase with the lower pole resultant flux. The two fluxes react to produce a torque on the disc. If the operating winding is energized, this torque is in the contact closing direction. If current flows through the two restraining windings in the same direction, a contact opening torque is produced.

Electromechanical restraint relay (CA) is provided by a spiral control spring. In addition, double trip contacts available are equipped with their typical target and seal-in unit or indicating contactor switch. The relay is equipped with a time dial usually fixed to maintain a setting of time dial **one**, providing minimum disc travel, and therefore, quick response.

Referring to Fig. 2.1-12, the percent slope characteristic is graphically represented for the Westinghouse type CA relay. At lower values of current, a slightly different

percent slope is tested at a restraint current other than that specified by the manufacturer.
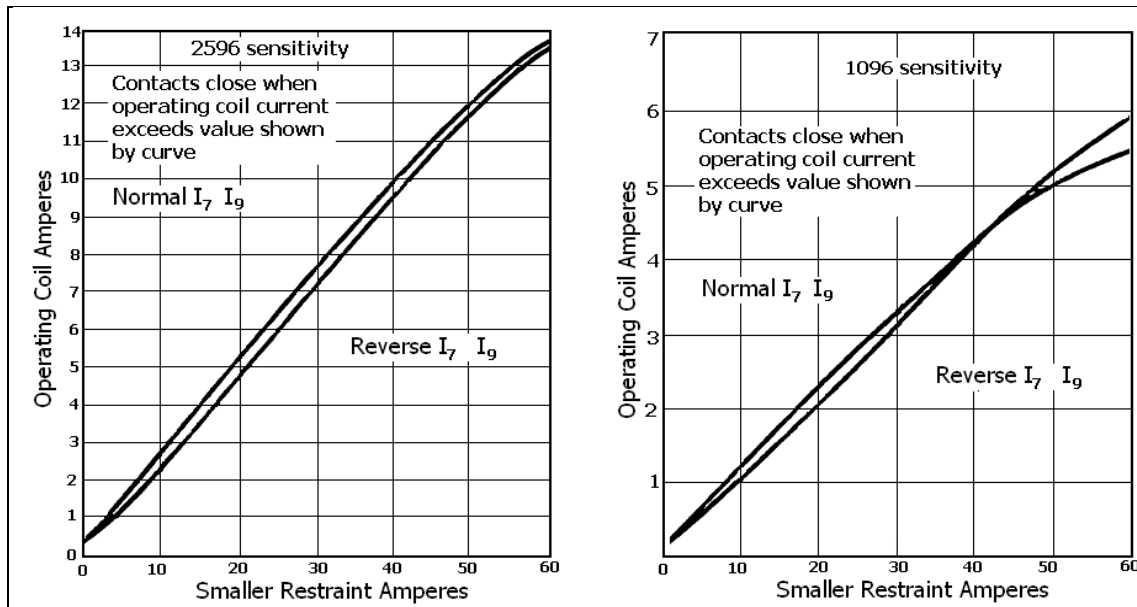
Fig. 2.1-12 Operating Characteristics of a Type CA 10 Percent & 25 Percent Sensitivity Generator Relay

An external schematic is shown in Fig. 2.1-13 for the three phases of a generator. Note the polarity of the connections.

When a differential relay is used to protect a generator or motor, identical CT ratios may be used for both primary and secondary. Transformers, however, may have different CT ratios. This results in unbalanced differential currents even under normal load conditions.

To correct this problem, some differential relays are equipped with CT ratio matching taps. These taps are selected so that they rebalance the relay magnetically when the restraint currents are unbalanced. Such relays work the same as their untapped counterparts for internal faults.
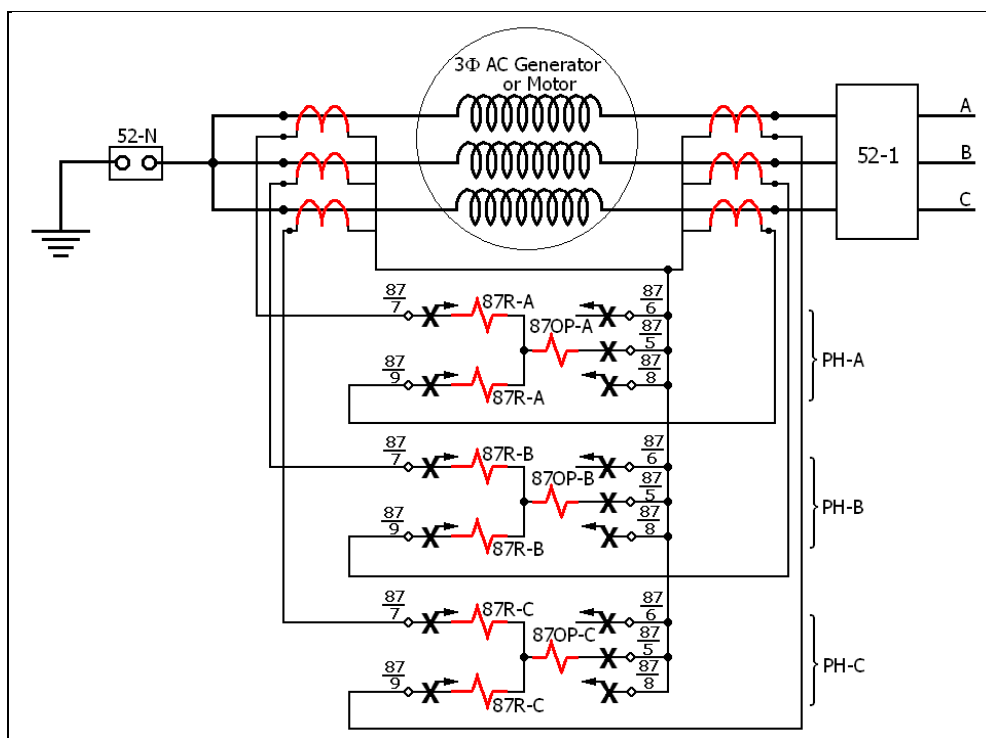
Fig. 2.1-13 External Schematic Diagram of a Type CA Generator Relay

The DC control circuit of the example of generator percentage differential scheme is indicated in Fig. 2.1-14.

APPLICATION OF DIFFERENTIAL RELAYS

The percentage differential relay is applied to each phase of large motors, generators, transformers or frequency changers. Available percentage slopes include 5, 10, 15, 25 and 50 percent, slope is incorporated to allow for small current transformer (CT) errors possibly due to CT ratio mismatch and/or CT saturation. The main function of the relay is to detect internal faults in the protected equipment. The current entering one end of a winding must be within a specified percentage of the current at the other end.
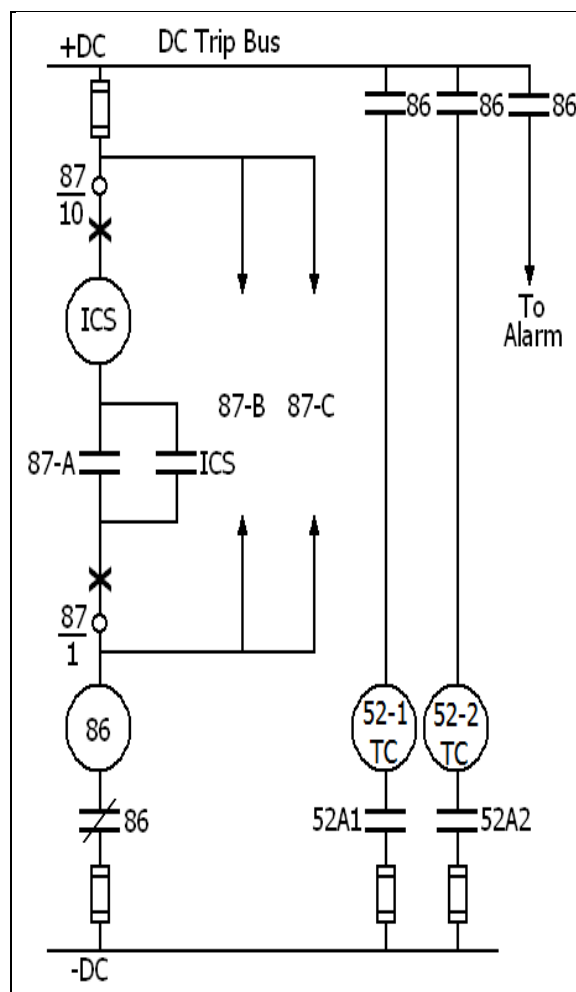
Fig. 2.1-14 DC Control Circuit for Percentage Differential Relay

DEVICE NUMBER CHART:

87: Generator percentage differential relay

87A: Restraining coil

87OP: Operating coil

86: Auxiliary tripping relay

52: Circuit breaker

TC: Trip coil

ICS: Indicating contractor switch

52A1 & 2: Breaker auxiliary contacts

SUMMARY

- Differential protection is normally used for generators, transformers, buses, and large motors.

- The principle of differential protection is simply that current entering the system must equal current leaving the system, under normal operating conditions (no fault).

- An internal fault will create an imbalance between incoming and outgoing currents and this will be detected by CTs, which in turn are connected to the relay.

- The relay will not trip for through faults, as incoming current will equal outgoing current.

- Where differential protection is applied to transformers, the CT ratios must be selected to allow for the turns ratios of the transformers.

- Under normal (no fault) conditions, a differential current may appear due to different CT characteristics and/or transformer tap positions.

- Restraint coils protect against inadvertent tripping due to the above errors. Percentage differential means, that the relay will only trip, when current through the differential operating coil is above a preset percentage of current in the restraint coils.

- Harmonic restraint coils prevent inadvertent tripping, due to inrush, at the moment the transformer is energized (connected from the first side).

FORMULAE

% unbalance = I_O / I_R.(small) x 100

where I_O = Current in the operating coil

             I_R (small) = the smallest of the two restraints

GLOSSARY

Restrain:	Resist operation.
Imbalance:	Inequality
Accessible:	reachable
Mismatch:	Variance
Inadvertently:	By mistake
Counterpart:	Corresponding item

REVIEW EXERCISE

Circle the letter a, b, c or d that correctly completes the statement and follow the directions to answer the other questions:

1. Differential relay usually use …………………….for each phase:
   a. Three Potential transformers.   b. Three current transformers.
   c. Two current transformers.   d. One CT & one VT.

2. The basic principle of differential relays is:
   a. To compare the secondary currents of two CTs.
   b. To divide the voltage by the current of each phase.
   c. To multiply the voltage by the current of each phase
   d. To add the secondary currents of two CTs.

3. A percentage differential relay utilizes .... to prevent false operation due to current transformer errors.
   a. Restraining coils.   b. Operating coil.
   c. Induction disc.   d. Instantaneous unit.

4. The device number of the differential relay is:
   a) 21   b) 87
   c) 59   d) 67

5. Name four equipment can be protected by differential relay.
   a. ………………………   b. …………………………….
   c. ………………………   d. …………………………….

6. Match the names of parts pointed with numbers on the following drawing.

	Restraining coil.	
	Operating coil.	
	Difference current.	
	Secondary winding.	
	Quadrant winding.	
	Relay electromagnet.	
	Current transformer.	
	Protected equipment.	
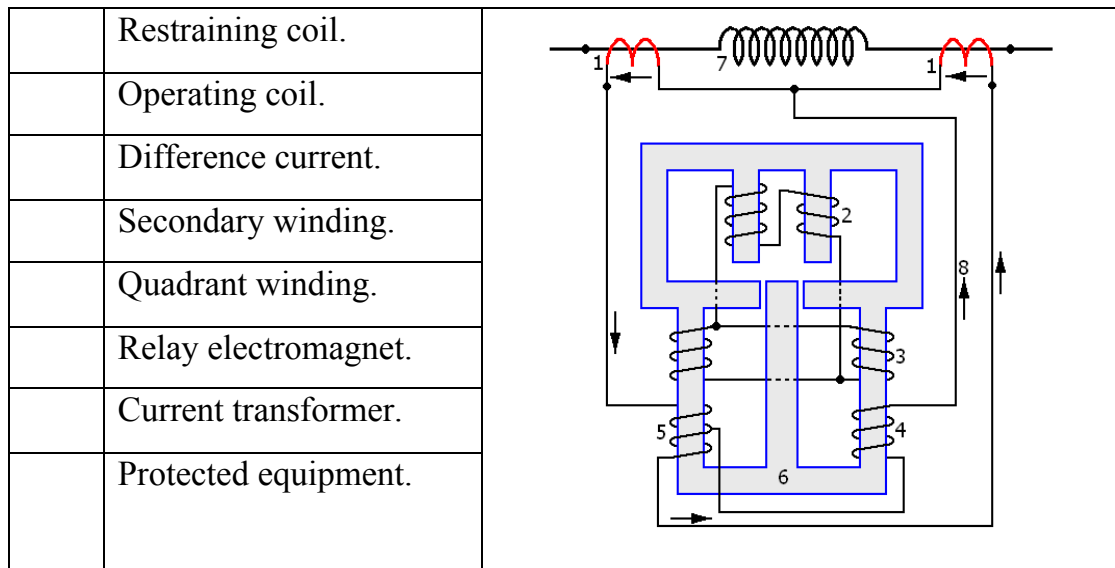
7. Complete the drawing shown below by connecting differential relays to CT's.
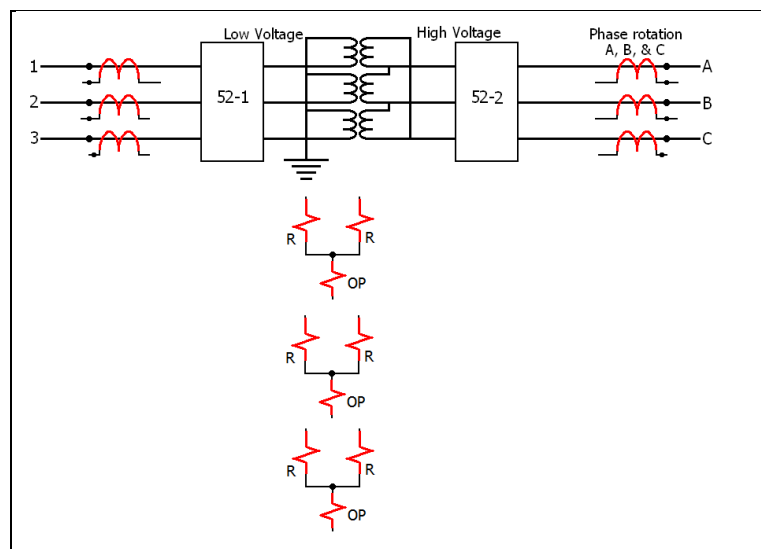
8. If the percentage slope of a differential relay is 25% and the restraint current (I_{REST}) is 4 amps. Using the following percentage curves shown find the required current to operate the relay (I_{OP}).
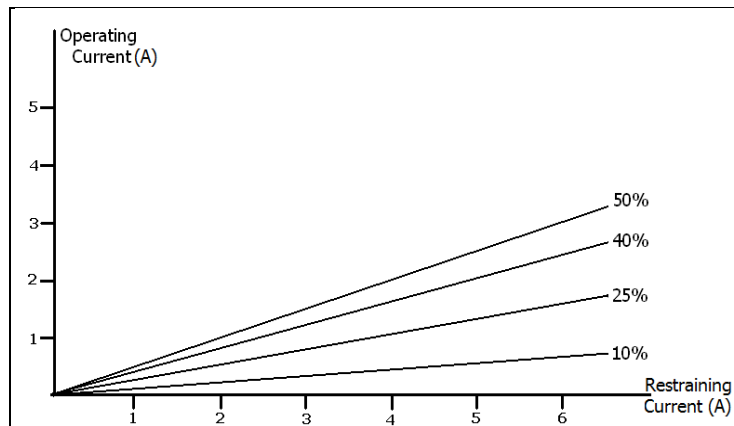
9. Study the tripping circuit given below and then match the names of parts pointed with numbers & letters on the drawing shown.
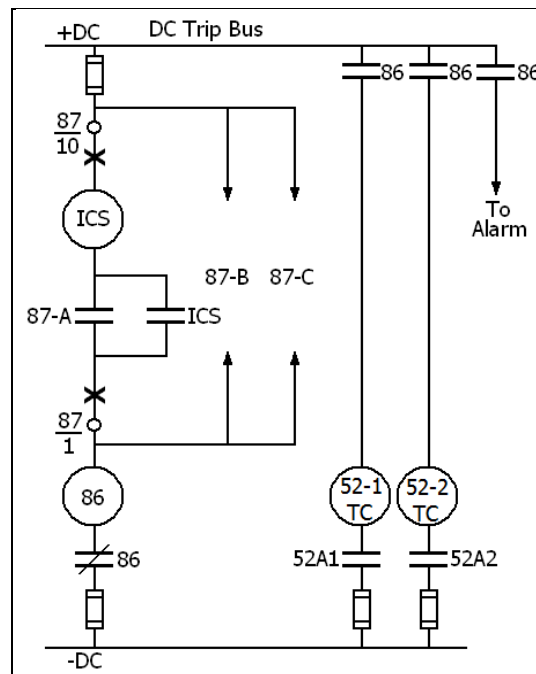
	Auxiliary tripping relay
	Circuit breaker
	Trip coil
	Indicating contractor switch
	Breaker auxiliary contacts
	Operating coil
	Generator percentage differential relay
	Restraining coil

TASK 2.1-1

DIFFERENTIAL RELAY TYPE CA

OBJECTIVE

After completion of this task, the participants will be able to:

- Identify and inspect the percentage differential relay type CA.

TOOLS, EQUIPMENT & MATERIALS

- Differential percentage relay type CA.
- Instruction manual.
- Personal safety equipment as recommended in relay workshop.

PROCEDURE

1. Remove the relay from the casing carefully.

2. Inspect the percentage differential relay, check for the following items:

   - The electromagnet

   - Tap block

   - Stationary contact

   - Moving contacts

   - Damping magnet

   - Induction disc

   - Restraint coils

   - Operating coil

   - Time dial

3. Identify and inspect the indicating contactor switch (ICS).

4. Identify the terminals of restraining coils and operating coil.
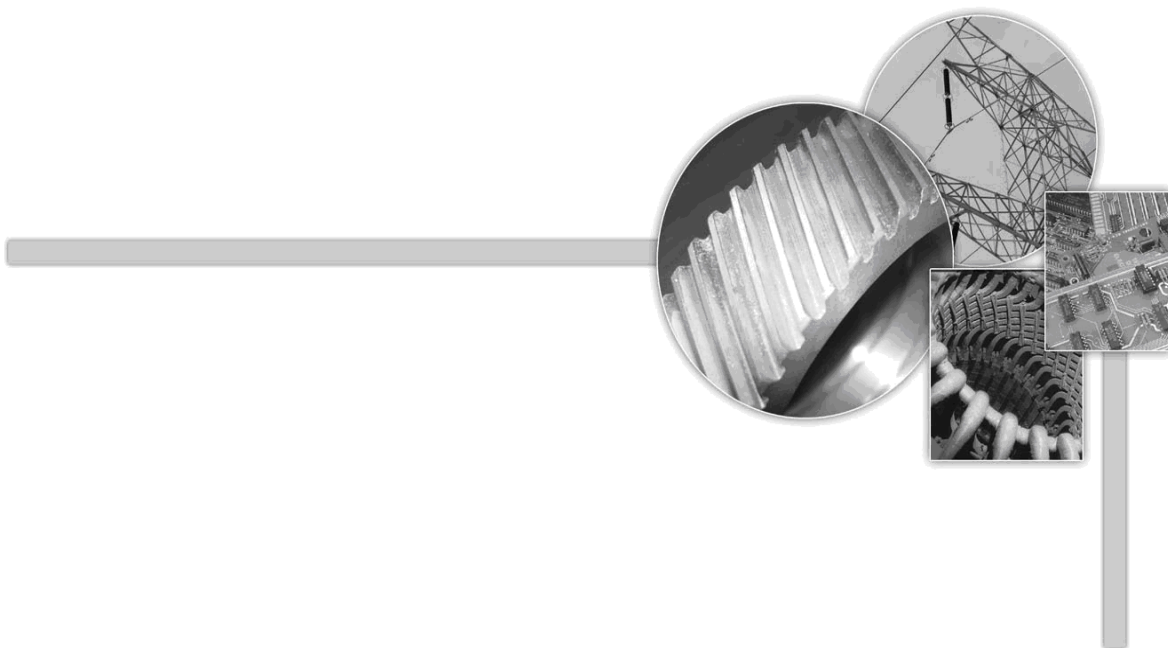
LESSON 2.2

DISTANCE PROTECTION

LESSON 2.2

DISTANCE PROTECTION

OVERVIEW

This lesson discuses the distance protection as one of the important main protection schemes used for transmission lines. It can detect the fault through instrument transformers and trip the circuit breakers of the transmission line.

OBJECTIVES

Upon completion of this lesson, the trainees will be able to:

1. Identify the R-X diagram.
2. Verify the fundamentals of distance relaying.
3. Identify the distance relay characteristics.
4. State distance relaying schemes.

Task 2.2-1: Demonstration for main parts of a distance relay type KD-10.

INTRODUCTION

A widely used and very successful method of protecting transmission lines is by the distance relaying. The term "distance" is applied to a family of relays that respond to a ratio of voltage to current and, therefore, to impedance or a component of impedance. Impedance is a measure of distance along a transmission line protected with such relays, which explains the choice of the term distance.

R-X DIAGRAM

This diagram, as its name implies, is the plot of impedance on the basis of its resistive and reactive component, (Fig. 2.2-1).

$$Z = V / I$$
$$R = Z \cos \varphi$$
$$X = Z \sin \varphi$$
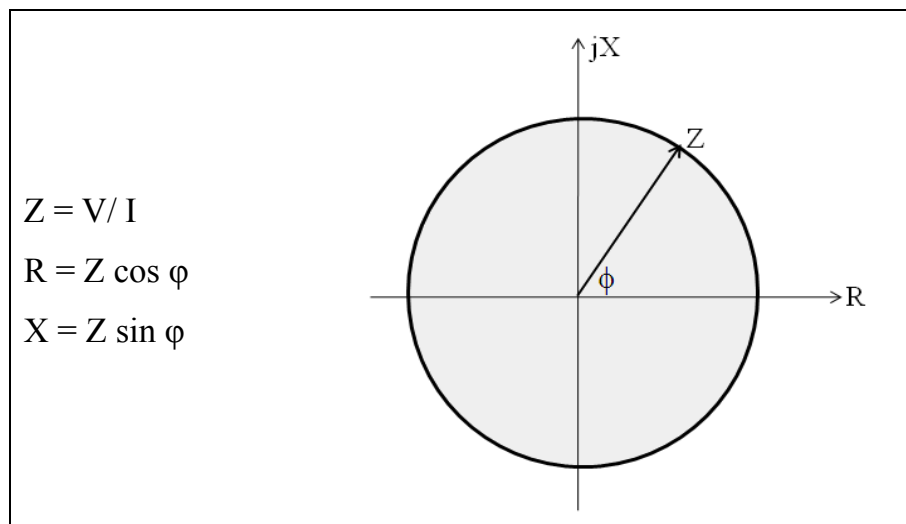
Fig. 2.2-1 Representing Impedance Vector on R-X Diagram

Fig. 2.2-2 shows impedance diagram for a line having 50Ω resistance and 86.6Ω reactance. The total impedance is 100Ω with angle 60° from the reference vector.
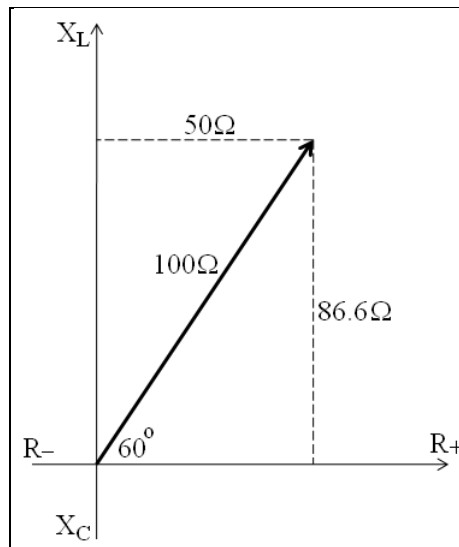
Fig. 2.2-2 Impedance Diagram

FUNDAMENTALS OF DISTANCE RELAYING

Relays that measure the distance to a fault on transmission line are called distance relays. Since the impedance of transmission line is proportional to its length, for distance measurement it is appropriate to use a relay capable of measuring the impedance of a line up to given point. Such a relay described as distance relay and designed to operate only for faults occurring between the relay location and the selected point, thus giving discrimination for faults that may occur on different line sections.

IMPEDANCE RELAY

To explain the principle of distance relays, a balanced beam unit is used, as shown in Fig. 2.2-3.
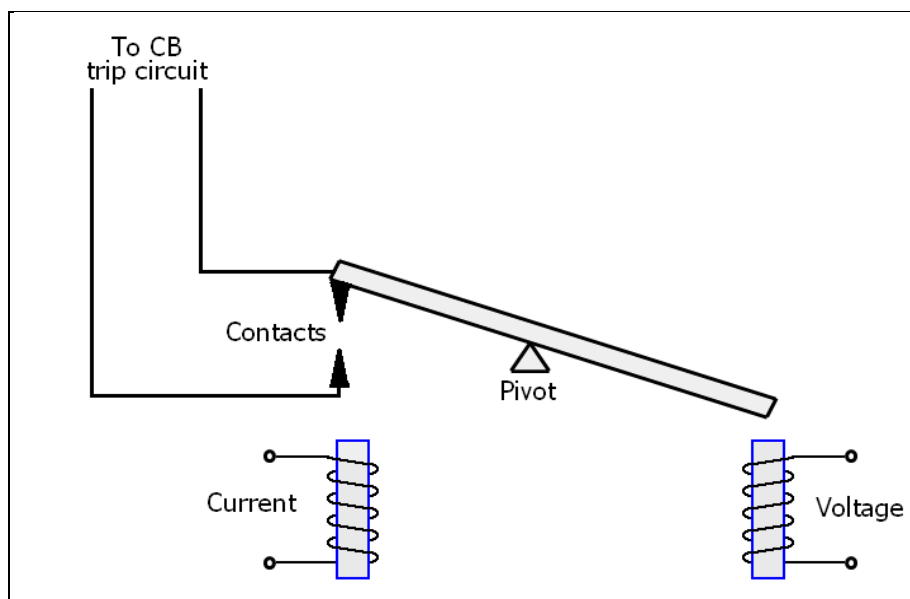
Fig. 2.2-3 Balanced Beam Equivalent for Distance Relay

The voltage coil is fed from the voltage transformer on the line or bus while the current coil is fed from current transformer on the protected line. Under normal operating conditions, the voltage coil's attractive force is stronger than that of the current coil, hence the tripping contacts holds open.

If a fault occurs on the line, the magnitude of current increases greatly and the current coil's attractive force will overcome the restraint of the voltage coil. The balance beam see-saws in the opposite direction and closes the contacts in the tripping circuit, thus tripping the line circuit breaker. The tripping force depends upon the comparison, that is, the ratio of voltage to current.

$$\text{Line impedance } Z_o = V / I$$

Fig. 2.2-4 illustrates the above balanced beam operation during a fault on a transmission line, the fault current increases and the voltage at fault point reduces. The ratio V/I is measured at the location of CTs and VTs. The voltage at VT location depends on the distance between the VT and the fault.

If fault is nearer, measured voltage is more less. If fault is farther, measured voltage is more. Hence each value of V / I measured from relay location corresponds to distance between the relaying point and the fault. Hence such protection is called Impedance Protection or Distance Protection.
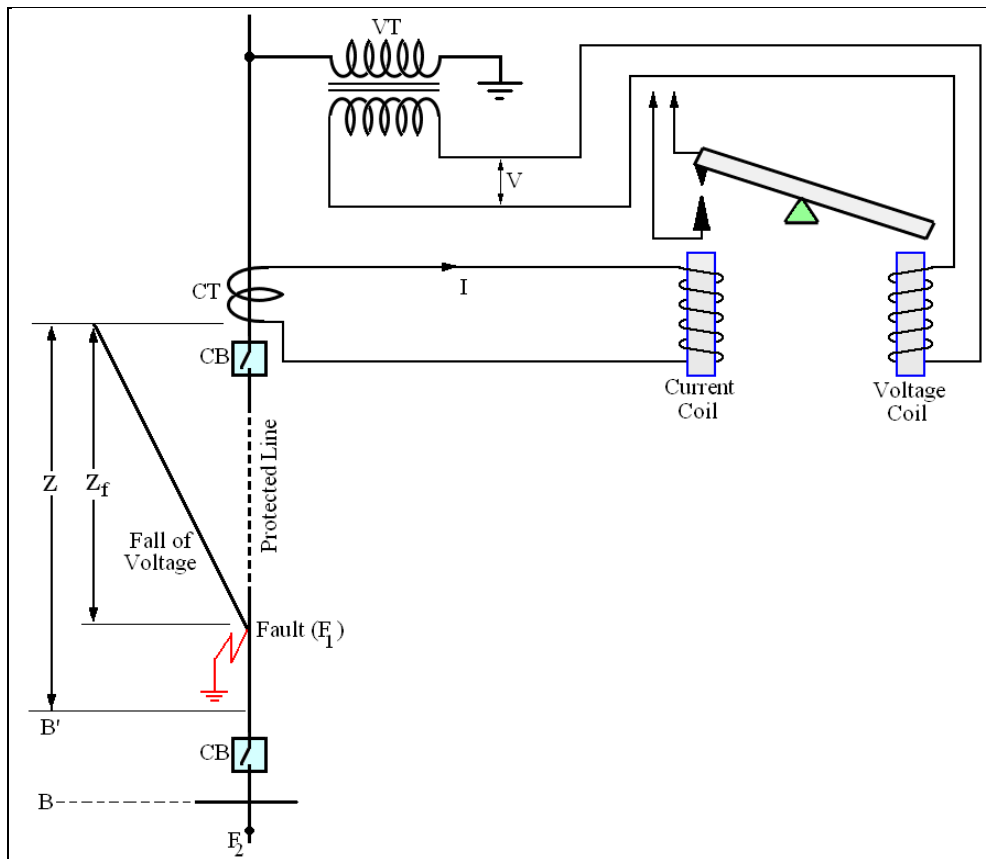
Fig. 2.2-4 Explaining Distance Protection

The operating torque (T_I) developed by the current coil is given by:

$T_I = k_1 I^2$ (operating torque)

The restraining torque (T_V) developed by the voltage coil is given by:

$$T_V = k_2 V^2$$

for operation:

$K_1 I^2 > k_2 V^2$

$V / I < \sqrt{(K_1 / K_2)}$ or $Z_o < \sqrt{(K_1 / K_2)}$

Thus the relay operates if the line impedance (Z_o) falls below a certain value as shown in Fig. 2.2-5, the balance $V / I = Z_o$ (radius of circle - setting).

$V / I = Z_1 < Z_O$, trips

$V / I = Z_2 > Z_O$, does not trip.
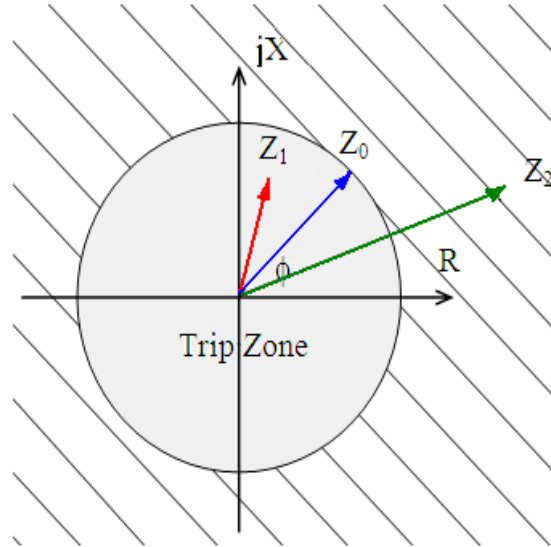
Fig. 2.2-5

Fig. 2.2-6 shows an example. The line is 125 miles long and the total impedance is 100 ohms. If we have a fault on the line, say, a direct phase to phase fault, then the only impedance in the circuit is that of the conductors themselves. At the half way point, the impedance will be 50 ohms, at three quarter length, 75 ohms, and so on. The relay is installed at the substation close to the breaker, and it can be adjusted to reach-out as far along the line as we wish.
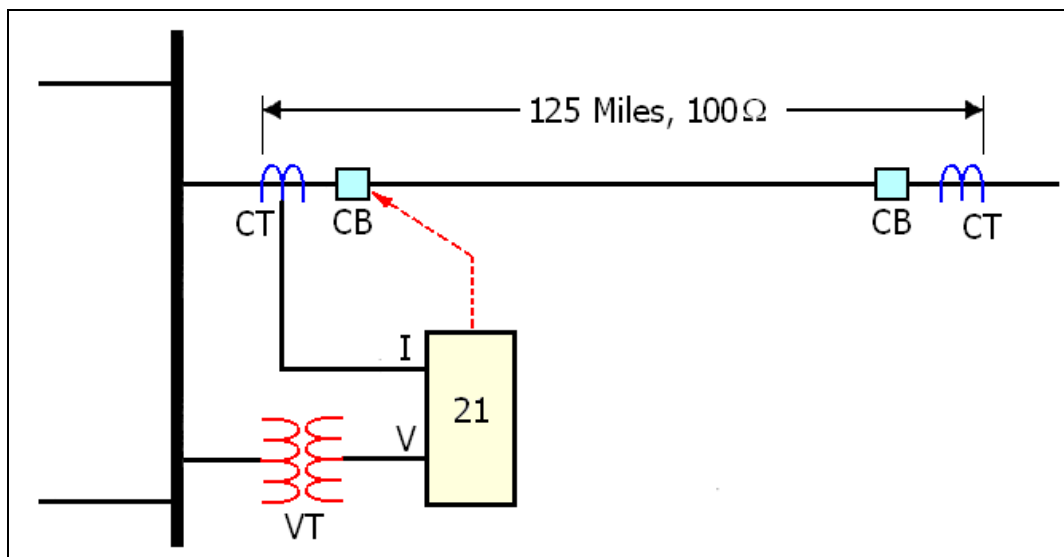
Fig. 2.2-6 Distance Relay on a 125 Miles Line

Typically, it will be set to protect up to 90% of the length of the line, that is, for an impedance of 90Ω. The relay actually sees secondary values of current and voltage from the CTs and VTs, so that it really measures secondary impedance.

The relay continuously compares voltage and current and if the primary impedance falls below 90 Ω (90% of the line impedance), it will trip its associated breaker. However, if a fault occurs beyond the line, the impedance will be higher than 90Ω and the relay will not trip. Hence the relay is giving the desired selectivity.

Usually a second element is installed, as shown in Fig. 2.2-7, to protect for the remainder of the line and reach-out into the second line or zone. A third element may be added to reach even further, providing local and remote back-up protection.

In each case, a timer is added in order to delay operation of the backup protection (second and third elements, as shown in Fig 2.2-7 and allow the primary protection to operate in those zones.
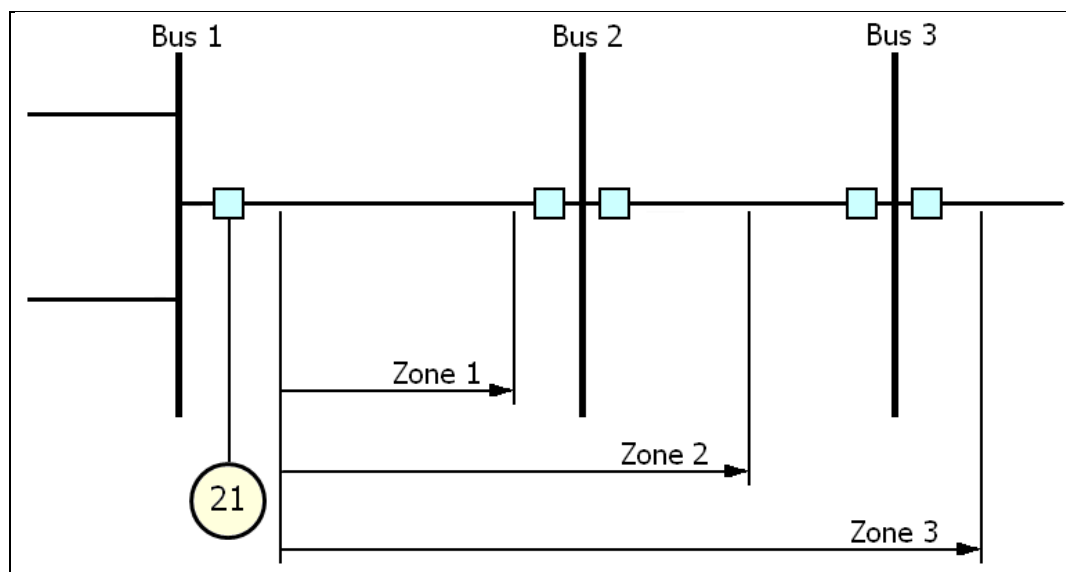
Fig. 2.2-7 Distance Relay with 3-Elements for 3-Zone Protection

The distance relay measures the line impedance, not only the resistance. Typically, the conductors in 125-miles long transmission line will exhibit a resistance 50Ω, and reactance 86.6Ω. Fig. 2.2-8 shows this plotted on an impedance diagram. Resistance is shown along the horizontal reference vector and inductive reactance is shown on the vertical axis. Capacitive reactance, if present, would be shown on the negative vertical

axis. In this example, we will assume that the line reactance of 86Ω has taken into account both inductive and capacitive reactance. Plotting resistance and reactance, we find that the total impedance comes to 100Ω and it is at an angle of 60° from the reference vector. If the relay is set to protect 90 percent of the line, it will operate for any impedance along the line between zero and 90Ω.

Actually, the simple balanced beam type relay would operate for anywhere within the circle where 90Ω is the radius. The balanced beam does not take into account phase angle or direction of current flow. Even when current through the CT is reversed, the relay still responds to high current in relation to voltage. That is, it sees low impedance. Fig. 2.2-8 shows the circle diagram. For a fault upstream (in bus direction) the operating point would be in the third quadrant. To avoid this problem, directional relays, device number 32, are usually combined with balanced beam relays in order to restrict operation to the faults downstream (in line direction) of the relay.
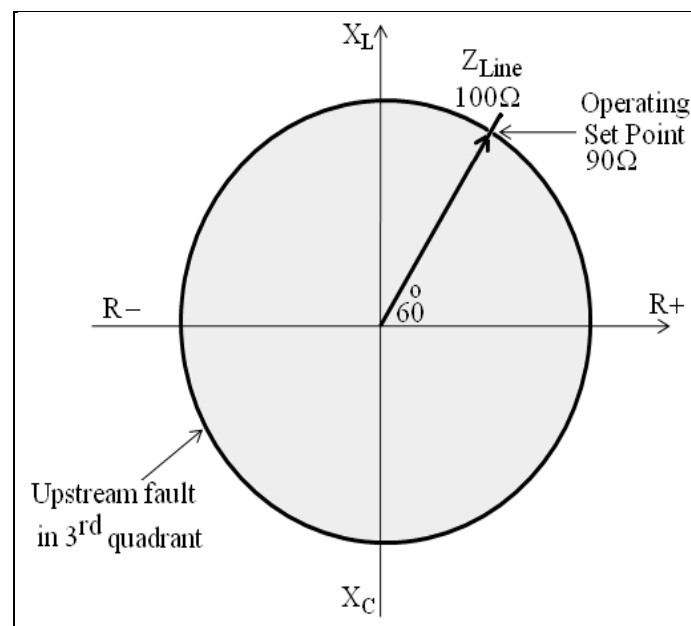
Fig. 2.2-8 Impedance Diagram for Balanced Beam Relay

A practical method of indicating the characteristic of an impedance element is the R-X diagram shown in Fig. 2.2-9 with a directional element added.
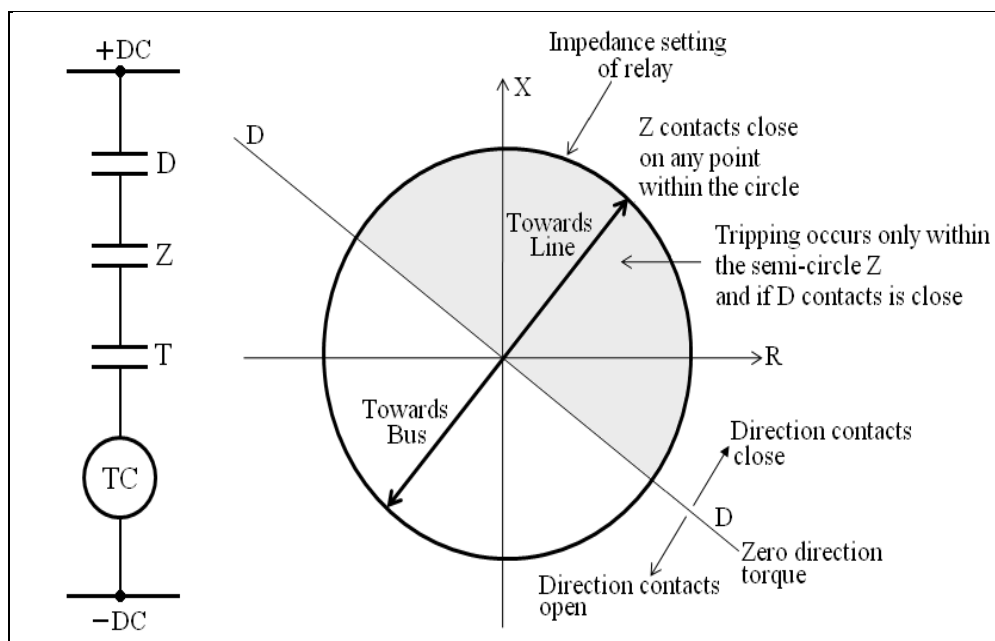
Fig. 2.2-9 Impedance Element with Directional Control

Any combination of current and voltage that produces a value of impedance, which falls within the semi-circle (above the directional line D-D), will trip the breaker.

The impedance relay has two disadvantages:

- It is affected by arc resistance.
- It is highly sensitive to power swings, because of the large area covered by the impedance circle.

POWER SWING

Power swings are oscillations in power flow, which might be caused by sudden removal of faults, loss of synchronism or changes in direction of power flow as a result of switching. A power swing may cause the appearance impedance measured by a distance relay to move away from the normal load area and into one or more of its tripping characteristics, thus causes unwanted trip.

To ensure the stability of distance relay, power swing blocking function is integrated in most of the modern distance relays to block the operation during a real power swing. Power swing detectors prevent distance relays from mal-operation under power

system out-of-step conditions. The traditional swing detection approach is to measure the time, which the traveling swing impedance trajectory needs to pass through two distance relay setting stages.

ARC RESISTANCE

The arc resistance can be computed approximately from the empirical formula:

$R_a = (8750 \text{ L}) / I^{1.4}$

Where   L is the length of arc (feet)

             I is the current in the arc (ampere).

MODIFIED IMPEDANCE TYPE RELAY

An impedance element can be modified to see a higher value of impedance in the line direction than what it sees in the bus direction. This is called "biasing" or "off-setting" the characteristic. It is done by introducing a controlled value into the voltage element, and phase angle of current from the current supply, (Fig. 2.2-10).
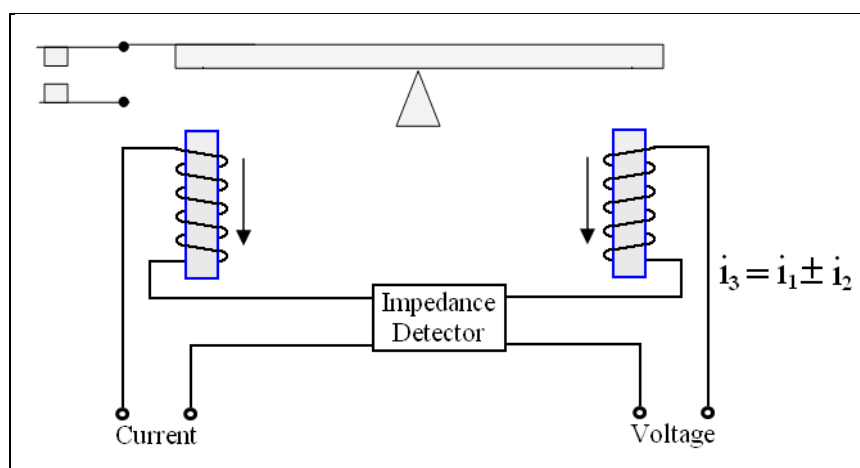
Fig. 2.2-10 Modified Impedance Element

When power flows out on the line, the induced current i_2 will combine vectorially with i_1 to produce a current i_3, which is less than i_1. This decreases the force of the E coil and allows closing of the relay contacts at a lower value of current I.

For a given value of line voltage, we now require less current to operate.

In other words, the impedance setting of the relay "reach" has been increased for power flow from bus to line. When power flows from the line to the bus, current i_3 is greater than i_1. The voltage restraint is increased and a greater value of current I is required to close the contacts. This is equivalent to a decrease in the impedance setting of the relay for power flow from line to bus. The R-X diagram in Fig. 2.2-11 shows the off-set feature of the modified impedance type relay.
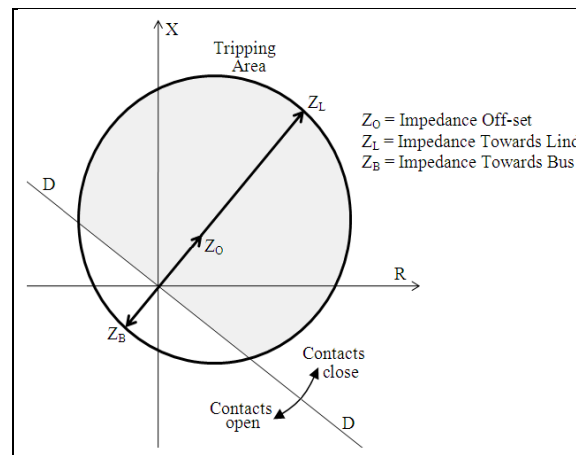
Fig. 2.2-11 Modified Impedance Element with Directional Control

MHO-TYPE ELEMENT

Mho element is inherent directional with voltage restraint as mentioned above. The element is normally biased to produce an impedance circle that passes through the origin of R-X diagram as shown in Fig. 2.2-12.
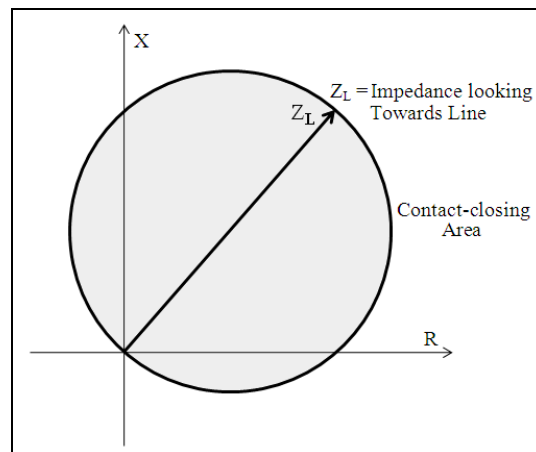
Fig. 2.2-12 Mho Element

Since the contact closing area does not lap into the reverse or bus direction, the Mho element is inherently directional and it will discriminate between faults towards the line and those towards the bus. A separate directional element is not required.

In some applications, a Mho element may be offset or completely reversed to respond to faults in the reverse or bus direction. This usually applies only to one Mho element of a relay having two or three Mho elements.

Induction-cup-type relay is used mostly for the Mho element to explain the operation, as shown in Fig. 2.2-13. The diagram does not show the bias interconnections or the adjustable components.
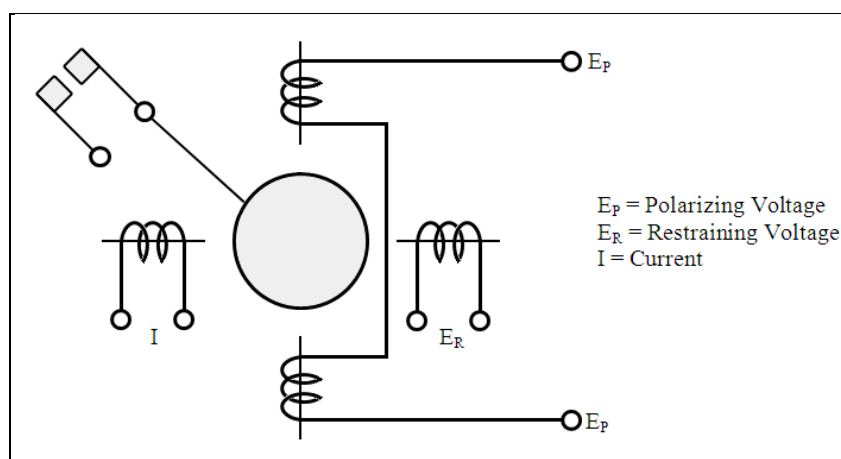
Fig. 2.2-13 Mho Element

The polarizing voltage (E_P) establishes the reference flux. The restraint coil (E_R) maintains sufficient torque under normal voltage conditions to keep the contacts open. Coil (I) produces a contact-closing torque when the current is in the desired direction with respect to the polarizing voltage. The induction cup will rotate to close the contacts when the current in coil (I) is high enough to produce a torque that overcomes the weakened restraint in coil (E_R).

REACTANCE TYPE ELEMENT

The reactance type element was developed for protection of lines where the resistance of a power arc would introduce an error in the impedance measurement by a distance

relay. Since arc resistance has no effect on the inductive reactance of line, the reactance element is designed to measure reactance rather than impedance. This is done by introducing a potential-derived current at a 90° phase angle out of the current measuring component of the relay.

In Fig. 2.2-14, the current (i) leads voltage (E) by approximately 90° due to reactance of condenser C This leading current creates a contact-opening force. Any value of current (I) that acts to close the contacts, must have a sufficient lagging reactive component to overcome the force of coil (i).
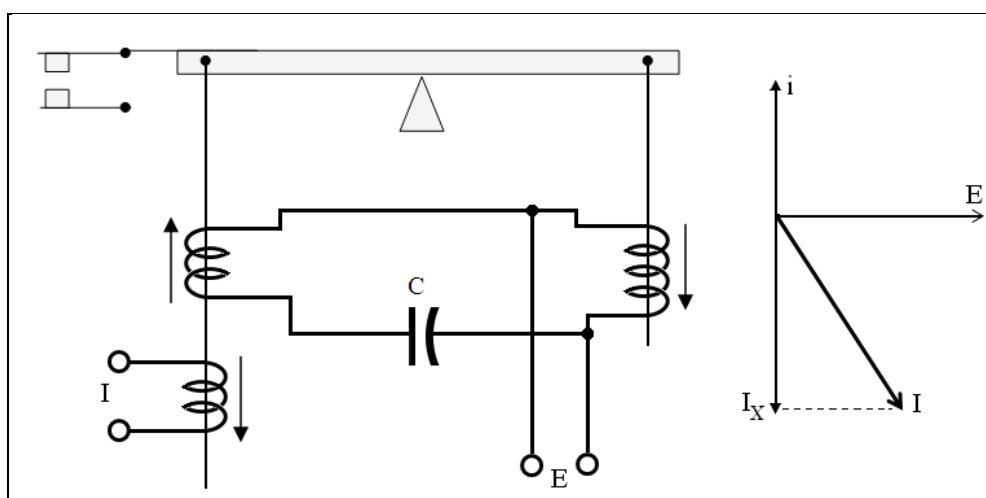
Fig. 2.2-14 Reactance Element

The operating characteristic of the reactance relay appears as a straight horizontal line on the R - X diagram when pure reactance is measured. If a resistance component is also present, the line becomes circular, as shown in Fig. 2.2-15.

Impedance Z_1 in Fig. 2.2-15 will not close the contacts of the reactance element; however, impedance Z_2 of more ohmic value will close the contacts. The reactance element cannot be used alone because it does not distinguish between normal load currents and fault currents, nor will a simple directional control element work with a reactance element. An impedance characteristic must be imposed on the reactance element to make it inoperative under normal loads, as will be explained later.
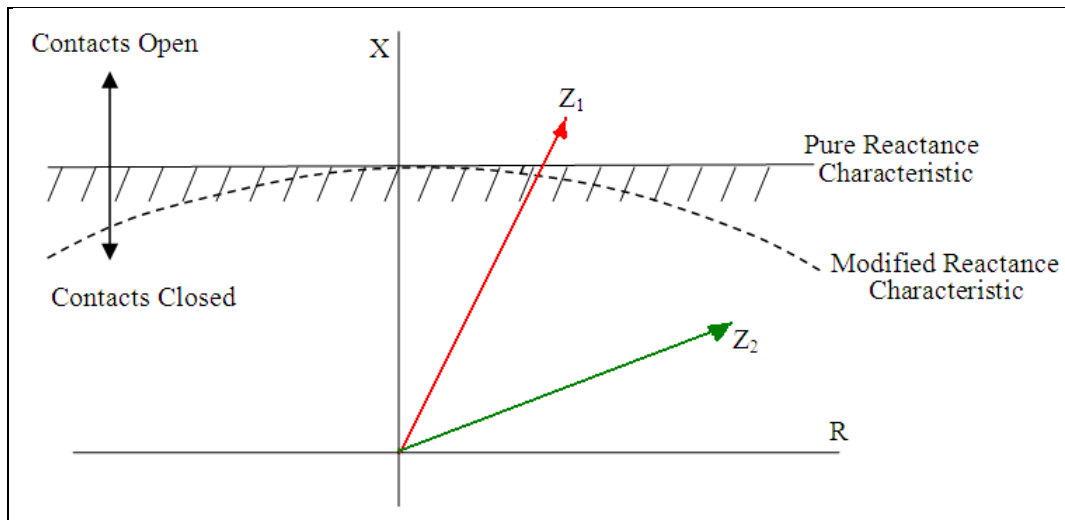
Fig. 2.2-15 Reactance Element

REACTANCE-TYPE RELAY

The reactance-type distance relay combines the reactance-type element with a directionally controlled impedance element. The latter may be either Mho element or impedance element plus a directional element.
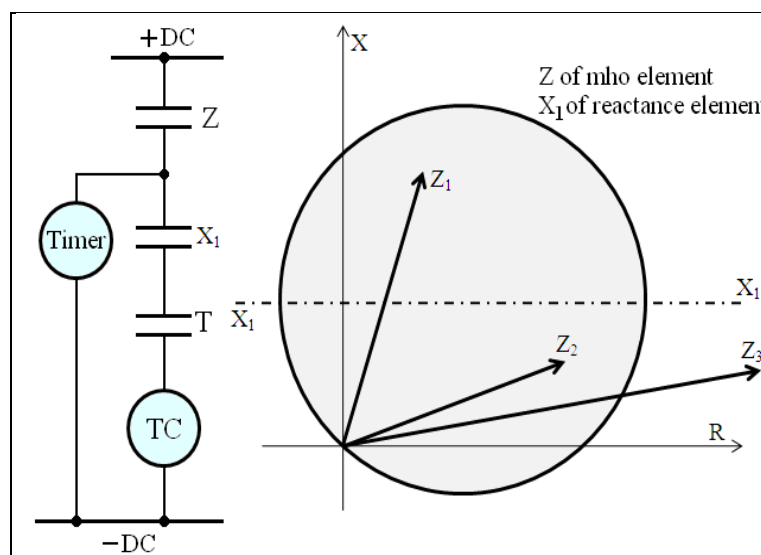
Fig. 2.2-16 Reactance-Type Distance Relay

Load Z_1 will cause trip through operation of the Mho element because this load impedance falls within the circle. It does not affect the reactance element because its

reactance component is above the line (X_1). A timer may be connected to the Mho element contact as shown in Fig. 2.2-16.

Load Z_2 will cause trip due to the operation of both elements, Mho and reactance, because this load impedance is within the circle and it is also below the reactance line (X_1). When the contacts of both elements close, instantaneous tripping takes place.

Although (Z_3) is below line (X_1), it will not cause trip because this load impedance is outside of the impedance circle. This illustrates how a normal heavy load will not operate the reactance element.

STEP DISTANCE RELAYS

Distance relaying may be applied to a line as a single-zone protection that reaches or extends out to 80 or 90% of the line length and provides rapid or instantaneous tripping. The remaining 10 to 20% of the line must be protected by another stage relay. Distance relaying is also applied to a line as a two or three-zone protective scheme that includes the first-zone protection just mentioned, and also provides additional reach to include the total length of the protected line plus an extended reach into associated lines as a back-up protection for these lines. This is shown graphically in Fig. 2.2-17.
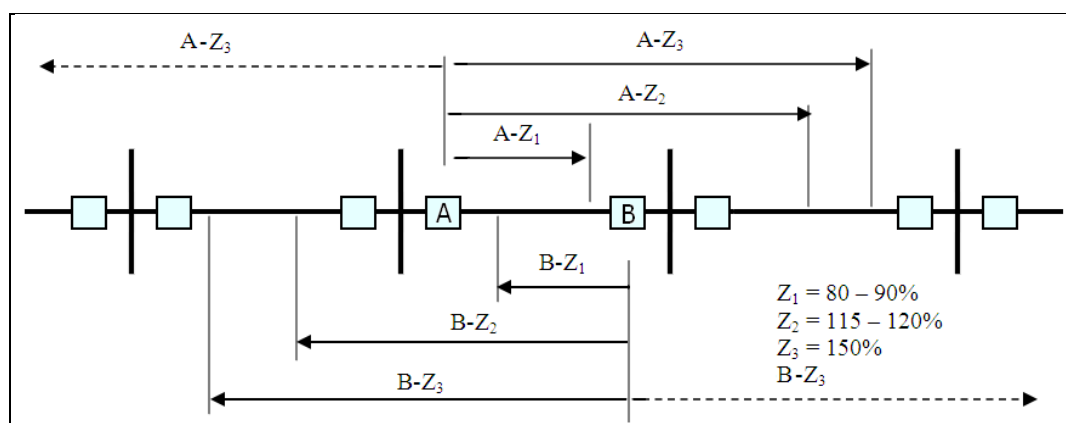
Fig. 2.2-17 Step Distance Relaying

The distance relays at station A have a first zone (A-Z_1) reach of 80 to 90% of the line, a second zone (A-Z_2) reach of about 115-120% of the line and a third-zone (A-

Z_3) reach of about 150% of the line. In some applications, the third zone may be non-directional, responding to faults in either direction. Zone 1 is always instantaneous in operation; Zone 2 has a definite time-delay (0.4 to 0.5 sec); Zone 3 has a greater time-delay than Zone 2 (0.8 to 1 sec).
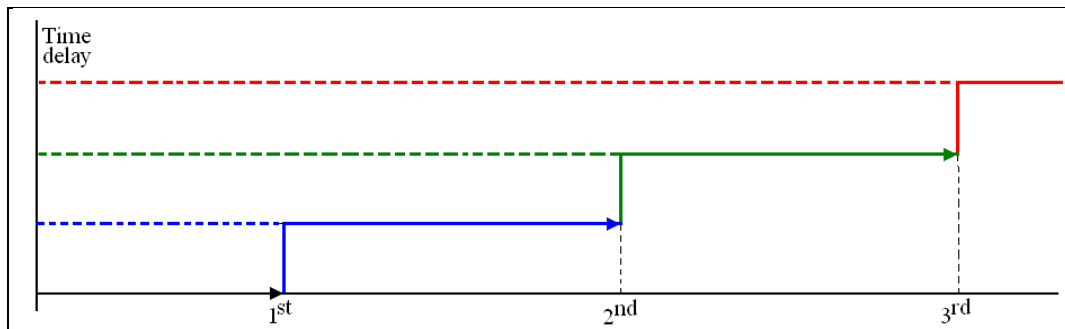
Fig 2.2-18 Coordination Time for Distance Relay Stages
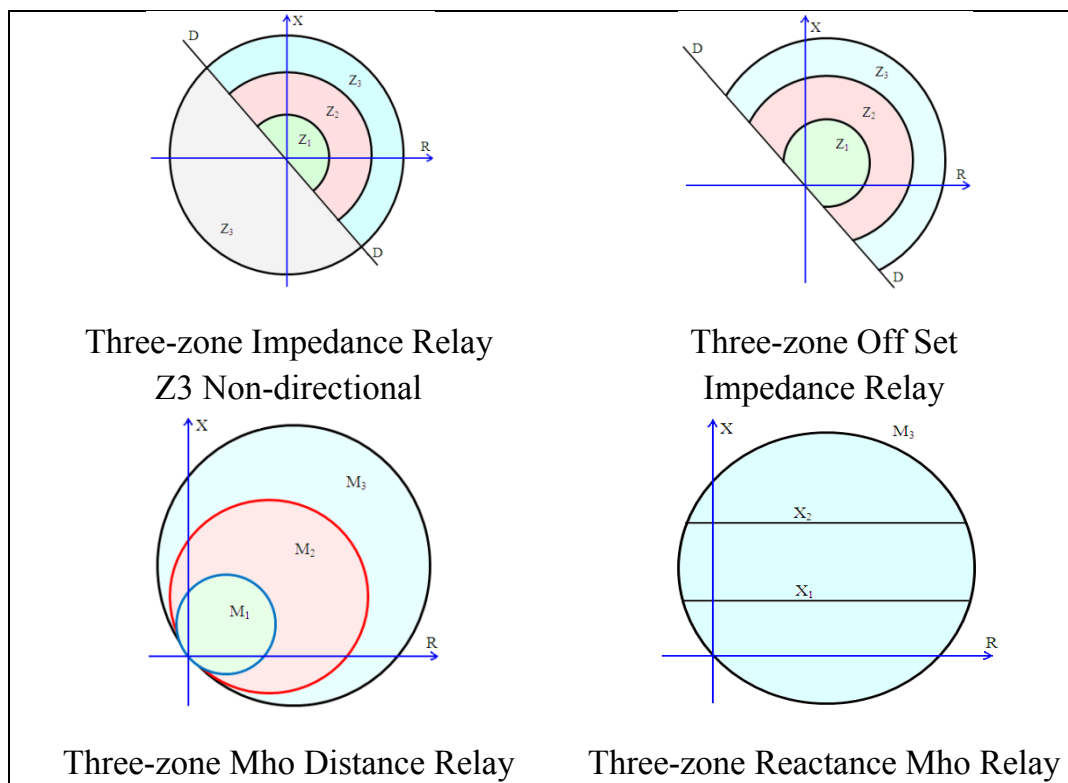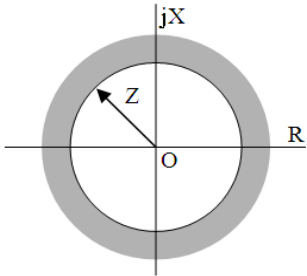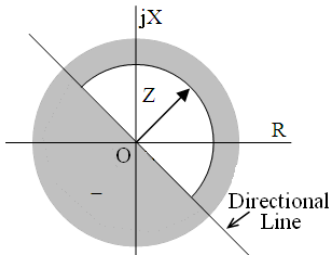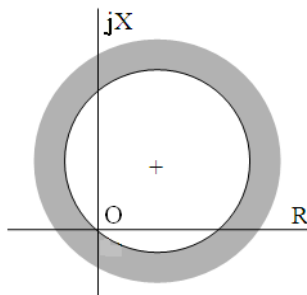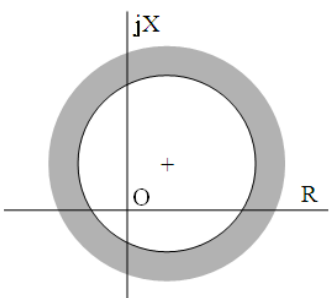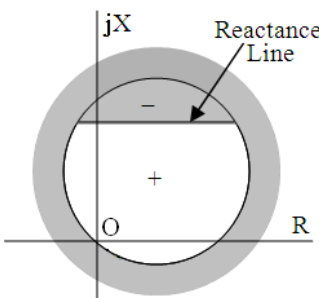
Fig. 2.2-19 Three-Zone Distance Relays

The distance relays at B have the same reach as the relays at A, but in the opposite direction. Typical R - X diagrams for three-zone distance relays are shown in Fig. 2.2-19. There are other various combinations of distance relay elements. Each one is designed to meet specific performance requirements.

COMPARISON BETWEEN DISTANCE RELAY CHARACTERISTICS

Type of Measurement	R-X Characteristics	Applications
Impedance		• Responds to faults on both sides of relay location. • Affected by arc resistance. • Affected by power swings. • Used for moderate lengths of line. • Operation within circle.
Directional Impedance		• Responds to faults in one direction only. • See above.
Mho Admittance*		• Stable for power swings. • Least affected by arc resistance. • Preferred for very long lines.
Off-set Mho		• Back-up for station bus bar. • For blocking main relay against power swings.
Reactance aided Mho Relay.		• For short lines in which arc resistance is important.
* Admittance is the reciprocal of impedance ($Y = 1/Z$), Mho is the inverse of Ohm letters		

Table 2.2-1 Distance Relay Characteristics

DISTANCE RELAYING SCHEMES

There are several alternative schemes to choose from. The schemes may be divided into the following three broad groups:

(1)   Distance schemes designed for phase faults only. Ground fault protection provided by overcurrent relays

(2)   None-switching schemes for phase faults as well as earth faults. Such schemes have separate distance relays for phase faults and earth faults. Thus, such schemes have several measuring elements fed with the corresponding values directly without the need of switching.

(3)   Switched schemes having one measuring element (for all kinds of fault) to which an appropriate measured quantity is applied (switched to) according to type of fault.

STARTING ELEMENTS FAULT DETECTOR

Starting elements (SE) are used with distance schemes having one or more measuring element (ME). SE will serve to switch the ME to correct input quantity depending on type of fault or to change distance steps or reversing the direction of measuring element after certain time lag.

The starting element may be:
- Overcurrent element
- Under-voltage element
- Impedance element

In the event of fault, the SE will operate first, and apply the secondary voltage and current to ME.

APPLICATION ON THREE PHASE DISTANCE RELAYS

DISTANCE RELAY TYPE KD

The type KD relay consists of three single air gap transformers (compensators), three tapped autotransformers, two cylinder type operating units, and an indicating contactor switch ICS.

Fig. 2.2-20 shows the AC voltage and current circuit schematics of the phase-to-phase portion of the Compensator Relay. The three-phase AC voltage at the relay location is connected to the relay potential coils through the secondary windings of the line drop compensators.
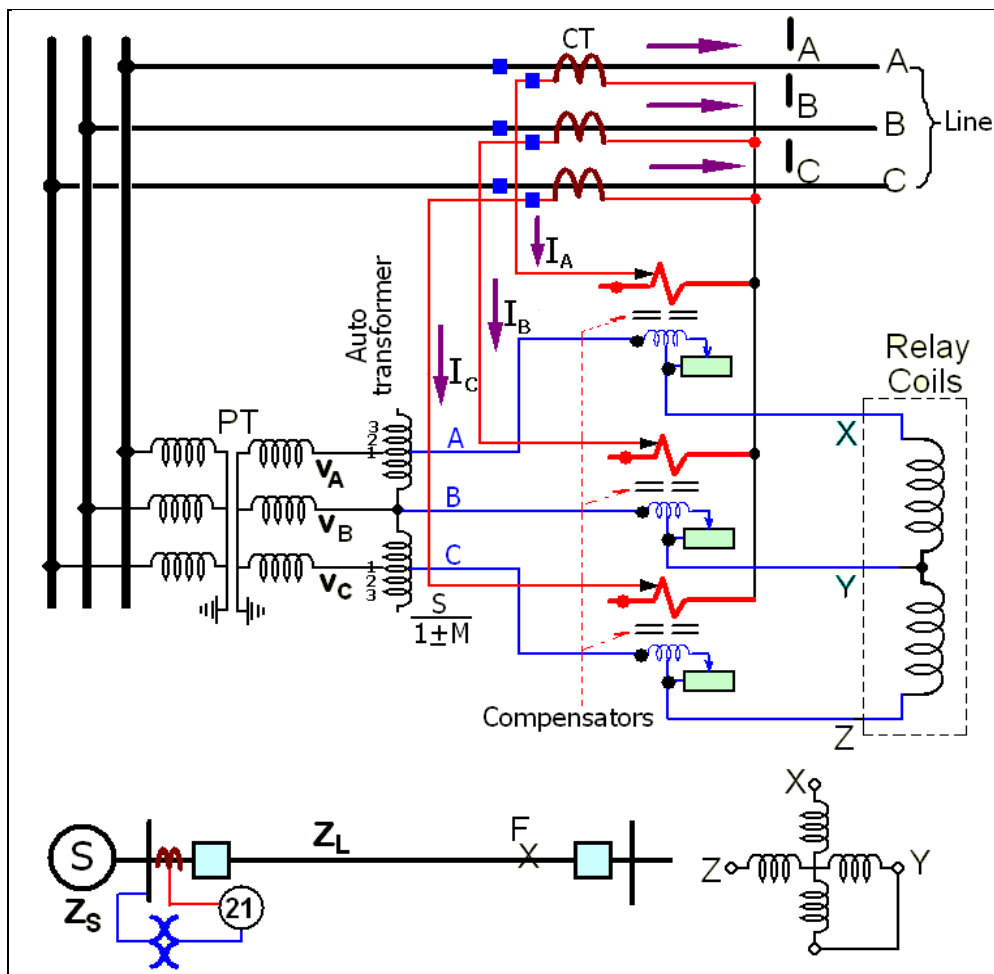
Fig. 2.2-20 Type KD Relay Phase-to-Phase Unit AC Connections

The primary windings of the line drop compensators are energized from the secondary windings of the line current transformers, as shown. Thus, the system voltages at points A, B and C are modified by the drop through the compensators to give the potential V_X, V_Y and V_Z at the terminals of the relay operating coils. The phase rotation of the voltage applied to the relay coils with no line current flowing is such that the relay has restraining torque on it and its contact is held open.

The mutual impedance of the compensators is set so that it is equal to the desired line balance point impedance in terms of secondary ohms. By means of a loading resistor connected across a portion of the secondary winding of the line drop compensator, the angle between the primary current and the secondary voltage of the compensator can be made equal to the angle of the protected line section. Consider a phase to phase (**BC)** fault beyond the relay balance point. Since there is a greater impedance drop between the fault location and the relay, the voltage triangle will not be collapsed as much as for the fault at the balance point. This condition is shown in Fig. 2.2-21(b). The collapsed voltage triangle is defined by **ABC**. The potentials are modified by the drops in the compensators in phases **B** and **C** to give the voltage triangle applied to the relay of **XYZ** rotation. This triangle has positive sequence rotation and the relay receives a restraining torque. Thus, the contact will not close for this fault, which is beyond the balance point of the relay.

(a) BC Fault Beyond Balance Point   (b) BC Fault Within Balance Point
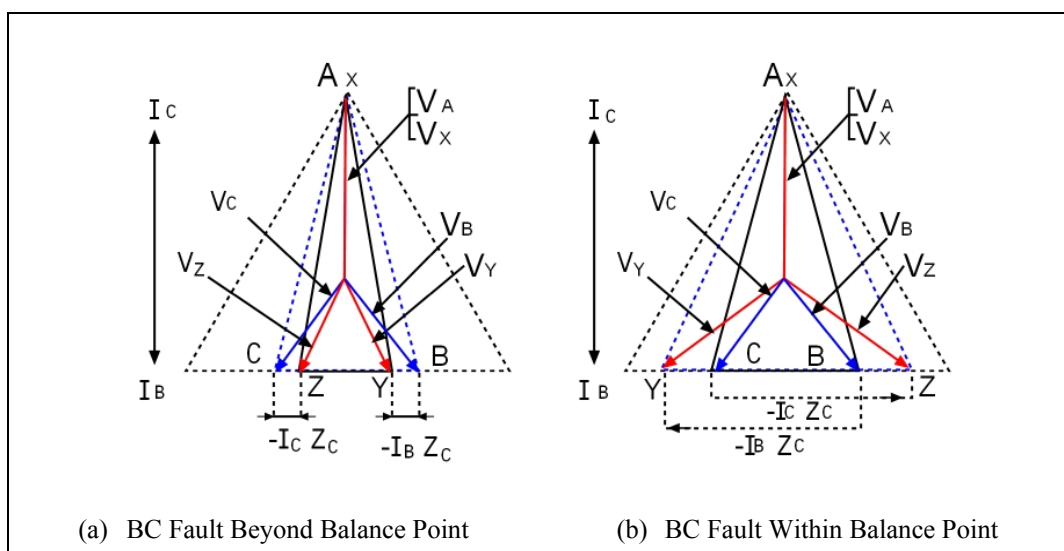
Fig. 2.2-21 Type KD Relay Phase-to-Phase Unit Voltage and Current Relationships for different Fault Conditions

If the fault is moved closer to the relay (within the balance point), the voltage conditions become, as shown in Fig. 2.2-21(c). The potential of point (**X**) coincides with that of point **A**. The compensator voltages subtract from the system voltages as before, but because of the smaller initial voltage at the relay location and the increased fault current magnitude, the positions of points (**YX)** and (**Z**) actually cross, thus giving us a triangle of voltage applied to the relay unit of phase rotation **XZY**.

This is a negative sequence phase rotation and the relay now has an operating torque to close its contact and complete the trip circuit.

KD THREE-PHASE UNIT

The second relay unit in the KD relaying system is the three-phase unit. The basic electrical circuit of this relay is shown in Fig. 2.2-22(a). The three-phase unit also uses a four-pole induction cylinder relay unit, but only a single compensator. This compensator is connected in series with the phase (**A**) voltage lead to the relay unit. Its primary is energized with the current, $(I_A - 3I_o)$. Phase (**B**) and phase (**C**) voltages are connected directly to points (**Y**) and (**Z**) , as shown in Fig. 2.2-22(a). The three-phase relay has a characteristic circle, which passes through the origin, as shown in Fig. 2.2-22(b).
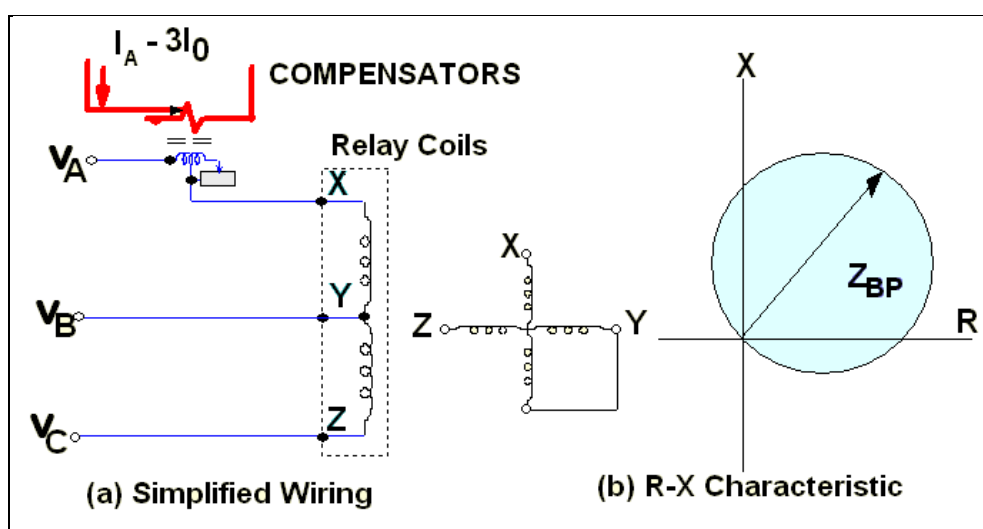
Fig. 2.2-22 Type KD Relay Three-Phase Unit

RELAY COMPONENTS

- Three-phase relay
- Single-phase operating unit
- Three auto transformers
- Line drop compensator (**T**) in the 3 phase unit
- Line drop compensator (**TAB**) and (**TBC**) in the phase-phase unit

- Tap plate
- Target and seal-in relay

As shown in Fig. 2.2-23 and 24, the compensator (**T**) is two-winding air gap transformer, it has one primary current winding. The compensator (**TAB**) and (**TBC**) are three winding air gap transformers having two primary current windings. Each primary winding has seven taps, which terminate at the tap block, as shown in Fig. 2.2-23a. The secondary winding has a single tap, which divides the winding into two sections.

| (a) Front View | (b) Rear View |
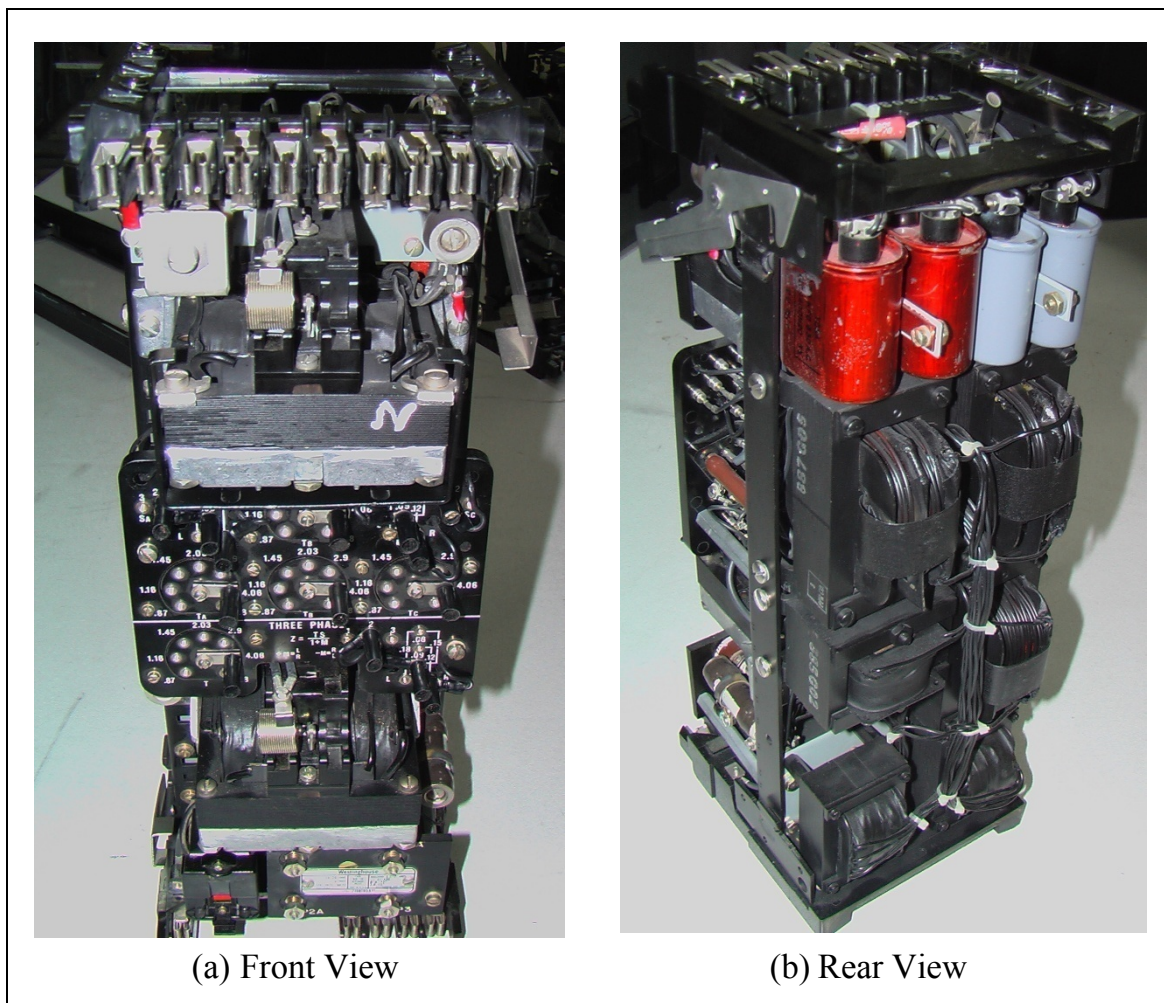
Fig. 2.2-23 Distance Relay Type KD-10

AUTO TRANSFORMER

The auto-transformer makes it possible to expand the basic range. Therefore, any relay ohm setting can be made within 1.5 percent from the desired value.

Simplified internal schematic of the Westinghouse KD-10 relay is shown in Fig. 2.2-24:

Minimum recommended electrical Tests:

- Insulation resistance test
- Auto transformer check
- Maximum torque angle verification
- Reach or impedance verification
- Target and seal-in relay operation
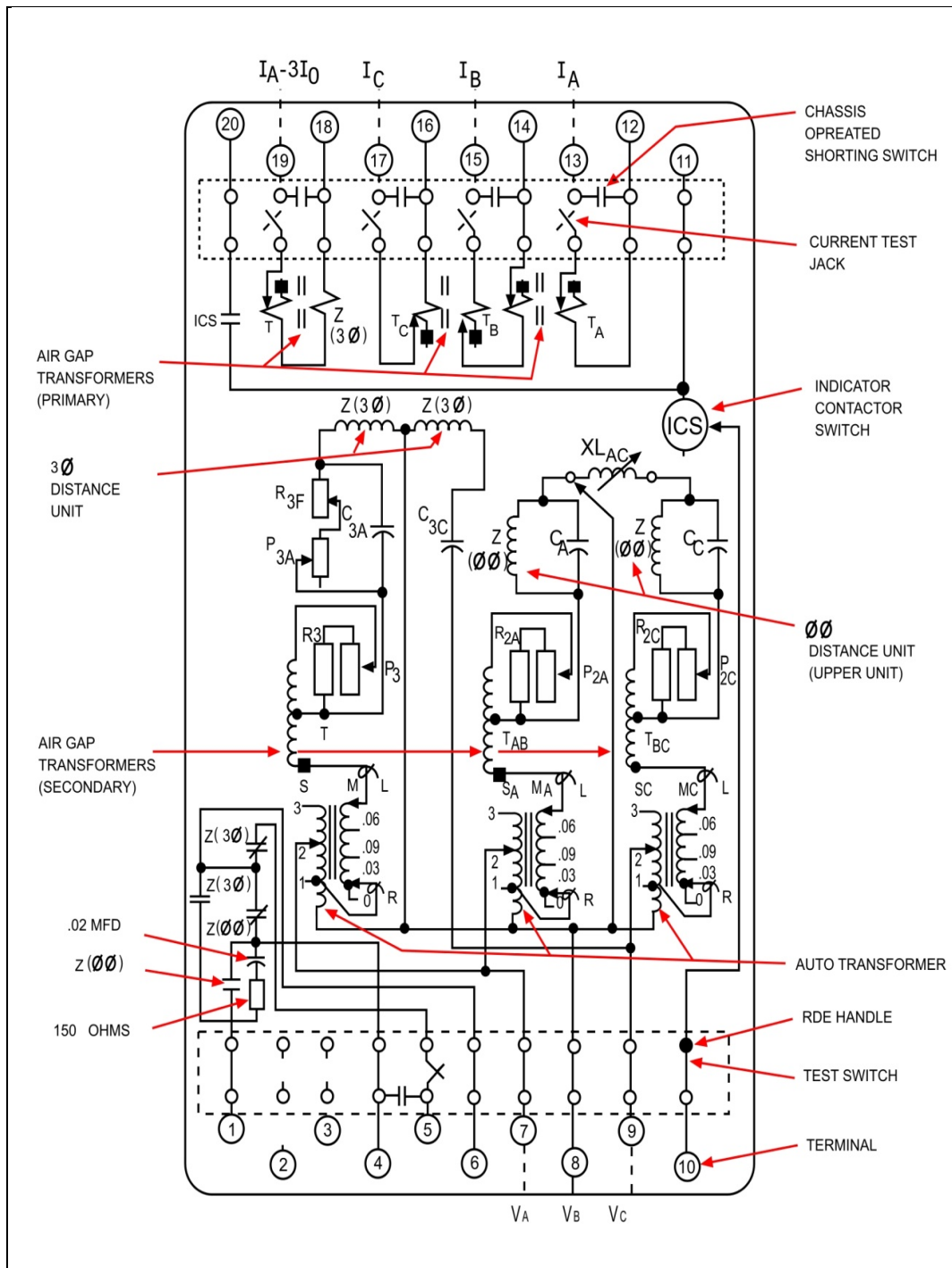
Fig. 2.2-24 Type KD-10 Relay Internal schematic
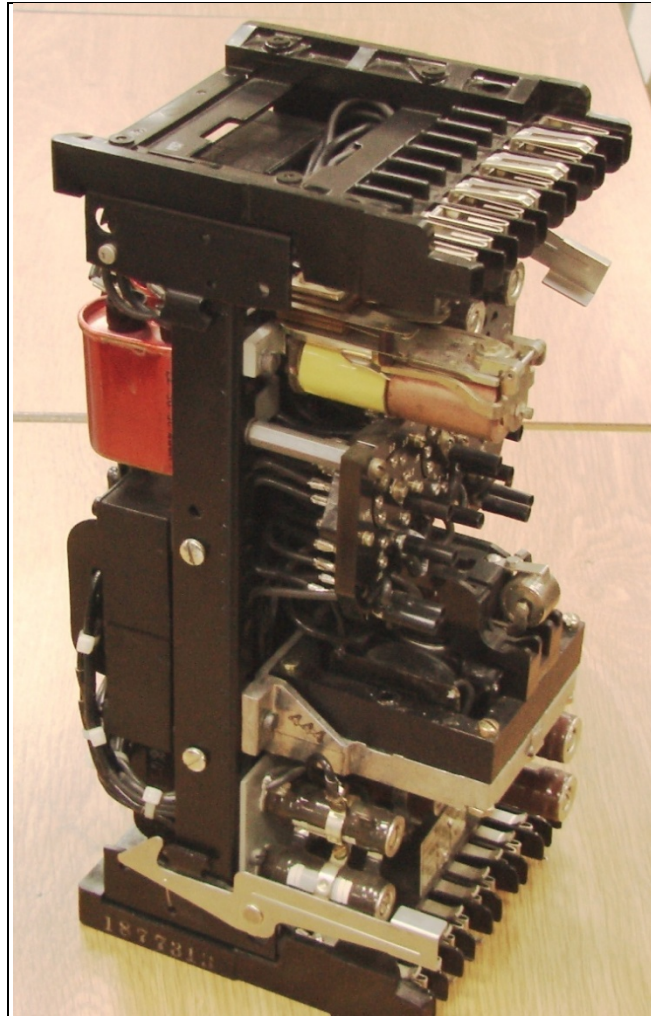
Fig. 2.2-25 Distance Relay Type KD-10

SUMMARY

- Distance protection is used to protect transmission lines.

- The line is divided into sections for coordination.

- Distance protection measures the impedance seen by the relay from the CT & VT location.

- Balanced beam relay divides voltage by current to determine line impedance.

- Distance relay operates according to certain characteristics selected according to TL configuration.

- Impedance characteristic is represented with a circle; its center in the origin of the R-X diagram.

- Mho characteristic is represented with a circle; its circumference passes through the origin of the R-X diagram.

- Offset Mho characteristic is represented with a circle; its center is shifted from the origin of the R-X diagram.

- Reactance characteristic is represented with a horizontal line intersects the X-axis on the R-X diagram.

- Directional unit is used with the impedance relay to determine direction of the fault if it is forward or reverse.

- Time coordination is set with the distance relay stages (2nd & 3rd).

FORMULAE

$V / I = Z_o$ (line impedance)

$K_1 I^2 > k_2 V^2$

For operation:

$V / I < \sqrt{(K_1 / K_2)}$ or $Z_o < \sqrt{(K_1 / K_2)}$

Where V & I are the secondary of VT and CT

GLOSSARY

Inoperative: Out of use

Adaptation: Adjustment to suit the requirement

Seesaw: Swing

Imposed: Forced

REVIEW EXERCISE

Circle the letter a, b, c or d that correctly completes the statement and follow the directions to answer the other questions:

1. The characteristics shown below represents …………………….....

a. Impedance element with directional control.

b. Mho distance element.

c. Reactance type relay.

d. Impedance relay.
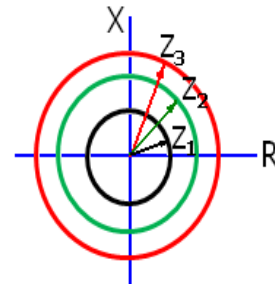
2. The characteristics shown below represents …………………….....

a. Mho distance element.

b. Impedance relay.

c. Impedance directional type relay.

d. 3-zones impedance relay.
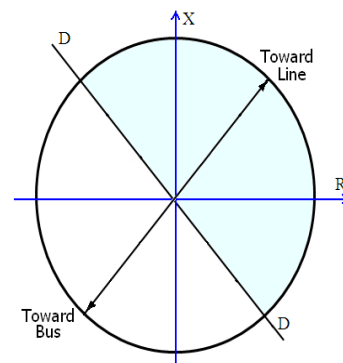
3. Disadvantage of impedance relay that:

a. It is affected by the arc resistance.

b. It is highly sensitive to power swing.

c. It is very fast in instantaneous operation.

d. Both a & b.

e. All of the above.

4. The reach of zone (3) is ……………………………… of the line.

a. 150 %

b. 90%

c. 120%

d. 100%

5. The reach of zone (1) is ………………………………… of the line.

    a. 100 %

    b. 80 - 90%

    c. 120-150%

    d. More than 150%

6. The characteristic shown below represents: ………………………

    a. 3-zone mho distance.

    b. Impedance relay.

    c. Offset impedance relay.

    d. Reactance element.
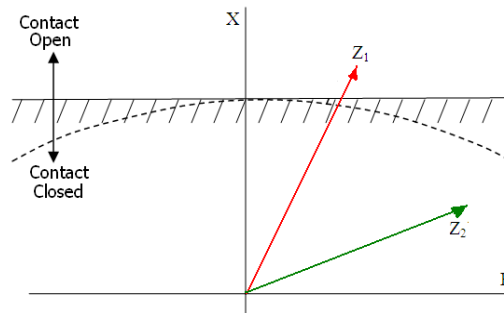
7. The characteristics shown below represents ………………………

    a. Mho distance element.

    b. Impedance relay.

    c. Reactance type relay.

    d. 2-zones impedance relay.
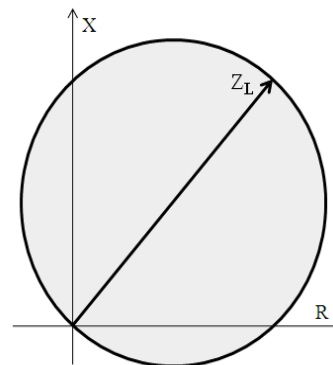
8. The best unit for the electromechanical Mho relay must be:

    a. Induction disc unit.

    b. Induction cup unit.

    c. Plunger type unit.

    d. Balanced beam type unit.

9. The best unit for the electromechanical impedance relay unit:

    a. Induction disc unit.

    b. Induction cup unit.

    c. Plunger type unit.

    d. Balanced beam type unit.

10. When a fault impedance vector lies in the 1st quadrant, it means that it lies in the:

   a. forward zones and the line has inductance.

   b. reverse zone and the line has inductance.

   c. forward zones and the line has capacitance.

   d. reverse zone and the line has capacitance.

11. When a fault impedance vector lies in the 2nd quadrant, it means that it lies in the:

   a. Forward zones and the line has inductance.

   b. Reverse zones and the line has inductance.

   c. Forward zones and the line has capacitance.

   d. Reverse zones and the line has capacitance.

12. When a fault impedance vector lies in the 3rd quadrant, it means that The fault lies in the:

   a. Forward zones and the line has inductance.

   b. Reverse zone and the line has inductance.

   c. Forward zones and the line has capacitance.

   d. Reverse zone and the line has capacitance.

13. When a fault impedance vector lies in the 4th quadrant, it means that it lies in the:

   a. forward zones and the line has inductance.

   b. reverse zone and the line has inductance.

   c. forward zones and the line has capacitance.

   d. reverse zone and the line has capacitance.

14. The start element depending on a voltage drop and over current to operate a distance relay is called: ………………………………………

   a. Over current element.

   b. Under voltage element.

   c. Impedance element.

   d. Directional impedance element.

15. The reactance type distance is preferred to protect TL when the:

    a. resistance is neglected compared to the line inductance.

    b. fault has accurse in the reverse zone.

    c. fault impedance is closed to load impedance.

    d. power swing is used to happen.

16. What is the function of air gap transformers in KD relay?

…………………………………………………………………………………………

…………………………………………………………………………………………

17. Study the network shown in the diagram below and fill the next table to show which relay(s) will start for the fault shown.
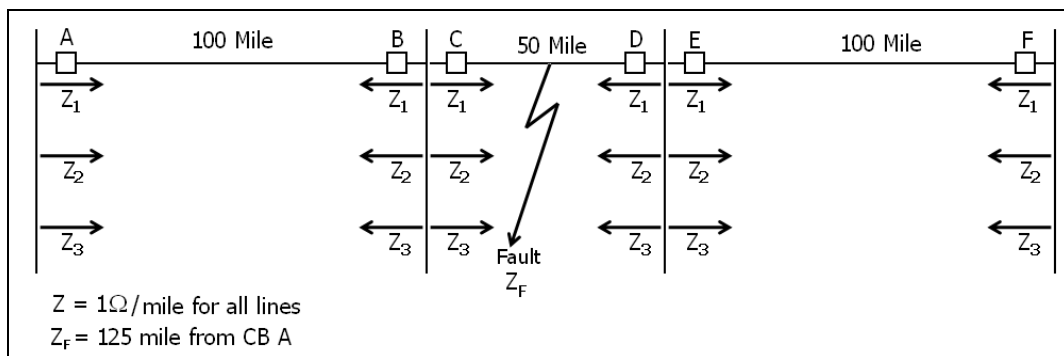
Circuit Breaker	Z_1	Z_2	Z_3
A			
B			
C			
D			
E			
F			

TASK 2.2-1

INSPECTION FOR THE PARTS OF DISTANCE RELAY TYPE KD-10

OBJECTIVES

Upon completion of this task, the trainees will be able to:

- Demonstrate an electomagnetic distance rekay, type KD-10

TOOLS, EQUIPMENT & MATERIALS

- Distance Relay, type KD-10
- Instruction manual
- Personal safety equipment as recommended in relay workshop.

PROCEDURE

1. Remove the relay from the casing carefully.
2. Identify and inspect the compensator (air gap transformers) for the following:
   - Three-winding air gap transformers (primary windings & the taps)
   - Two-winding air gap transformers.
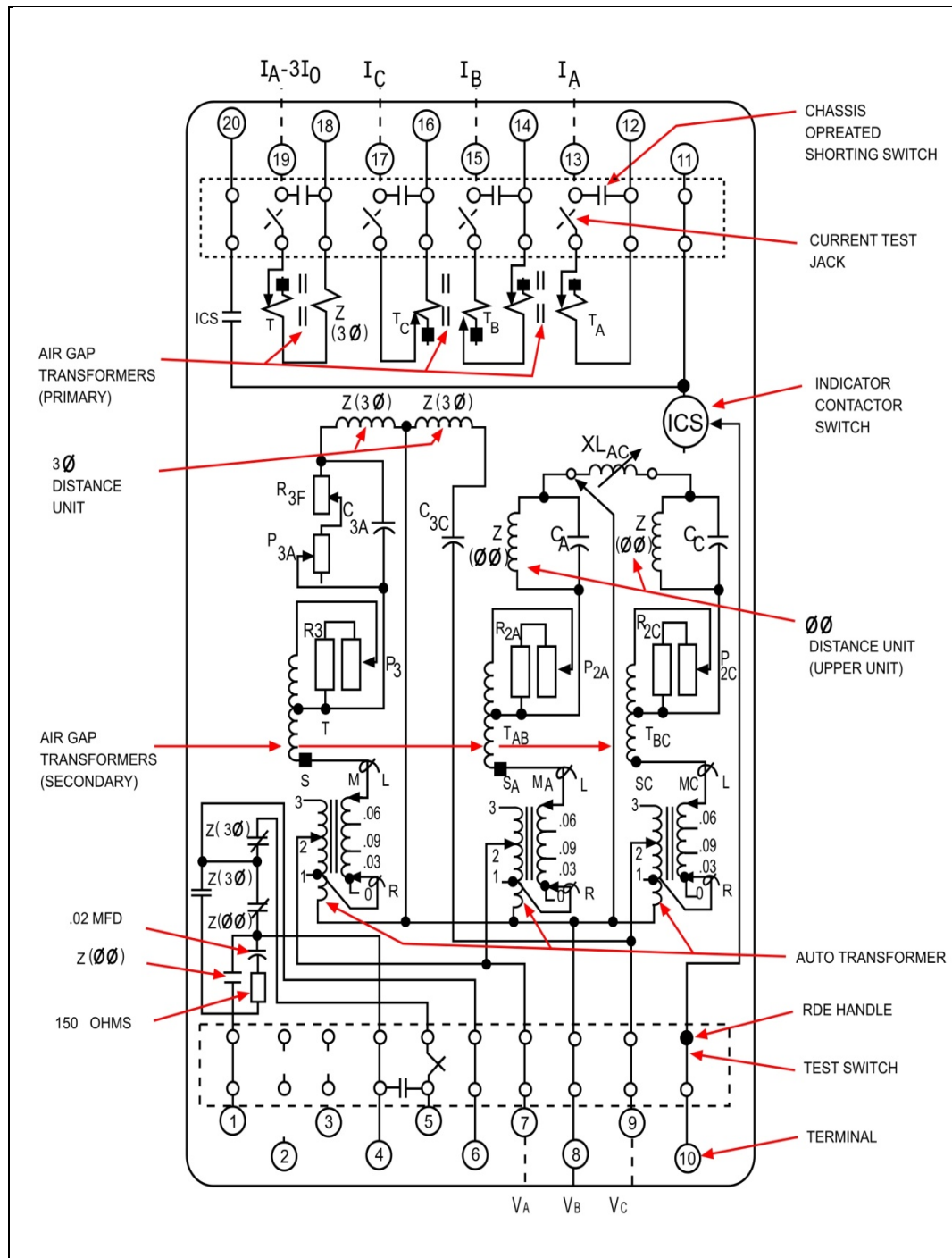
Fig. 1-1 Internal Schematic of KD-10 Relay

NOTE:

Compensator (air gap transformer)

TAB, TBC: Three winding air gap transformers, have two primary current windings.

TA: Two winding air gap transformers. It has one primary current winding.

3. Identify and inspect 3-phase and phase to phase distance unit.

4. Identify and inspect four-pole cylinder unit (trip initiator) for moving contact and stationary contact.

NOTE:

Tripping Unit: Cylinder with 4-pole initiate tripping. 4-pole connected open delta, contact closing torque is produced by the unit when the voltage applied to its terminals has a negative phase sequence.

Closing torque for the relay forces the moving contact to the left hand side as viewed from the front of the relay. Contact-opening torque is produced when positive-phase sequence voltages are applied.

The two electromagnets have two series-connected coils mounted diametrically opposite to one another to excite each set of poles.

The moving element assembly consists of a spiral spring, contact carrying member, and an aluminum cylinder.

The cylinder rotates in an air gap formed by the electromagnet and the magnetic core.
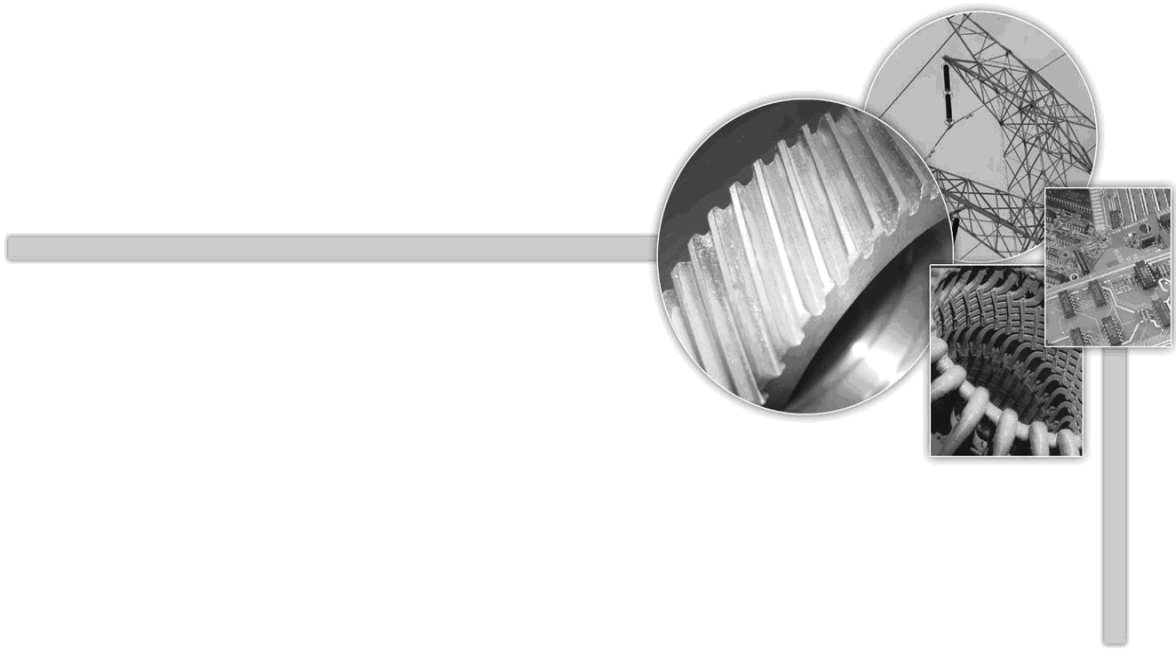
When the contacts close, the electrical connection is made through the stationary contact housing clamp to the moving contact through the spiral spring and out to the spring adjuster clamp.

5. Identify and inspect indicating contactor switch.

NOTE:

The indicating contactor switch is a small DC operated clapper type device. When the switch closes, the moving contacts bridge two stationary contacts, completing the trip circuit, and indicator target to drop. The target is reset from outside of the case by a push rod located at the bottom of the cover.

LESSON 2.3

OUT OF STEP RELAY

LESSON 2.3

OUT-OF-STEP RELAY

OVERVIEW

This lesson deals with the Out-Of-Step relays. Used for the protection of synchronous motors and to block the tripping for important transmission lines in case of power swing due to external faults.

OBJECTIVES

Upon completion of this lesson, the trainee will be able to:

- State the functions of out-of-step relay.

- Describe out-of-step blocking relaying.

- Demonstrate parts of KS type relay (out-of-step blocking relay).

Task 2.3-1: Identifying Out-of-Step relay type KS

INTRODUCTION

When a synchronous machine is subjected to a mechanical overload exceeding its maximum available torque output, it decelerates and is said to fall out of step or lose synchronism with the alternating supply to its stator. Loss of synchronism may also result from a fall in field current or supply voltage and if maintained, the machine will be subjected to undesirable overcurrent and pulsating torque, leading rapidly to stalling.

Swings of power system may cause out of step or out of synchronism when the load changes, by increasing or decreasing, or by faults. The swings or variations in current and voltage may cause unnecessary tripping of important transmission lines, unless some means were provided to prevent breaker trip-outs under these conditions. High speed distance relays are particularly susceptible to out-of-step power surges, and for this reason, out-of-step blocking relays are frequently used in conjunction with distance relays on the transmission lines.

OUT-OF-STEP RELAYS

The Out Of Step relay has device function number 68. When a phase-to-phase fault occurs within the first zone of a line protected by a three-step distance relay, all three-distance elements will close their contacts, simultaneously.

a) FOR SYNCHRONOUS MACHINES

The relay senses the change in power factor when the machine loses synchronism, and compares the phase (**A**) line current with the current caused by the voltage across phases (**B**) and (**C**).

The difference between phase (**A**) current and the current produced by the voltage across phases (**B**) and (**C**) is a relative phase angle of 90°, which gives a resultant current sufficient to operate relay element. Operation of that element allows the relay to be energized. When relay is energized a normally closed contact is opened to

prevent tripping of the synchronous motor. One normally open contact in the relay control circuit is closed to short-circuit part of a coil winding, thus giving a blocking to the trip circuit.

b) FOR TRANSMISSION LINE

When a system goes out-of-step, distance relays interpret the condition as a travelling three-phase fault. The three distance elements will close their contacts in sequence as the disturbance (decreasing load impedance) comes within their settings. These elements will reset in the opposite sequence as the disturbance (increasing load impedance) passes out of their settings. This change in load impedance occurs at a rate of speed much slower than the abrupt change in load impedance that occurs on a line fault. The time difference in the operation of impedance elements for these two conditions is used to discriminate between an out-of-step condition and a line fault. This is shown graphically in Fig. 2.3-1.
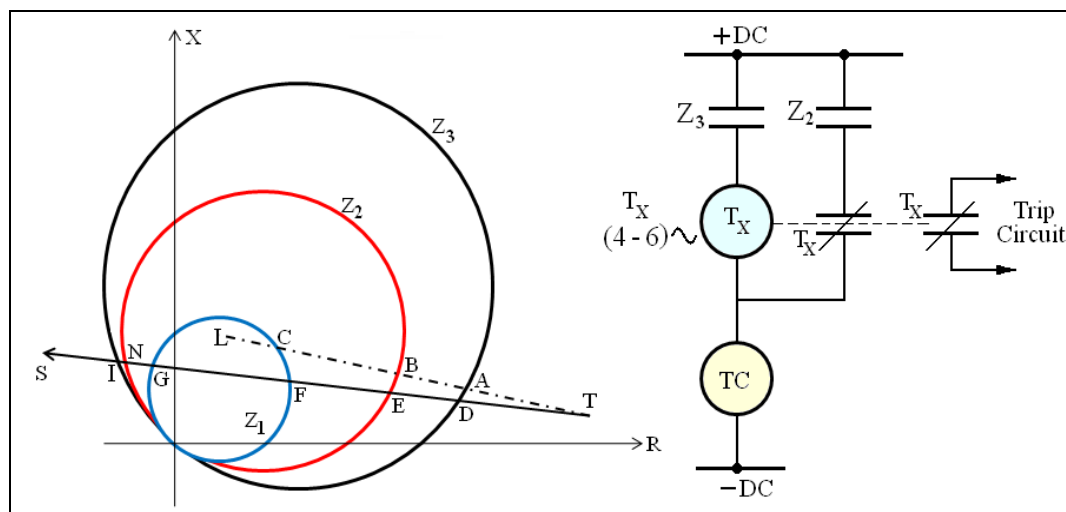
Fig. 2.3-1 Out-of-Step Blocking

A line fault at impedance point (**L**) will cause the load impedance to change from the normal load at point (**T**) to point (**L**) in an extremely short time. The impedance elements will close their contacts almost simultaneously as the impedance goes through the points A, B and C.

An out-of-step condition will cause an impedance change along some line such as TS. The change will traverse the three impedance zones, and the impedance elements will close their contacts in sequence as the impedance goes through points D, E and F. Likewise, the elements will open their contacts in sequence at points G, H, and I. When the surge swings back from S to T, a reverse action takes place.

The time interval between contact operations at D and E is very much greater than at A and B. The difference in time is the factor that permits discrimination between a fault and an out-of-step condition.

Out-of-step blocking is accomplished by several types of relay schemes. Some schemes make use of the distance relay elements; others contribute their own impedance element or elements. The out-of-step timing is accomplished by several different means to provide the desired discrimination and blocking.

A simplified version of an out-of-step blocking circuit is also shown in Fig. 2.3-1. On a line fault, contacts (Z_2) and (Z_3) close at the same time. The 'b' contacts of timer (T_X) do not open unless TX has been energized for a designated interval (usually four to six cycles). The coil of (T_X) is shunted by the contacts of Z_2 and T_X so the timer does not pick up, and tripping is permitted for a line fault.

For an out-of-step condition, contact (Z_3) closes first and timer (T_X) picks up before Contact (Z_2) closes. Operation of the timer opens the shunt circuit around the timer coil and it opens 'b' contact that prevents tripping of the breaker. When Contacts (Z_2) and (Z_3) open, the timer resets at once, ready for the next out-of-step swing.

OUT-OF-STEP RELAY TYPE KS

KS relay distance unit, (Z_{OS}), is set to include the ZP-3ϕ [21-2(3ϕ)] unit R-X diagram circle, as shown in Fig. 2.3-2. A minimum separation of two ohms is recommended between the (Z_{OS}) and ZP-3ϕ [21-2(3ϕ)] unit circles. This separation provides the means for distinguishing between 3-phase faults and out-of-step conditions. When a fault occurs on the protected line, the impedance seen by the relays changes suddenly from the pre-fault value, (Z_{Load}), to the fault value, represented by the line (**O-F**).

When a swing or out-of-step condition occurs, the impedance seen by Z_{OS} & ZP (21) changes gradually, as the voltage decreases. As the current increases as shown, the swing describes an arc that intersects the Z_{OS} circle at point Q, and ZP-3ϕ circle at point P.
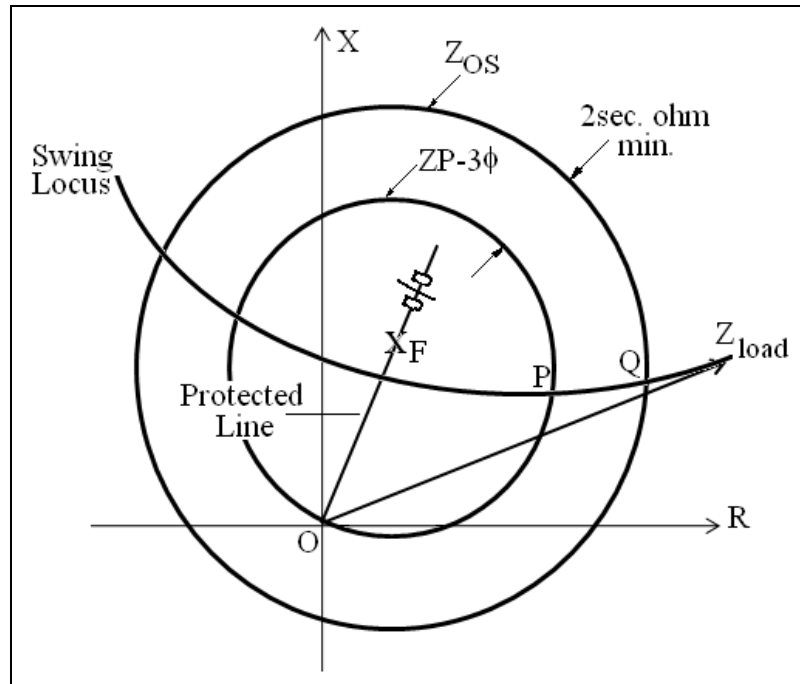
Fig. 2.3-2 Out-of-Step Relay Characteristic on R-X Diagram
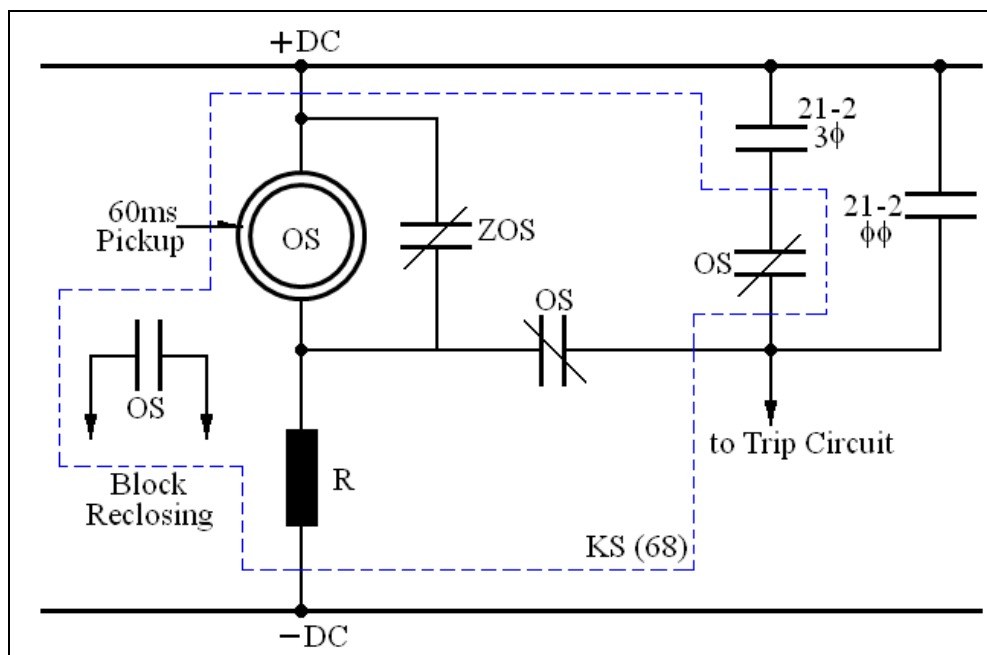
Fig. 2.3-3 Out-of-Step Blocking Circuit Operations

During an Out-Of-Step condition the contact ($\mathbf{Z_{OS}}$) in Fig. 2.3-3 opens before ZP-3ϕ (21-3ϕ) contact closes. unit (**OS**) is energized and, after 4 cycles, (**OS**) contact opens the ZP-3ϕ (21-3ϕ) trip circuit. All this occurs before the swing reaches point P in Fig. 2.3-2.
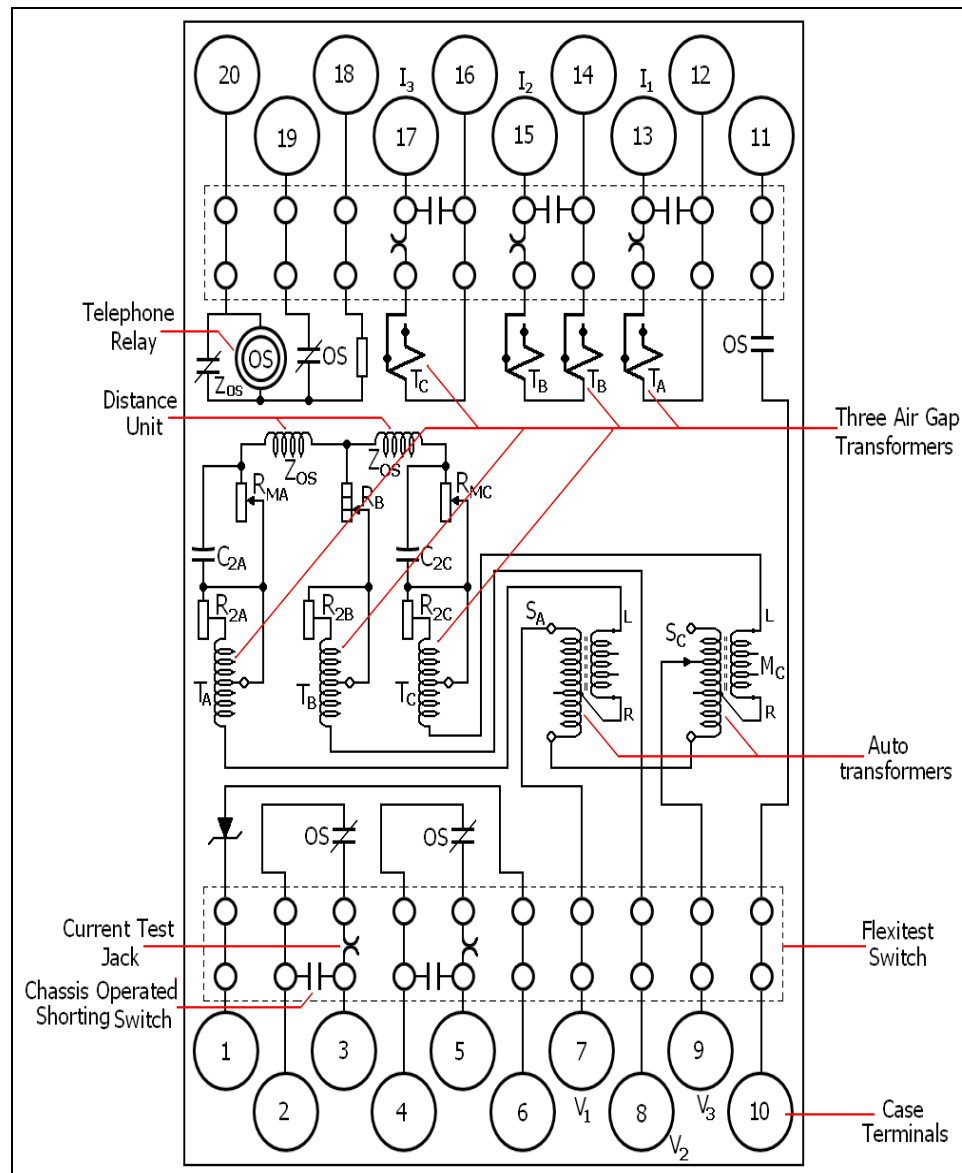
Fig. 2.3-4 Out-Of-Step Relay Internal Connection Diagram

CONSTRUCTION OF RELAY (KS)

The blocking relay type (KS) mainly uses induction cup, as shown in Fig. 2.3-5

| (a) Front View | (b) Rear View |
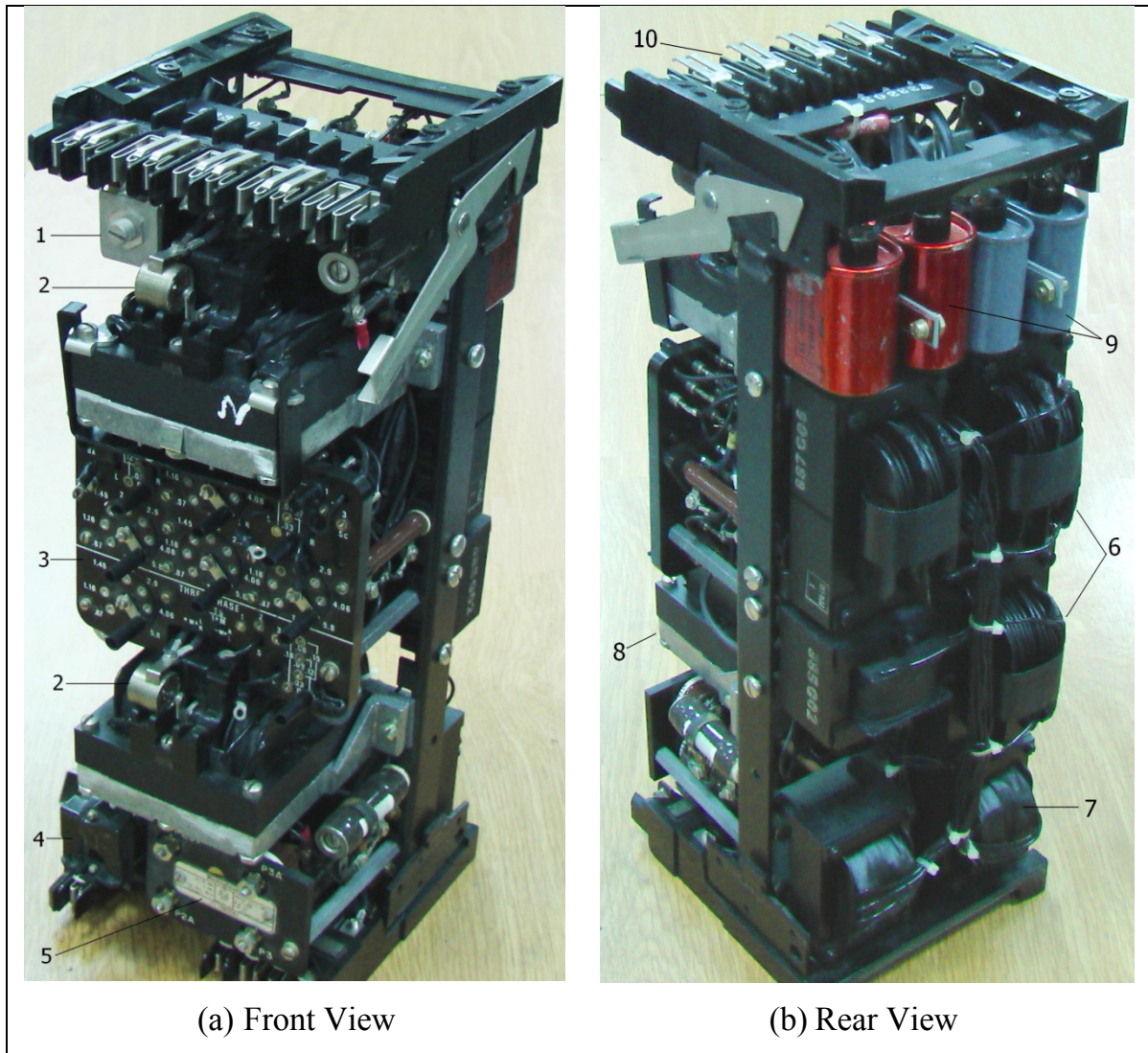
Fig. 2.3-5 Out Of Step Relay Type KS

1	Telephone type relay	2	Cylinder type operating unit
3	Tap plates.	4	Seal-in unit.
5	Name plate.	6	Air gap transformers.
7	Auto transformers.	8	Induction cup unit.
9	Capacitors.	10	Relay Terminals.

The three air gap transformer (compensators) are designated T_A, T_B - T_B, and T_C. The current winding of each compensator has seven taps, which terminate on the tap plate. The compensators provide sensitivity in the case of Out-Of-Step conditions. The autotransformer has three taps on the main winding(s), which are numbered 1, 2 and 3 on the tap block, and winding (M) has four taps, (Fig. 2.3-4). The cylinder unit initiates the blocking. When contacts ($\mathbf{Z_{OS}}$) close, the electrical connection is made through the stationary contact housing clamp to the moving contact through the spiral spring out to the spring adjuster clamp to short-circuit the telephone type relay coil, (**OS**). When operating torque causes the contacts to open, then the short-circuit is removed from across (OS) permitting it to be energized.

Telephone Type Relay: The telephone type relay unit, (OS) is a clapper unit the delay in operation is obtained by a copper slug, which acts as a lag coil and delays the build up of magnetic lines of force in the core. When the telephone relay is energized, by the opening of the cylinder unit contacts, it opens its several sets of contacts, which are normally connected in series with the KD relay three phase unit contacts and thus prevents completing the trip circuit during an out-of-step condition.

OPERATION OF KS-RELAY

A fundamental difference between a three-phase fault and an out-of-step or out-of-synchronism condition is that a fault suddenly reduces the voltage and increases the current; whereas during an out-of-step condition the voltage and current changes are comparatively gradual. When the line impedance to the apparent fault ($\mathbf{Z_F}$) is less than the compensator setting ($\mathbf{Z_C}$), ($\mathbf{I_{ZC}}$) becomes greater than the line voltage drop to the fault. This reverses the compensated voltage and thereby reverses the phase sequence of the voltage applied to the relay, and contact-opening torque is produced in the cylinder unit. Under out-of-step conditions, the apparent impedance measured by the relay anywhere near the electrical center starts at a high value, gradually decreases to a much lower value, and then gradually increases again to a higher value, and thus the system goes through a complete one oscillation. On the other hand, if the disturbance

is a fault, the impedance seen by the relay will suddenly drop to a much lower value, and then either retains this value or slightly increases due to the effects of fault resistance until the fault is cleared. The KS relay takes advantage of the distinction between a fault and an out-of-step condition. Under out-of-step conditions, the KS relay will operate, followed after a short time delay by the KD relay of Zone 2, as the apparent short circuit drifts toward the relay. In case of a fault, the KS as well as one or two zone relays will operate. If more than the KS relay is to operate, the others will operate within a very short time, and will not follow the sequence described for an out-of-step condition.

BLOCKING UNIT

The device to initiate blocking is a four-pole cylinder unit, which is connected open delta and operates as a three-phase induction motor. Contact-closing torque is produced by the unit when the voltage applied to its terminals has a positive phase sequence. The cylinder unit then has restraint or operating torque as determined by the phase sequence applied to its terminals.
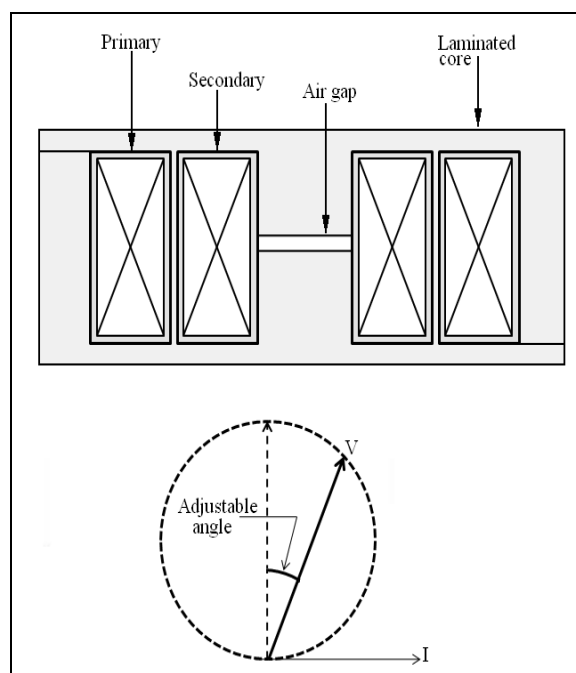
Fig. 2.3-6 Compensator Construction

THE COMPENSATORS

Sensitivity to the out-of-step condition is provided by compensators designated as T_A, T_B, and T_C. Each compensator is proportioned so that its mutual impedance (Z_C), has known and adjustable values. Compensator mutual impedance ($\mathbf{Z_C}$) is defined as the ratio of secondary induced voltage to primary current. The secondary (voltage) winding of the compensator is in series with the applied voltage and vectorially subtracts a value from the applied voltage, which is proportional to I_{ZC} where I is the relay current.

When the line impedance to the electrical center or to a fault ($\mathbf{Z_F}$) is less than the compensator setting ($\mathbf{Z_C}$), I_{ZC} becomes greater than the line voltage drop to the electrical center of fault. This reverses the phase sequence of the voltage applied to the relay, and a contact-closing torque is produced in the cylinder unit.

CHARACTERISTICS OF (KS) RELAY

Referring to Fig. 2.3-2. The impedance circle of the relay is set to encircle the second zone KD relay three-phase unit. The difference between the two circles provides a margin on ohms sufficient to give the telephone-type relay time to operate before the swing condition enters the characteristic of zone after having entered the circle of the KS relay. The telephone-type relay will open within 3 to 4 cycles. Thus all of the (**OS**) contacts operate to block tripping, and also to prevent the short-circuiting and de-energizing the (**OS**) coil as the zone 2 contacts close. When zone 2 operates before OS, as it does for a three-phase fault condition, a short-circuit across the coil OS is completed through the KD relay, and (**OS**) is not energized even through the ($\mathbf{Z_{OS}}$) contacts do open.
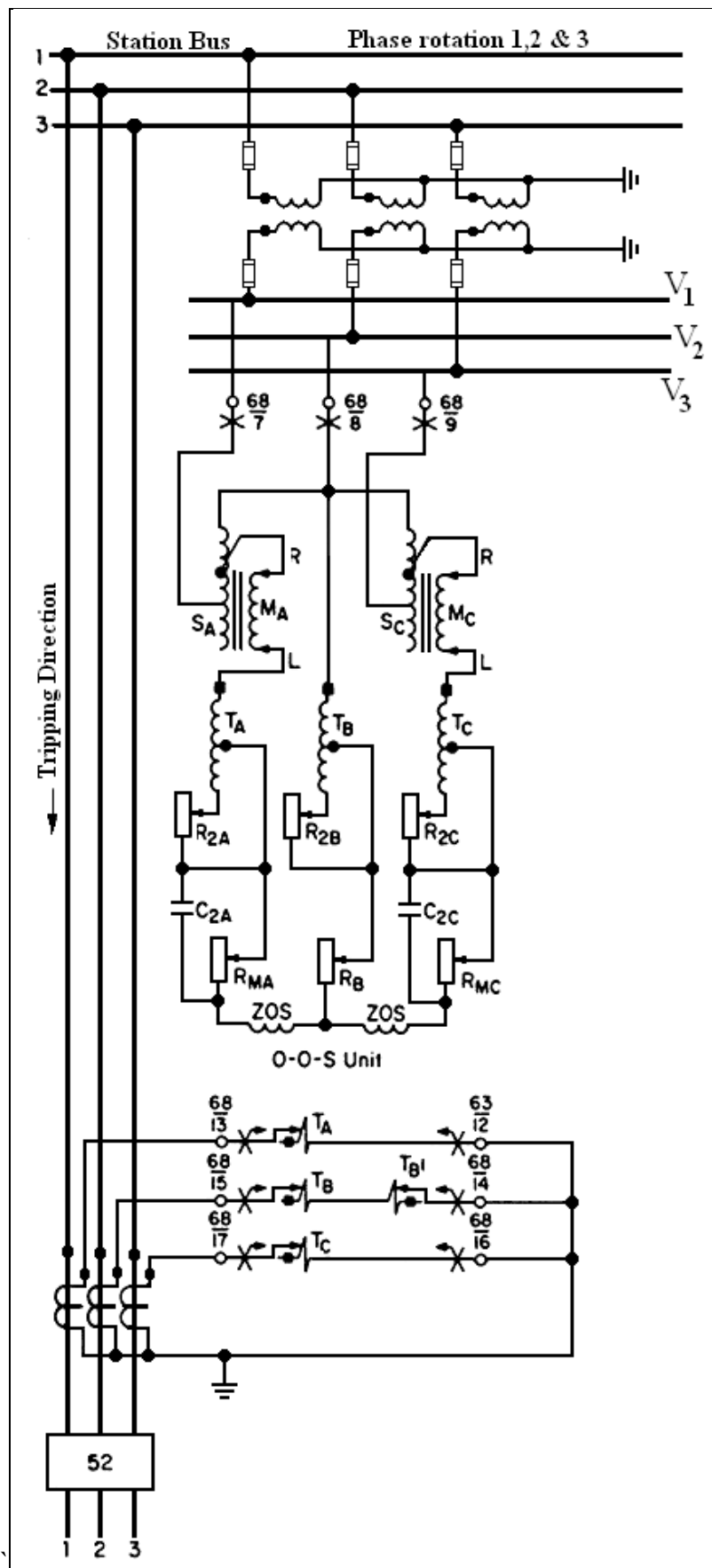
Fig. 2.3-7 External Wiring of KS Relay

ITEM	DESCRIPTION
Z_{OS}	Two element adjustable coils:
R_{MA} & R_{MC}	adjustable resistor.
R_B	adjustable taps resistor
R_{2A}, R_{2B}, R_{2C}	adjustable resistors
C_{2A}, C_{2C}	capacitors
T_A, T_C	Compensator (primary taps – 87; 1.16; 3; 2.2; 3.0; 4.2; 5.8)
T_B-T_B	Compensator (primary taps – TB = 2.85; 3; 4.95; TB = 0; -15; -3; -45; -6; -75; -9)
S_A, S_C	Auto-transformer (primary taps – 1; 2; 3)
M_A, M_C	Auttransformer (secondary between taps -0.0" .03; .06; .06)
OS	Telephone type relay

Table 2.3-1 Nomenclature for type KS relay

SUMMARY

- Out Of Step occurs when synchronous motor is subjected to mechanical overload.

- Out Of Step relay has device function number of 68.

- Out Of Step relay makes blocking to the protection trip circuit to prevent interruption to the important transmission lines.

- Out Of Step relay has two inputs, phase current from CT and line voltage from VT.

- Out Of Step relay senses the change in power factor when the motor loses synchronism.

- The relay compares the phase A current with the current caused by the voltage across phases B and C.

- The difference between phase A current and the current produced by the voltage across phases B and C is a relative phase angle of 90°, which gives a resultant current sufficient to make normally closed contact opens.

GLOSSARY

Lose synchronism:	Decrease synchronous motor speed.
Stall:	Tend to stop
Pulsating torque:	Unstable rotation.
Simultaneously:	At the same time
Slug:	Portable metal core to change coil inductance

REVIEW EXERCISE

Circle the correct answer for each of the following:

1. Out-Of-Step blocking relay is used in conjunction with ………………………….
    a. Under-voltage protection
    b. Overcurrent none directional only
    c. Distance protection
    d. Differential protection

2. In the figure shown below, what is the purpose of the 2 Ohms difference between the two circles?
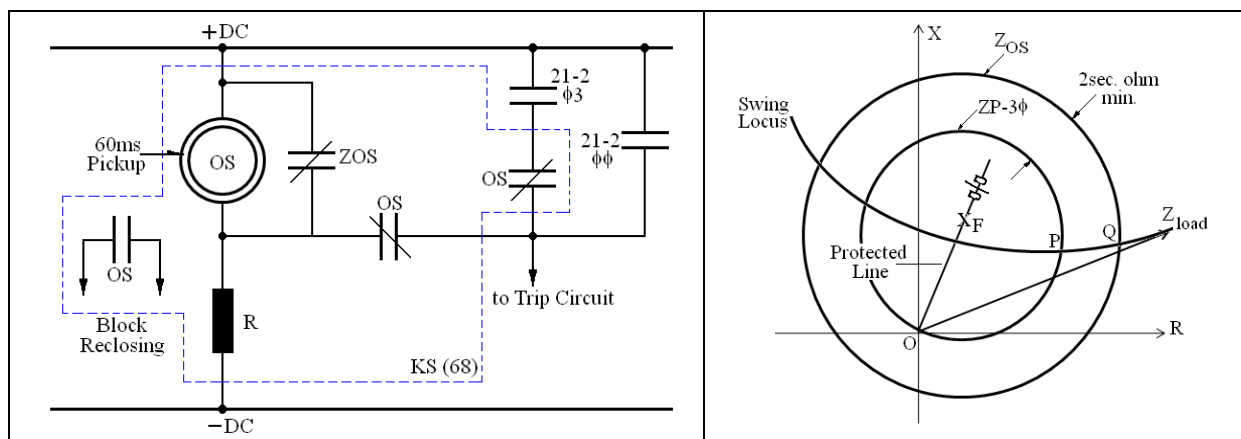
    a. For distinguishing between 3-Φ fault and out-of-step condition
    b. To protect the line from phase to phase fault
    c. To protect the line from 3-Φ fault
    d. All of the above

3. During ………………………. condition (Z_{OS}) contact opens before Z_P-3Φ (21-3Φ) contact closes to open the trip circuit of Z_P-3Φ (21-3Φ).
    a. Φ-Φ fault
    b. 3-Φ fault
    c. Out-of-Step
    d. All of the above

4. In the fault condition $\mathbf{Z_P}$-**3Φ** (**21-3Φ**) contact closes almost _____$\mathbf{Z_{OS}}$ opens.

   a. At the same instant that

   b. Before

   c. After

   d. None of the above

5. During fault condition, the voltage and current changes _____.

   a. Suddenly

   b. Gradually

   c. The voltage gradually but the current suddenly

   d. The current suddenly but the voltage gradually

6. During Out-of-Step condition, the voltage and current change _____.

   a. Gradually

   b. Suddenly

   c. Suddenly for voltage only

   d. Suddenly for current only

7. Air gap transformers are used in **KS** relays to _____ to Out-of-Step condition

   a. Provide power supply

   b. Increase the voltage of relay

   c. Provide sensitivity

   d. All of the above

8. Out-Of-Step blocking relay is used to _____ during out-of-step condition

   a. Provide tripping

   b. Prevent tripping

   c. Isolate circuit breaker feeding the line

   d. Isolate current and voltage transformers

Study the wiring diagram for KS relay shown below then answer the questions:

9. What are T_A, T_C and T_B, T_B'?

   a. Distance units

   b. air gap transformers

   c. autotransformers

   d. telephone relays

10. What are S_A and S_C?

   a. air gap transformers primary taps

   b. autotransformer primary taps

   c. current transformers

   d. potential transformers

11. What are M_A and M_C?

   a. air gap transformer secondary

   b. autotransformer secondary taps

   c. telephone relay primary

   d. None of the above

12. What are the voltage terminals?

   a. 13, 15 and 17

   b. 12, 14 and 16

   c. 7, 8 and 9

   a. 1, 2 and 3

13. What are the current terminals?

   a. 13, 15 and 17

   b. 12, 14 and 16

   c. 7, 8 and 9

   d. Both a & b
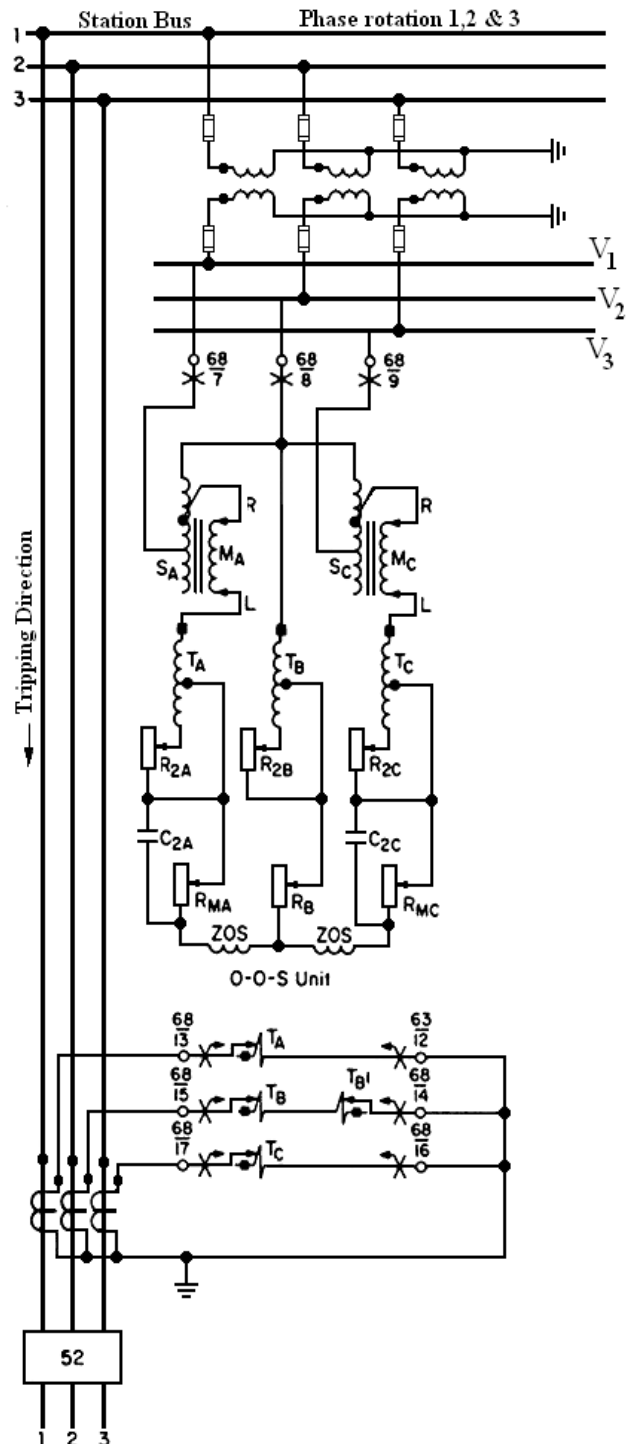
Task 2.3-1

OUT OF STEP RELAY TYPE KS

OBJECTIVES

After completion of this task, the participants will be able to:

- Identify the parts of Out of Step relay type KS.

TOOLS, EQUIPMENT & MATERIALS

- Out Of Step relay type KS.
- Instruction manual.
- Personal safety equipment as recommended in relay workshop.

PROCEDURE

1. Remove the relay after releasing the latches.

2. Identify and inspect the telephone relay-out-of step time delay type.

3. Identify and inspect cylinder unit including:
4. moving contact
5. stationary contact
6. induction cylinder

7. Identify and inspect air gap transformers including primary taps, and tap plate.

8. Identify and inspect the autotransformer including main winding taps and secondary winding taps.

9. Identify the terminals for voltage and current.
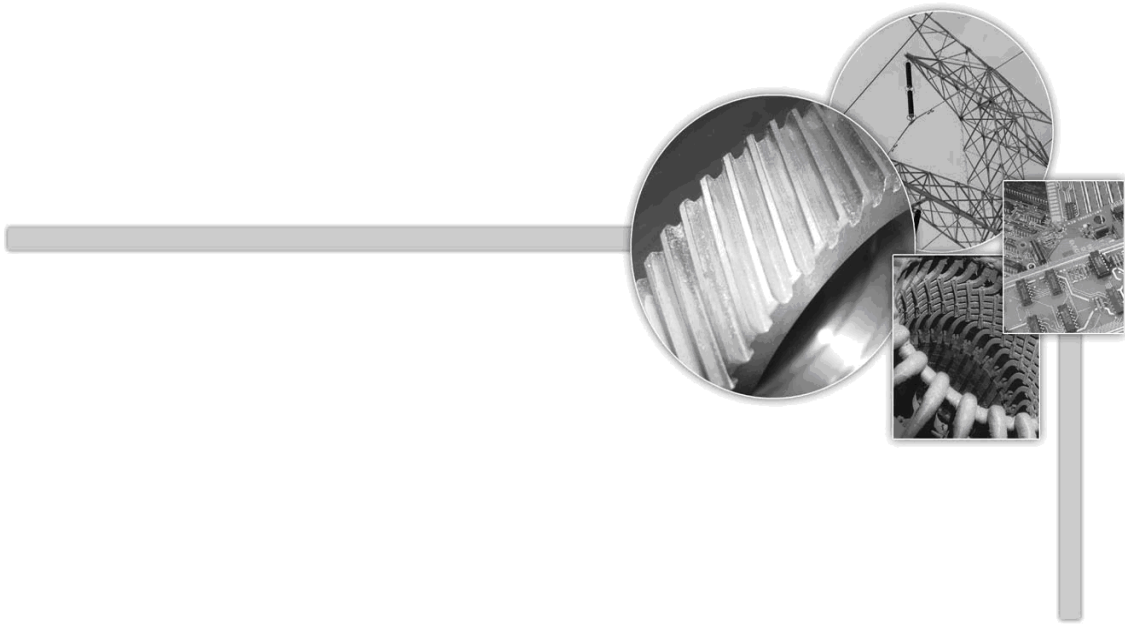
LESSON 2.4

GROUND FAULT PROTECTION

LESSON 2.4

GROUND FAULT PROTECTION

OVERVIEW

Thise lesson discusses the ground fault, its causes and how to detect it. The protection against ground fault is also covered in this lesson.

OBJECTIVES

Upon completion of this lesson, the trainee will be able to:

1. State the methods of detecting earth faults.

2. Explain and draw schematics of earth fault protections.

3. Explain and draw schematics of nondirectional O/C ground fault protection.

4. Explain and draw schematics of directional O/C ground fault protection.

INTRODUCTION

Ground faults occur because of failure in the insulation system so that the current returns to the source by a path, such as the conduit, or the building piping or steel frame, rather than via the normal conductor. The causes include such conditions as damaged conductor, loose connections, moisture, dust, etc. and these most commonly create an arcing ground fault.

GROUND FAULT PROTECTION

The single phase-to-ground fault is the most common type of fault that occurs on transmission lines. Protection from this fault requires understanding of ground relay operation and ground relaying schemes.

DETECTION

Current transformers are utilized to detect ground fault current. Its connections include:

   a)   Conventional connection
   b)   Zero sequence connection
   c)   Source neutral

A) Conventional Connected CTs

Residually connected current transformers are shown in Fig. 2.4-1. This method is widely used to protect medium-voltage systems.

This common, or residual, connection measures the vector summation of the phase conductor currents (3 for 3-phase 3-wire systems and 4 for 4-wire systems incorporating any loads connected line-to-neutral). No current flows in the residual

connection under normal conditions, which can include phase-to-phase or phase-to-neutral faults, since the net output of the 3 (or 4) current transformers is zero.

(a) Three CTs in the Protected Circuit   (b) One CT in the Ground Neutral Circuit
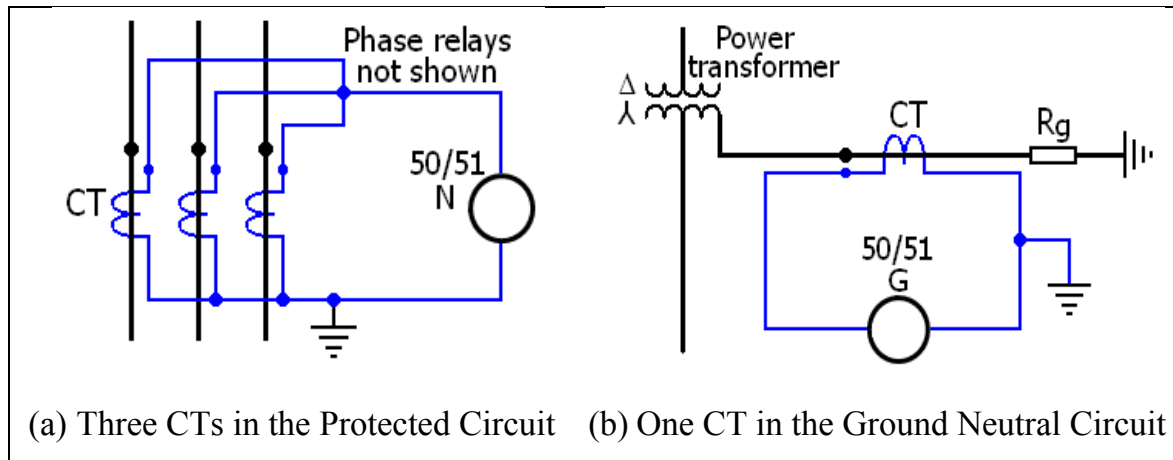
Fig. 2.4-1 Ground Protection with Conventional Current Transformers

The occurrence of a ground fault means that some current is delivered through the CTs from the power source but does not return through one of the conductors; the vector sum of the currents is not zero; current flows in the residual connection, and the ground fault relay is activated. The sensitivity of residually connected relay is determined by the CT ratio and relay pickup setting.

B) Zero Sequence (Core Balance CT)

The zero sequence current transformer, window-type CT or core balance CT includes only a secondary winding on an iron core, and the active conductors constitutes a single-turn primary winding. All phase (and the neutral of 3-phase 4-wire system) conductors must pass through the transformer core opening.

The principle of the core-balance current transformer circuit is shown in Fig. 2.4-2. The main conductors pass through the same opening in the current transformer and are surrounded by the same magnetic core.

Under normal conditions, that is, balanced, unbalanced, or single-phase load currents (if all conductors are properly enclosed), all currents flow out and return through the current transformer. The net flux produced in the current transformer core will be zero

---

and no current will flow in the ground relay. When a ground-fault occurs, the ground fault current returns through the equipment grounding circuit conductor (and possibly other ground paths) bypassing the current transformer. The flux produced in the current transformer core is proportional to the ground-fault current, and proportional current flows in the relay circuit. Relays connected to core-balance current transformers can be made quite sensitive.
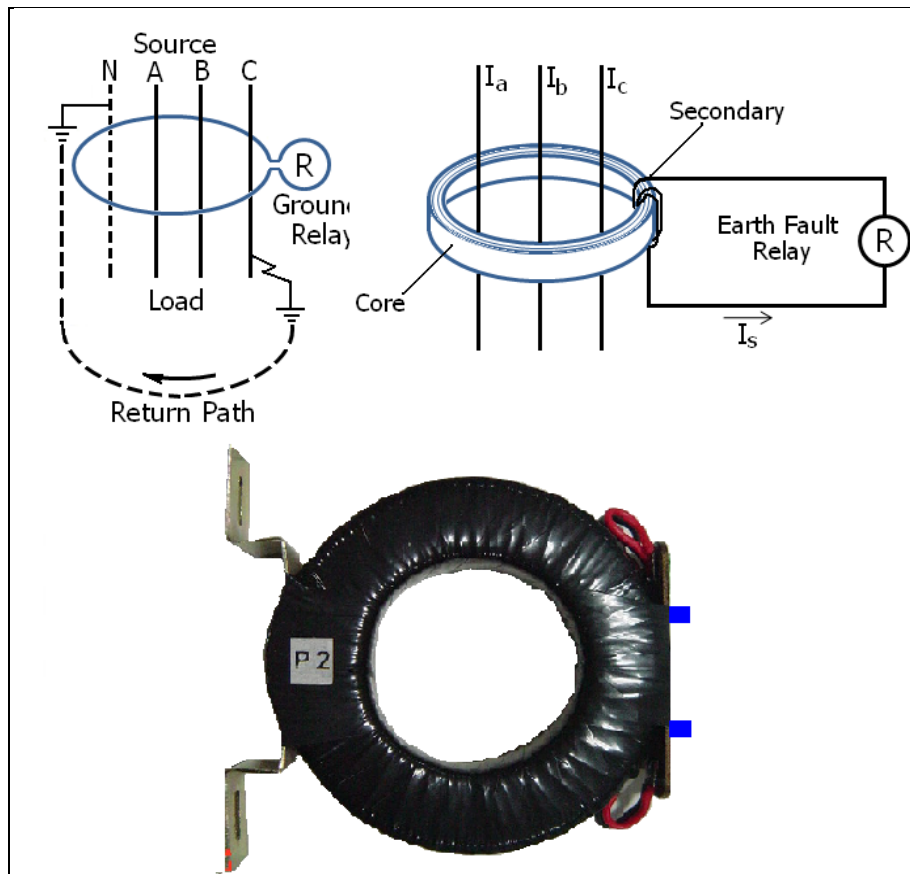
Fig. 2.4-2 Core-Balance Current Transformer

C) Source Neutral

The source ground current transformer is generally located in the system where the system ground is connected to the transformer neutral but where the normal neutral load current does not flow. The source ground current transformer circuit is shown in Fig. 2.4-3. The CT monitors only the ground fault current but since there is only one system ground location it must respond to ground fault occurring anywhere down-stream in the system.
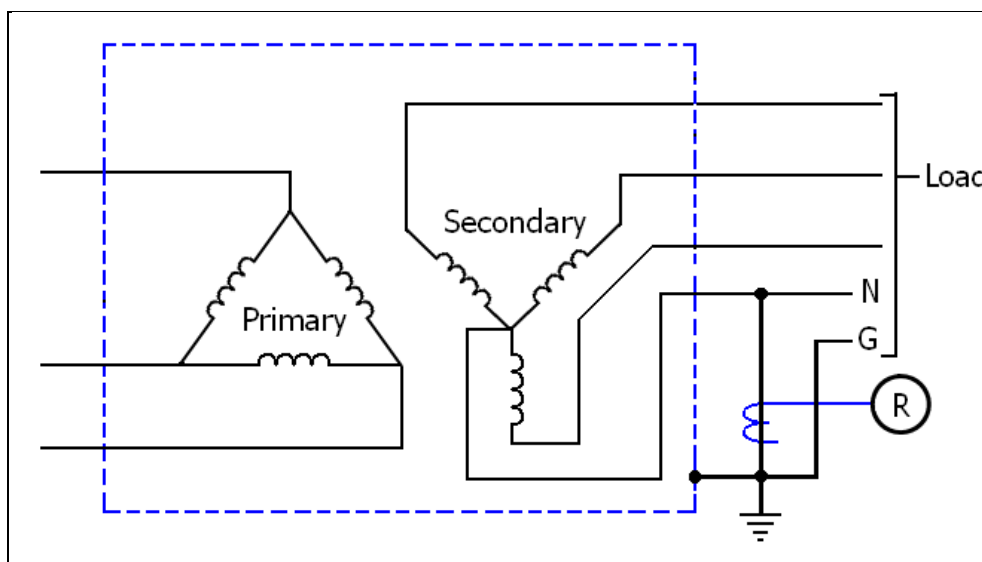
Fig. 2.4-3 Source Neutral Detection

This will prevent selectivity or coordination except by current magnitude or time-delay to trip. Consequently, this arrangement is often used as back-up protection or, with a low fault setting, to provide an alarm rather than trip signal. Conventional bar-type or window-type CT can be used for this application.

GROUND FAULT PROTECTION

With a few significant differences, the general application rules for phase relays also apply to ground relays. Ground relays are for faults involving zero sequence quantities, primarily single phase-to-ground faults and sometimes two-phase-to-ground faults. There are two basic types of ground relays - overcurrent and distance. The directional or non-directional overcurrent types are used widely at most voltage levels.

NONDIRECTIONAL OVERCURRENT GROUND PROTECTION

Non-directional O/C ground fault protection can be obtained by the current transformer connections shown in Fig. 2.4-4.
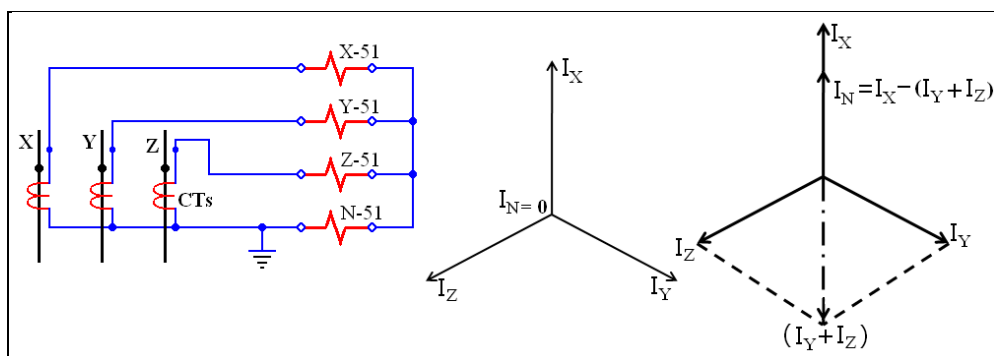
Fig. 2.4-4 Overcurrent Ground Relay

For normal loads and for phase-to-phase faults, the vector sum of the three phase currents I_X, I_Y, and I_Z equals zero, and the net or resultant current in N-51 is zero. If one conductor of the line is grounded, the vector sum of the three-phase current is no longer zero, and a resultant current (I_N) flows through the N-51 relay.

DIRECTIONAL OVERCURRENT GROUND PROTECTION

Directional overcurrent relays are used for ground fault protection in many applications. One method used on overhead tie-lines is the potential polarization scheme shown in fig. 2.4-5.
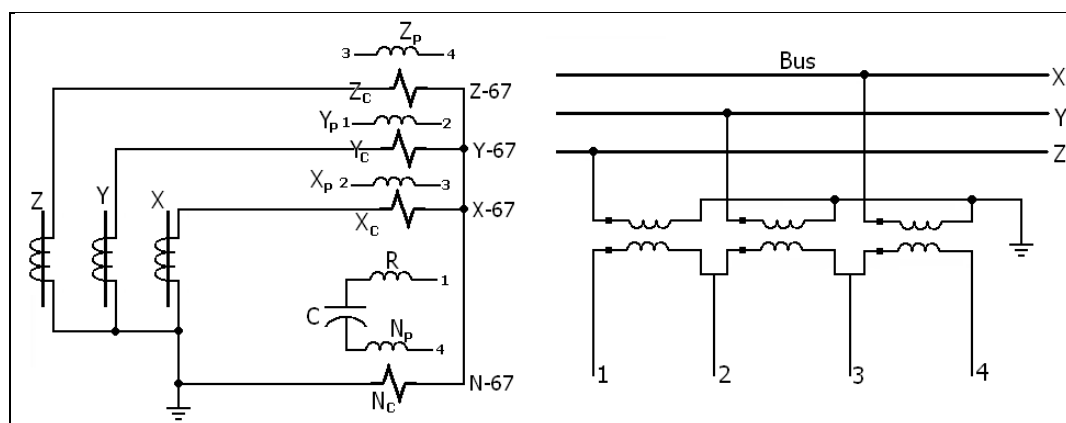
Fig. 2.4-5 Potential Polarized Directional Ground Relay

For normal loads and phase-to-phase faults, no current flows through N_C, and no potential exists between terminals 1 and 4 supplying the voltage coil (N_P) of N-67.

When one line conductor goes to ground, current flows through N_C, and a potential is developed between terminals 1 and 4 in the broken-delta connection of the bus potential transformers. If the phase relation between the coil currents of N_C and N_P indicates power flowing out on the line, the relay operates to trip the line breaker. Associated lines with similar ground relays will have power flowing towards the bus, and their directional contacts will remain open to prevent tripping.

The condenser and resistor in series with N_P are used to provide a phase-shift in coil current for better torque in the desired direction. The phases of the potential coils X_P, Y_P, and Z_P are also selected to give better torque for the power factors encountered under fault conditions.

Directional overcurrent ground relaying can use current polarization as well as potential polarization. The source of polarizing or reference current is usually a current transformer in the neutral of a Y/Δ power transformer. Refer to Fig. 2.4-6.
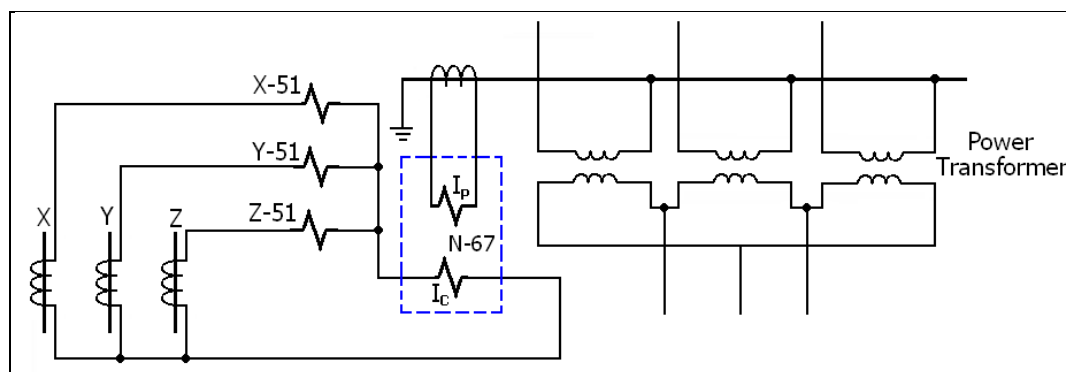
Fig. 2.4-6 Current Polarized Directional Ground Relay

A ground fault on the line will result in current flow through the coils (**I_C**) and (**I_P**) When the phase relation between these two coil currents indicates power flow towards the line, the relay will trip the line breaker. Similar ground relays on associated lines will have I_C current in the opposite (bus) direction, and their contacts will not close.

GROUND DISTANCE PROTECTION

Impedance type distance relays may be used as ground fault relays where overhead ground wires are used for lightning shields and where the impedance of the ground return path is reasonably constant. Without a ground wire, the ground fault impedance varies too much to provide accurate distance measurement.

Reactance-type distance relays, on the other hand, are not sensitive to variations in ground resistance, so they are applicable to ground fault protection where a ground wire is not used.

Distance relays are not used extensively for ground fault protection because this type of relaying requires more relays and auxiliary equipment than current directional ground relaying.

SUMMARY

- Ground faults occur because of a failure in the insulation system.

- Ground fault means that some current is delivered through the CTs from the power source but does not return through one of the conductors.

- At normal operation, the sum of CT secondary currents = zero.

- At abnormal operation, the sum of the CT secondary currents $\neq$ zero.

- For core balance CT, mains conductors pass through the window opening in the CT and are surrounded by the same magnetic core.

GLOSSARY

Occurrence:	Incident.
Residual:	Remaining.
Broken-delta:	Type of VT connections.
Consequently:	Resulting from.
Constituting:	Representing.

REVIEW EXERCISE

Circle the letter a, b, c or d that correctly completes the statement and follow the directions to answer the other questions:

1. The most common fault type occurs in transmission lines is:
    a) Phase-to-phase fault.
    b) Phase-to ground fault.
    c) Two phase-to-ground fault.
    d) Three phase-to-ground fault.

2. Ground fault relays include …………………………………………….
    a) Directional overcurrent unit type.
    b) None directional overcurrent unit type.
    c) Distance unit type.
    d) All of the above.

3. CT connections utilized to detect ground fault current include:
    a) Conventional connection
    b) Zero sequence connection
    c) Source neutral
    d) All of the above.

4. Mark true or false for each of the following.
    a) Zero sequence window type CT has only a primary winding and core.
    b) Reactance relays are sensitive to variations in ground resistance.
    c) Impedance relays may be used for ground fault relays, where overhead ground wire is used.
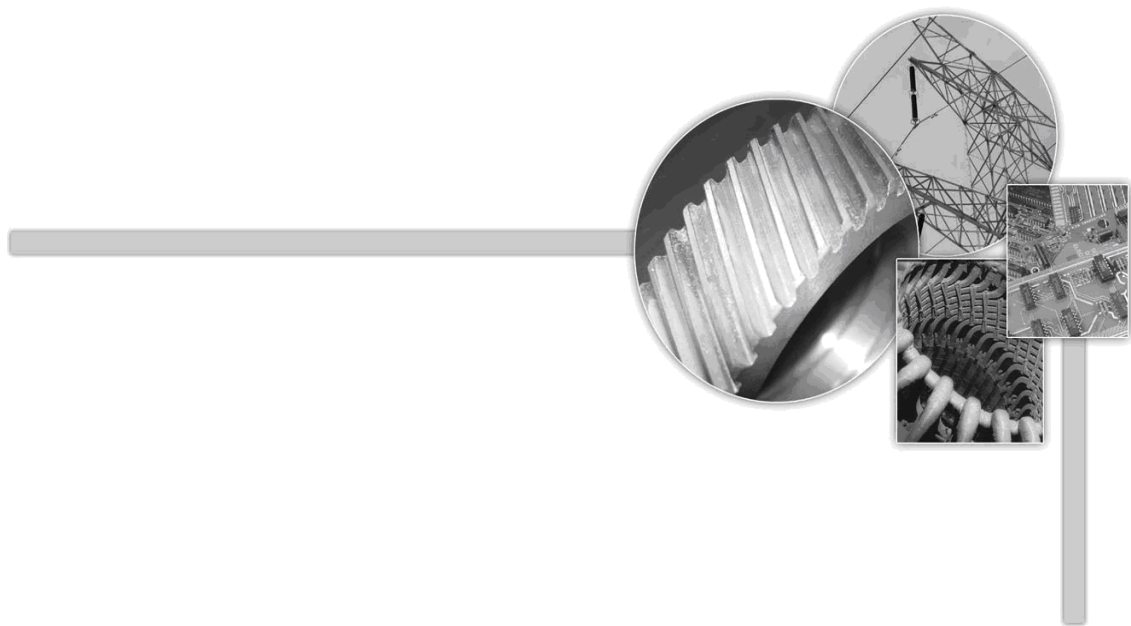
LESSON 2.5

BREAKER FAILURE

LESSON 2.5

BREAKER FAILURE

OVERVIEW

This lesson discusses the case when a fault occurs and the near breaker fails to trip. Breaker failure offers the solution for this problem.

OBJECTIVES

Upon completion of this lesson, the trainee will be able to:

- Define breaker failure.
- Describe local backup and breaker failure.
- State the application of the breaker failure.
- Identify parts of "KC" relay used for breaker failure schemes.

INTRODUCTION

Breaker failure is defined as a failure of the breaker to open or to interrupt when a trip signal is received. In the event of a breaker failure, some remote protection would isolate the faults. Backup relaying provides necessary redundancy in protective systems. Backup protection operates if the primary protection fails or is temporarily out of service. Backup protection for equipment such as generators, busses, and transformers usually duplicates the primary protection and is arranged to trip the same breakers.

LOCAL BACKUP AND BREAKER FAILURE

Local backup and breaker-failure protection are characterized by fault detection and initiation of tripping at the local terminal. The failure of circuit breakers to interrupt fault current when called upon to trip by relays is a moderately frequent and extremely serious problem in electric power system operation.

For example, if a fault on line HR (Fig. 2.5-1) is not properly cleared by the primary protection system because of a failure in any part of the system other than the circuit breaker, the secondary relaying system will detect the fault and trip breaker 2.
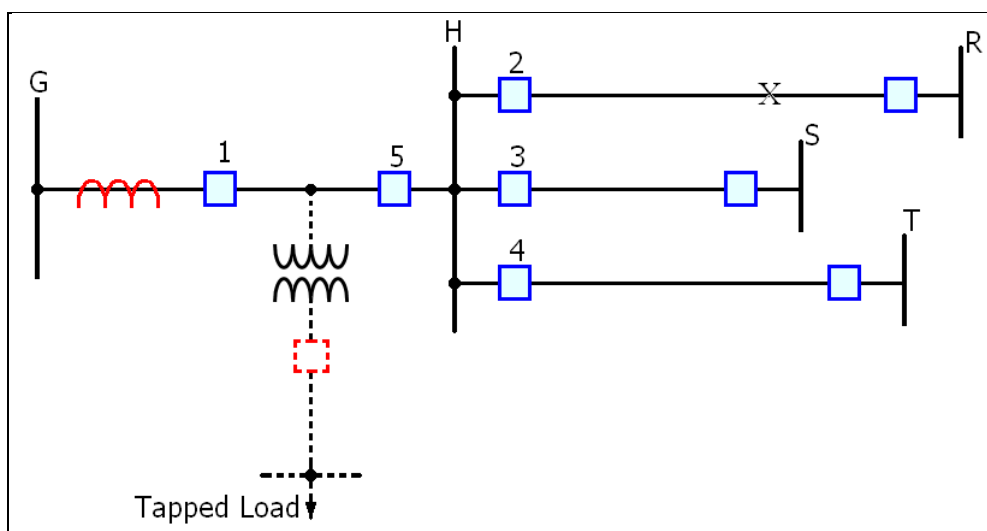
Fig. 2.5-1 Single Line Diagram to explain Breaker Failure Protection

If the fault on line HR is not properly cleared because of a failure of breaker 2, then the primary and/or secondary protective relays will initiate local breaker-failure backup to open breakers 3, 4 & 5 at bus H.

Fig. 2.5-2 shows an example to illustrate the advantages of local breaker-failure protection over the former practice of depending entirely on remote backup relaying.
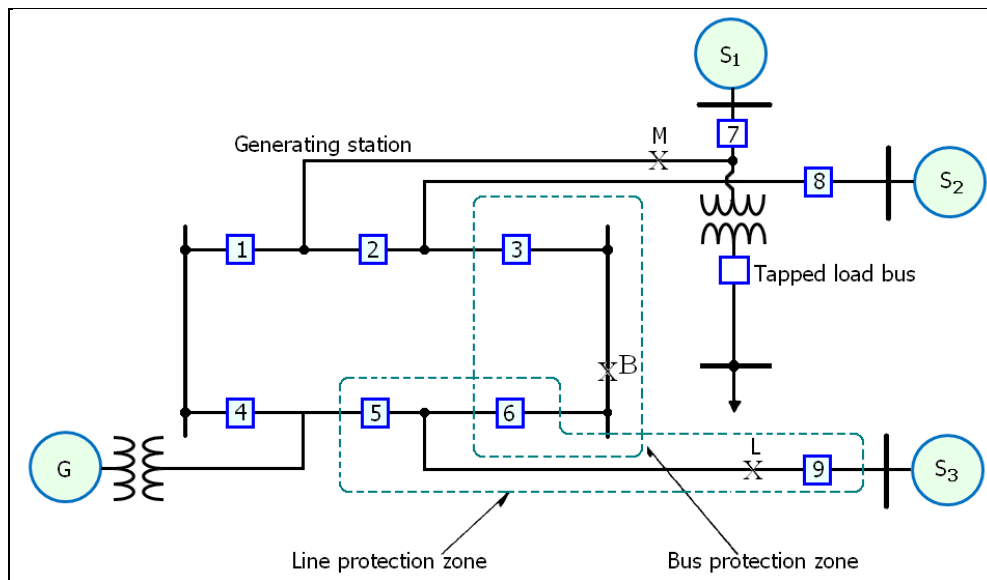
Fig. 2.5-2

In this diagram, the generating station high-voltage bus uses a breaker and a half arrangement. Lines interconnect the station to systems S_1, S_2 & S_3.

Fault L is normally cleared by line relays tripping breakers 5, 6 & 9. Assume, however, that breaker 6 mechanism sticks so that current flowing through breaker 6 is not interrupted. Under this condition, back-up protection must function. If remote backup is relied upon, time delay relays must trip remote breakers 7 & 8. In addition, local generator feed through breaker 6 must be interrupted by tripping breaker 4.

However, if breaker-failure protection is incorporated in the system, the fault is cleared by the tripping of breaker 3. This action provides selective tripping, since as much of the system as possible was left intact. If breakers 4, 7, & 8 must trip, the local generator is lost and unnecessary separation of the generating station from power systems S_1 and S_2 would result. In addition, the tapped load would be interrupted unnecessarily instead of being left tied to system S_2. Although breaker-failure

protection offers many advantages, remote back up cannot be eliminated from consideration. For example, assume that in Fig. 2.5-2, breaker 3 fails for bus fault B. Breaker-failure protection will promptly trip breaker 2, but the fault is still fed by breaker 9. Likewise, if breaker 2 fails with a line fault at M, a remote breaker must trip to clear the fault. Breaker-failure protection trips breaker 3, but breaker 8 continues to feed the fault. Although breaker-failure protection does not complete the job in these examples, it does provide quick trip to the local breaker, making it easier for the remote relays to detect the fault.

APPLICATIONS REQUIRING REMOTE BACKUP WITH BREAKER-FAILURE PROTECTION

Where ring busses or breaker-and-a-half schemes are used, breaker-failure protection does not necessarily eliminate the need for remote backup. As shown in Fig. 2.5-3, a fault on any line requires tripping two breakers at station H. A fault on line HR, for example, requires tripping both breakers 2 and 3 at station H. If breaker 2 fails to clear the fault, breaker failure would initiate tripping of breaker 5 but would leave line GH still connected to the fault. The breaker-failure protection for breaker 2 frequently initiates transfer-tripping of breaker 1 at station G. If transfer-trip is not applied or is not operative, however, remote backup at breaker 1 is still required to clear the fault.
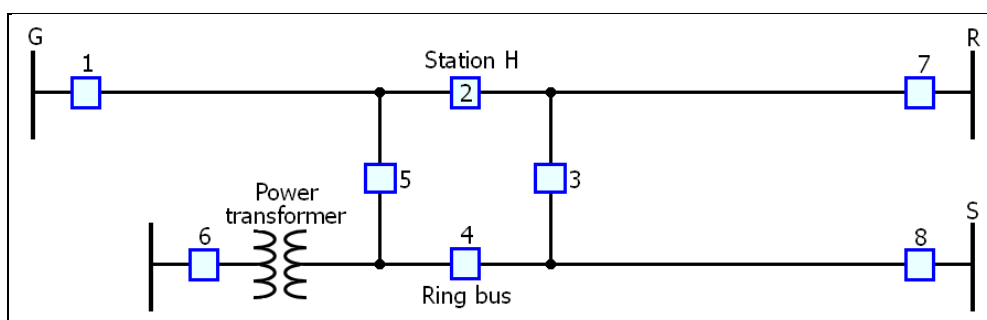
Fig. 2.5-3 Remote Backup Required with Breaker Failure at Station H where Ring Bus or Breaker and a Half Schemes are used

Because of the infeed effect and high apparent impedances, remote backup from the remote stations may be difficult if not impossible to achieve when all lines were in

service. Opening the breakers around the failed breaker will, however, remove the infeed effect and permit remote backup coverage. If for example, breaker 2 fails for a fault on line HR (Fig. 2.5-3), line protection will open breaker 3 and breaker-failure protection will open breaker 5 to remove all infeeds around station H except that from line GH.

Breaker-failure protection would trip both breakers 5 and 6 upon failure of breaker 4 for a line HS fault. Similarly, the failure of breaker 5 in Fig. 2.5-3 for a line GH fault would trip both breakers 4 and 6. All other breaker-failure conditions would require remote backup, which is recommended in addition to transfer-trip.

BREAKER FAILURE/LOCAL BACKUP APPLICATIONS

It is recommended that:

(1) One breaker-failure circuit per breaker be applied, regardless of the bus configuration.

(2) All adjacent breakers be tripped, regardless of fault location.

One timer per bus or one timer per breaker may be used. The latter is recommended, since it provides maximum isolation and flexibility, even though it does involve additional timers.

TIMING CHARACTERISTICS

The time chart Fig. 2.5-4 illustrates the various time delays, which determine the total breaker failure clearing time and the necessary time delays to achieve the security of the system. The shaded margin time provides the security. The setting of the timer must be sufficient to allow for the proper tripping of the breaker and the current detector reset. The additional security time margin mentioned above must take into account such variables as breaker interrupting times in excess of rated time, variations in time delay and timer over-travel and possible variations of setting values due to temperature changes.
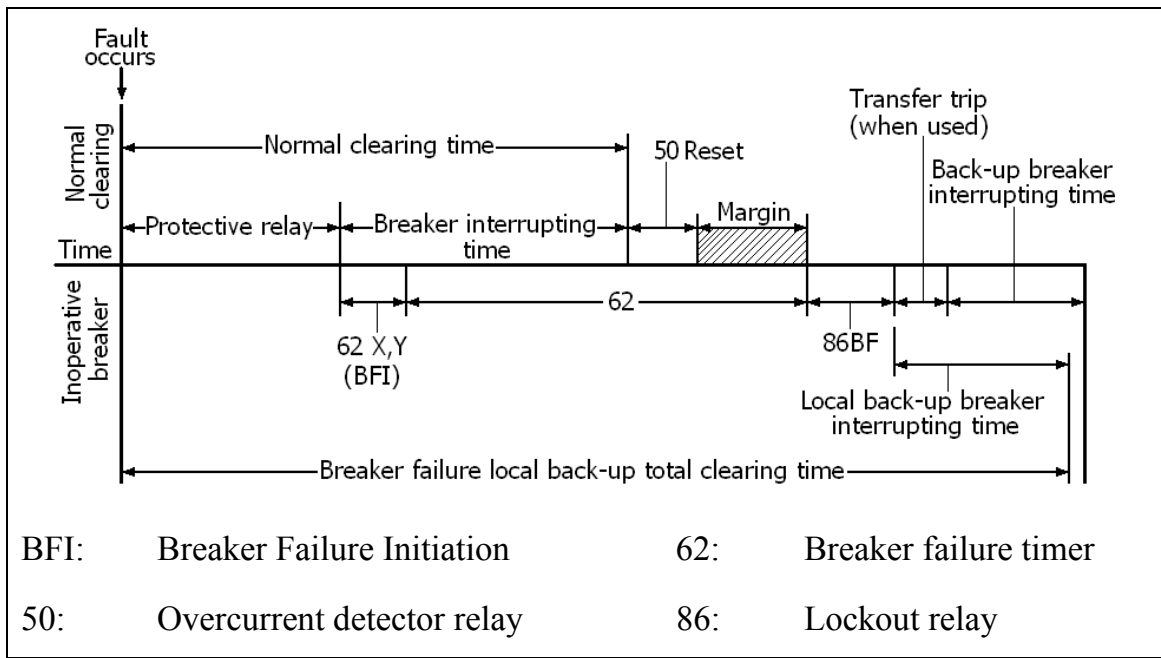
Fig. 2.5-4 Breaker Failure Local Backup Time Chart

CURRENT DETECTOR RELAY TYPE KC-4

Current detector relay type KC-4 (Fig. 2.5-5) is used for phase and ground faults and breaker failure protection schemes. It is a non-directional current or fault detector, which operates for all phase and ground faults to supervise the tripping of other protective relays. It is particularly suited for breaker-failure relaying schemes in which it supervises local back-up tripping, based on the presence or absence of current flow in the protected circuit breaker.

CONSTRUCTION

The KC-4 relay consists of two-cylinder type phase instantaneous overcurrent operating units, one ground overcurrent unit, and an indicating Contactor switch.

Each overcurrent unit operates to close its contact when current exceeds a specified value. The indicating Contactor Switch, actuated by closure of one of the cylinder unit contacts, relieves the main contact of carrying the heavy trip current, and displays a target, which indicates operation of the relay.

This target is reset by a push rod from outside the relay case.

(a) Front View	(b) Rear View
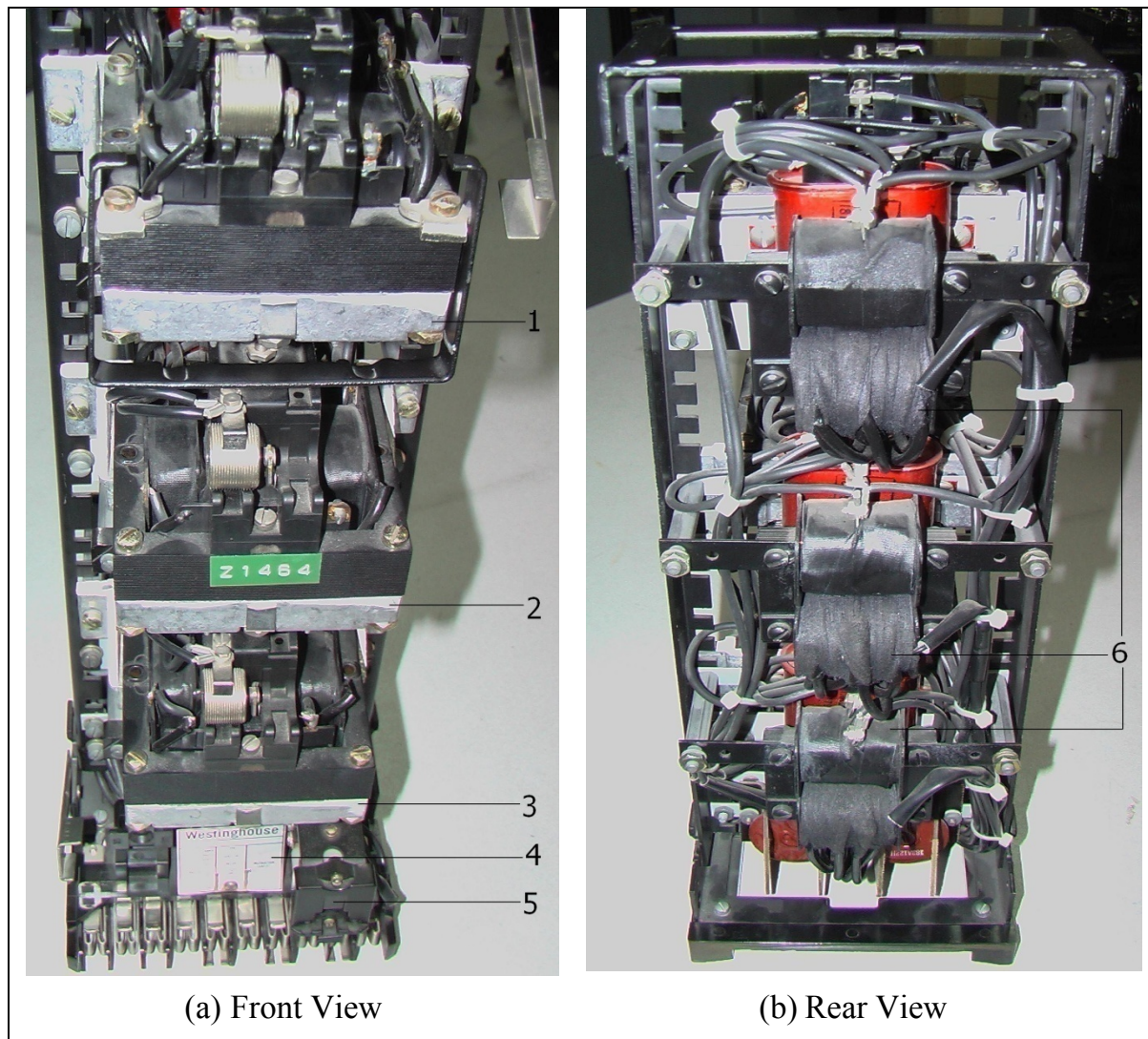
Fig. 2.5-5 Breaker Failure Relay Type KC-4

1)   Phase Instantaneous Overcurrent Unit (1_A).

2)   Phase Instantaneous Overcurrent Unit (1_C).

3)   Ground Instantaneous Overcurrent Unit (1_O).

4)   Indicating Contactor Switch.

5)   Name plate.

6)   Saturating transformer.

OPERATION OF BREAKER FAILURE SCHEMES

SINGLE BUS SINGLE BREAKER ARRANGEMENT

In a properly functioning breaker, current flow should cease shortly after the trip circuit is energized. The time interval between trip-circuit energization and current flow cessation is the breaker-interrupting time. If interruption doesn't occur in this much time, the breaker is assumed to have failed and the breaker-failure relaying should initiate tripping of adjacent and/or remote breakers to isolate the protected breaker. For the present bus arrangement, all the breakers on the bus must be tripped if any one of them fails. This is readily accomplished by having the breaker-failure protection circuits energize the bus-differential lockout auxiliary (**86B**).

SUMMARY

- Breaker failure relay is a device that sends trip signal to all the breakers around fault when the breaker near the fault fails to trip.

- Breaker failure starts its operation after time delay to give the back-up protection a chance to operate.

- Breaker failure has overcurrent detector element and timer that initiates operation but after coordination time with the backup protection.

- The total time to initiate breaker failure must contain the normal clearing time of the main protection with its reset time plus the local backup interrupting time plus a time margin.

GLOSSARY

Failure:	Breakdown.
Initiate:	Start.
Funnel:	A tool used to pour liquid in a bottle
In conjunction:	Along with

REVIEW EXERCISE

Answer the following questions, using the next diagram:

1.   Which breaker(s) will trip if there is a fault at point (L)?

      ……………………………………………………………………………………

2.   Which breaker(s) will trip if there is a fault at point (M)?

      ……………………………………………………………………………………

3.   Which breaker(s) will trip if there is a fault at point (N)?
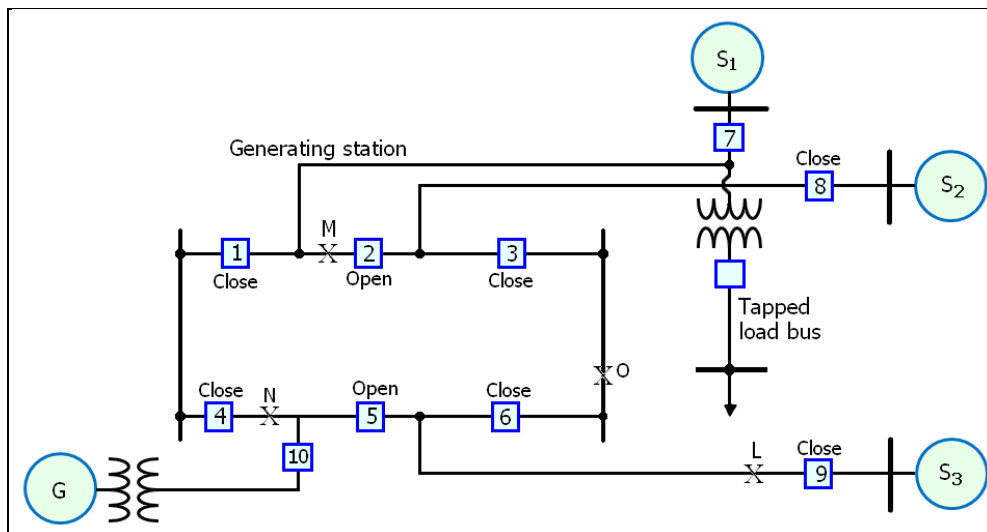
4.   What is the bus-bar arrangement for the above diagram?

   a)   Breaker and half.

   b)   Double bus double breaker.

   c)   Main and transfer bus.

   d)   Ring bus.

5.   Normal clearing time for fault with primary protection equals:

   a)   Protective relay operation time plus backup breaker time.

   b)   Backup breaker interrupting time, plus a margin.

   c)   O/C detector relay reset plus backup breaker time.

    d)   Protective relay operation time plus breaker interrupting time.

6.   Breaker failure relay is fed from:

    a)   Current transformer.

    b)   Voltage transformer.

    c)   Current & voltage transformers

    d)   None of the above.

7.   The breaker failure sends signal when:

    a)   The fault is detected.

    b)   The fault is not detected.

    c)   The elapsed time is over and the trip is not verified.

    d)   The elapsed time is over and the trip is verified.

TASK 2.5-1

PARTS OF BREAKER FAILURE RELAY TYPE KC-4

OBJECTIVE

Upon completion of this task, the trainees will be able to:

- Demonstrate the parts of breaker failure relay type KC-4.

TOOLS, MATERIALS, & EQUIPMENT

- Relay type KC-4
- Instruction manual
- Personal safety equipment as recommended in relay workshop.

PROCEDURE

1. Read the nameplate of the relay.

2. Remove the relay from the casing with care.

3. Identify phase instantaneous overcurrent unit (I_A) including:

   a) Cylinder frame.

   b) Moving contact and stationary contact.

   c) Electromagnet and bridge.

4. Identify phase instantaneous O/C unit (I_C) with same parts in step 3.

5. Identify ground instantaneous O/C unit (I_O) with same parts in step 3.

6. Identify indicating contactor switch.

7. Read the diagram in Fig. 2.5-6 (Information Sheet) Single bus Single breaker arrangement using KC-4 relay and one timer per bus. Explain to your Instructor primary relay tripping and backup relay tripping.
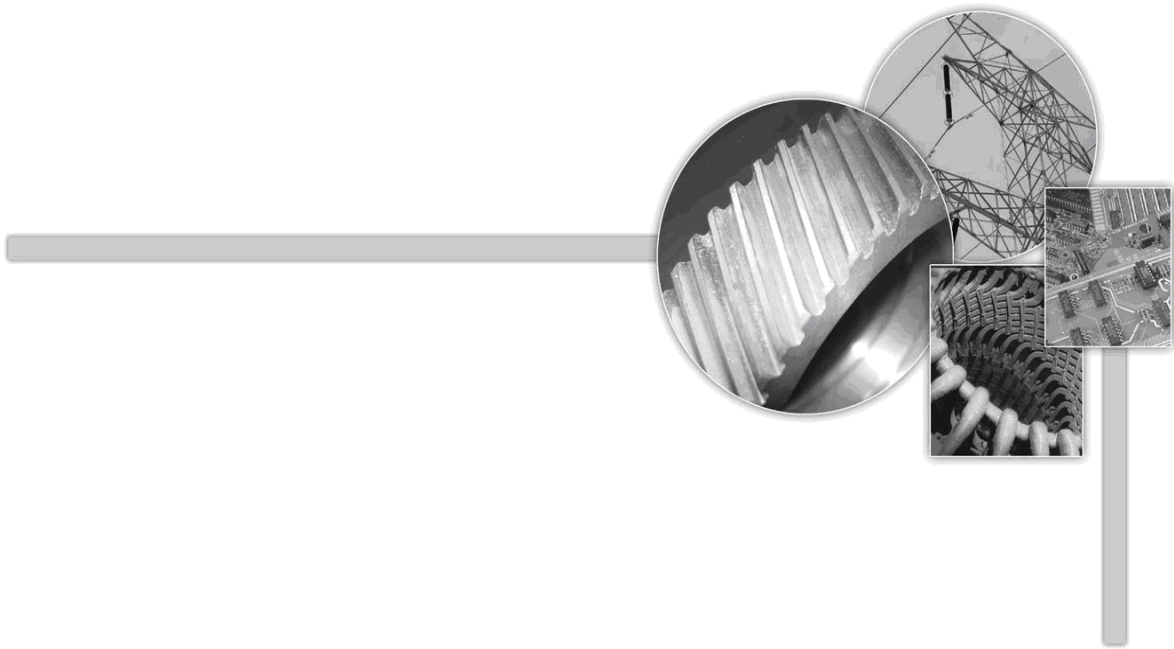
LESSON 2.6

FEEDER PROTECTION

LESSON 2.6

FEEDER PROTECTION

OVERVIEW

This lesson discusses the protection of feeder for radial and ring configurations, given the applications of directional and nondirectional overcurrent protection

OBJECTIVES

Upon completion of this lesson, the trainee will be able to:

- Discuss and verify protection of radial feeders.

- Demonstrate the coordination of nondirectional overcurrent protection.

- Identify protection of ring feeder system.

- Illustrate coordination of single source loop systems.

INTRODUCTION

Feeder is a circuit, which carries a large block of power to a sub-feeder panel or to some point at which the power block is distributed into smaller circuits. Feeders may exist in medium or low voltage transmission lines and cables over short distance, there are two types of feeders:

- Radial feeder.
- Ring feeder.

PROTECTION OF RADIAL FEEDERS

Fig. 2.6-1 shows several sections of a typical radial feeder. Because the feeder is radial each section requires only one breaker at the source or distribution substation end. To clear faults at (1) and other faults to the right, only the breaker at R needs to be tripped. To clear faults at (2) and (3) on the line between them, the breaker at H must be tripped, likewise, to clear faults at (4), (5) and between them, the breaker at G must be tripped.
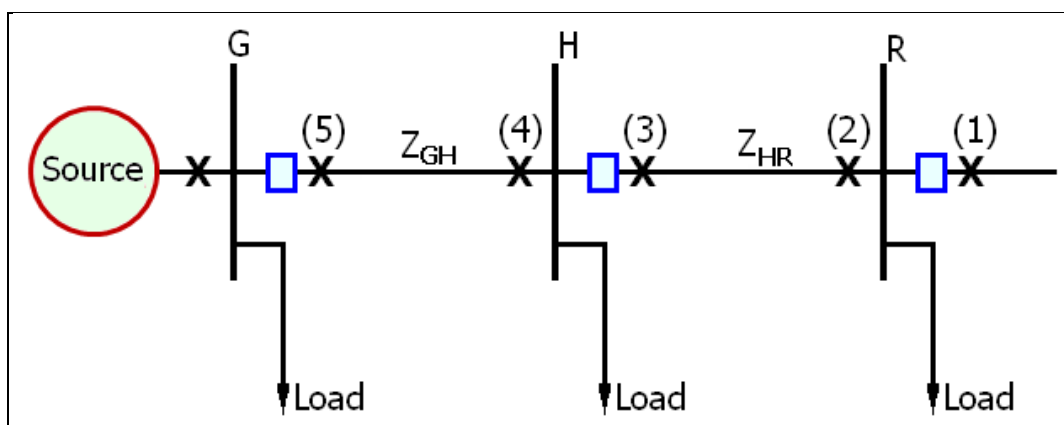
Fig. 2.6-1 A Typical Radial Feeder

The relays at the breaker location cannot distinguish whether the remote fault is on the protected line, on the remote bus, or on an adjacent line. The relays at H, for example, cannot distinguish between faults at (1) and at (2) since the current magnitude

measured at H for fault (1) or at (2) will be the same. Opening breaker H for fault (1) is not desirable, since it would interrupt the load at R unnecessarily. Two techniques are available to solve this problem:

    (a) Time delay or time graded.   (b) Pilot Relaying.

Time graded technique delays the operation of the relay for a remote fault, allowing relays and breakers closer to the fault to clear it, in Fig. 2.6-1, the relays at H will delay for faults at (1) or (2). If the fault is at (1) this delay will allow the R relays and breakers to operate before (H). Although (H) would not open for a fault at (1), unless the R relays or associated breaker failed, it would operate for a fault at (2). This technique, called coordination or selectivity, is designed to combine minimum operating time for the close in faults with a long enough delay for remote faults, the relays and breaker at R coordinate with those to the right. H must coordinate with R, and G. Relays are coordinated in pairs. If breaker (H) relay trip characteristic have already been coordinated with relays at R and beyond, the breaker at G must then be coordinated with those at H for the three critical fault points at (5), (3) and (2).

PROTECTION OF RING FEEDER SYSTEM

A ring system with a single source is shown in Fig. 2.6-2 for the purpose of the following discussion on ring feeder protection. All breakers in this system will be considered closed during operation. All locations have directional overcurrent relays, except locations (1), (10); having nondirectional overcurrent relays.
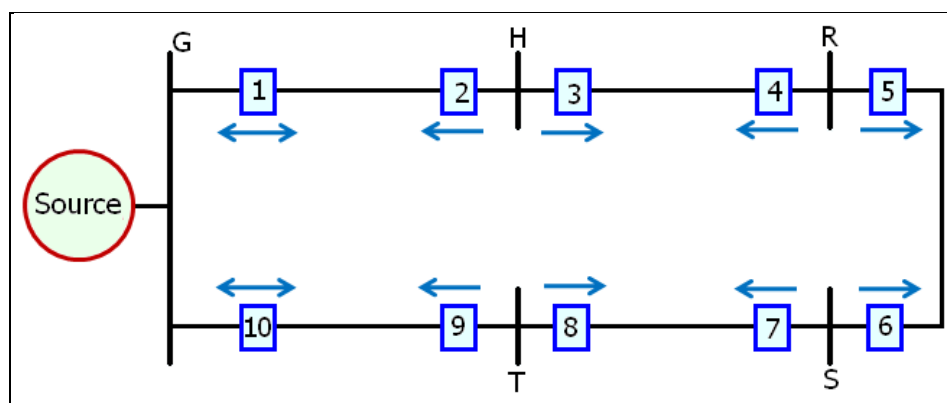
Fig. 2.6-2 Single Source Loop (Ring) Circuit and its Protection

At all other locations, current can flow in either direction through the relays for faults to the right of bus (**G**). With load taken off at each bus, load current can also flow in the other direction through relays 3, 4, 5, 6, 7 & 8.

If loads are tapped on lines-GH and GT, load current can also flow in either direction through relays 2 & 9. These directional relays are installed at all these locations.

These relays will operate when the pick-up current is above the setting, but only if the current flows in the direction of the arrows, which, in each case, is into the line.

For this single source system, lines-GH & GT can be protected by instantaneous directional overcurrent relays set very sensitively at 2 & 9. Since the fault current through relays 2 & 9 goes to zero as the fault location reaches bus-G, the instantaneous directional relays cannot overreach. For these same faults, the current through relay (1) or (10) will be maximum and the relays located at these locations will operate in minimum time. When breaker (1) or (10) opens, the current through relay (2) increases in the tripping direction, while for faults on line-GT, the current through relay (9) increases in the tripping direction. Thus, for faults on line-GH, close to bus-G, breaker (2) opens sequentially after breaker (1). Similarly, for faults on line-GT, close to bus-G, breaker (9) opens sequentially after breaker (10).

COORDINATION ON SINGLE SOURCE LOOP SYSTEMS

In principle, the coordination procedure for relays on a single source loop is the same as for radial feeders. This fault current on any bus, except the source bus is greater when the loop is closed; however, when the loop is opened between the fault and the source bus, the current in any branch will increase.

For directional relays, two sets of relays must be coordinated. With a breaker (10) open, relay (1) must be coordinated with relay (3), (3) with (5), (5) with (7) and (7) with (9), while with breaker (1) open, relay (10) must be coordinated with relay (8), (8) with (6), (6) with (4) and (4) with (2).

SUMMARY

- The main protection of radial feeder is the nondirectional overcurrent relay.

- In the ring feeder of single source both of directional and nondirectional overcurrent relays may be used.

- Coordination of single source loop system means that the relay near the fault must operate faster, and that far from the fault slower.

GLOSSARY

Radial feeder: Fed only from one side

Ring feeder: Loop of feeders

Coordination: Organization, between relays

Directional: Based on power flowing in one or the other direction

Non-directional: Look to both directions

Sequentially: One after the other.

REVIEW EXERCISE

Circle the letter a, b, c or d that correctly completes the statement and follow the directions to answer the other questions:

1.   Radial system feeders are protected by:

a)   Differential relays.   b)   None-directional overcurrent relays.

c)   Directional   overcurrent   d)   All of the above

      relays.

2.   Feeders of ring system with single source are protected by:

a) Directional   overcurrent   b)   Non-directional overcurrent relays.

      relays.

c)   Differential relays.   d)   Both of directional & non-directional

                                          overcurrent relays.

3.   Study the following diagram, and then answer the following questions:
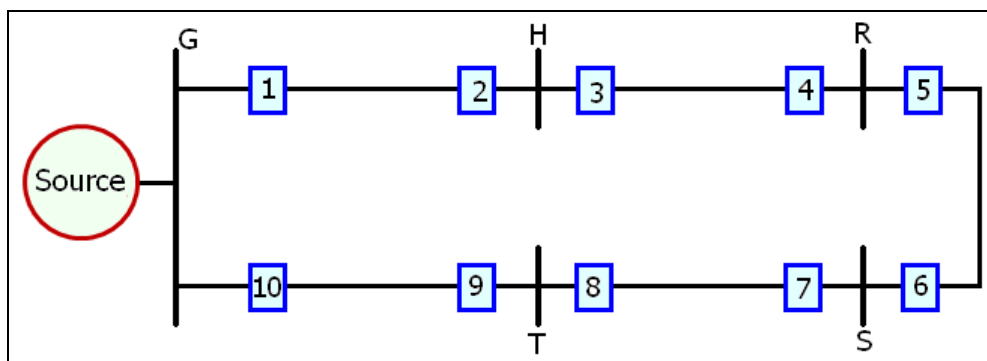
a.   Which location(s) should have directional overcurrent relays?

……………………………………………………………………………………………

b.   Which location(s) should have non-directional overcurrent relays?

……………………………………………………………………………………………

c.   On the diagram draw arrows representing the directionality of directional overcurrent relays.

LESSON 2.7

PHASE BALANCE PROTECTION

LESSON 2.7

PHASE BALANCE PROTECTION

OVERVIEW

This lesson discusses the three phase motor protection against unbalanced phases or open circuit for any phase during loading, demonstrating CM relay as an electromechanical phase balance relay for motor protection.

OBJECTIVES

Upon completion of this lesson, the trainees will be able to:

- Identify application and function of the current balance relay.
- Describe the operating principles of the current balance relays.
- Read the schematics of current balance relays.

INTRODUCTION

The current balance relay monitors and compares the three-phase currents. When the relay detects an abnormal difference between any two phases, it trips the circuit breaker.

The current balance relay is used for protection of three-phase lines and machines against damage due to phase unbalance and single-phase operation. Current balance relays are used where the three-phase currents of the system are normally balanced. Any unbalance of the currents would indicate a fault condition or open circuit in one or more of the phases.

There are two types of phase balance relays that are normally applied, current balance and negative sequence overcurrent. The current balance relay operates when the difference in the magnitude of rms currents in two phases exceeds a given percentage value. The negative sequence current relay operates on magnitude of negative sequence current, but is calibrated in terms of (I_2^2 t), corresponding to the thermal energy produced by this current. In order to set the negative sequence relay, the (I_2^2 t) characteristic of the machine must be specified.

CURRENT BALANCE AND PHASE BALANCE

Comparison of currents from two different current sources can be readily made by various relay types. A current balance relay may use the hinged armature, induction disc or the induction cup construction. Such a relay has two torque producing elements actuated by currents obtained from the two circuits - one element producing operating torque tending to close the contacts. The ratio in percent of the operating current to the restraining current to cause the relay to operate scaled the percent "**slope**" of the operating characteristics.

If induction disc relay is used, one coil of the relay produces a torque that opposes the torque produced by a second coil, and no movement results when the currents and

torques are equal. Unbalance of current results in a movement of the element, which may open or close a contact, or it may open one contact and close another.

Fig. 2.7-1 shows phase balance relay (46), which contains two induction-disc units.

One unit balances I_a against I_b, and the other balances I_b against I_c. When the currents become sufficiently unbalanced, the resultant torque is produced in one or both of the units, closing their contacts (which are connected in parallel in the trip circuit).
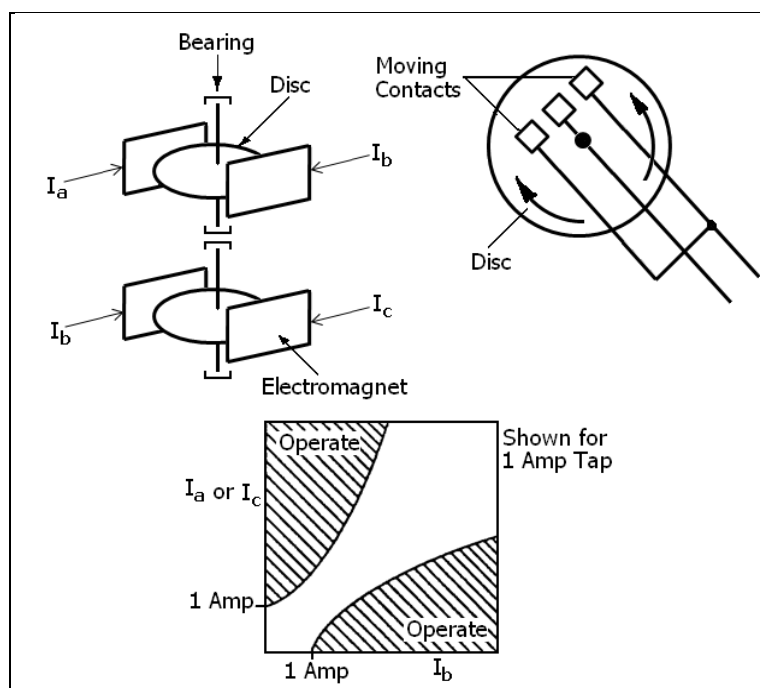
Fig. 2.7-1 Phase Unbalance Relay (46)

APPLICATION OF PHASE BALANCE RELAYS

Phase unbalance protection is applied to a feeder supplying a large motor or a group of small motors, where there is a possibility of one of the feeder phases opening as a result of a connector failure, fuse failure or similar cause.

Protection against phase unbalance in a three-phase feed is feasible when the load is normally balanced between phases, and unbalance would be an indication of trouble. This makes it possible to design a relay that is very sensitive to load unbalance, but will not be affected by a wide range of load current.

EXAMPLE OF PHASE BALANCE RELAYS

Relay type CM (Westinghouse made) is used for the protection of three-phase machines from phase unbalance or phase failure. The CM-relay (Fig. 2.7-2), is designed to provide protection against unbalance in phase currents by operating to trip the circuit breaker when a fixed percentage of unbalance exists between any two phases. It will therefore, protect the machines or apparatus under load when the desired sensitivity cannot be obtained by voltage-operated relay. That is because three-phase machines tend to maintain normal phase voltage even with one phase open, unless the machine is heavily loaded.
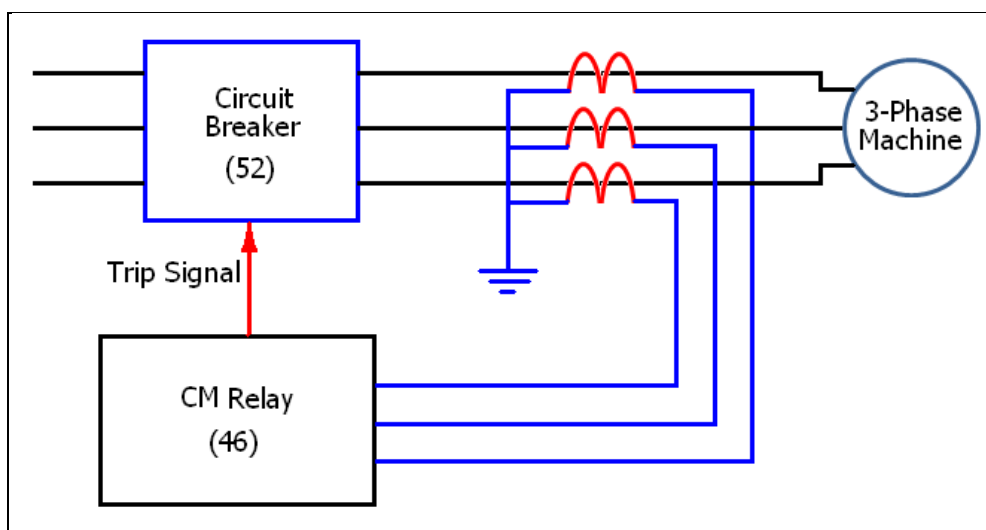
Fig. 2.7-2 Using CM Relay for 3-Phase Machine Protection

OPERATION

CM-relay consists of two mechanically independent induction disc units, (Fig. 2.7-3). Usually 1 and 2 phase currents energize the upper electromagnets, while phase 2 and 3 currents energize the lower electromagnets. When phase currents are balanced, the electromagnets create equal and opposing torques on each of the discs. The relay contacts are electrically common and connected in parallel. Closing of any one contact on either the upper or lower disc completes the trip circuit.
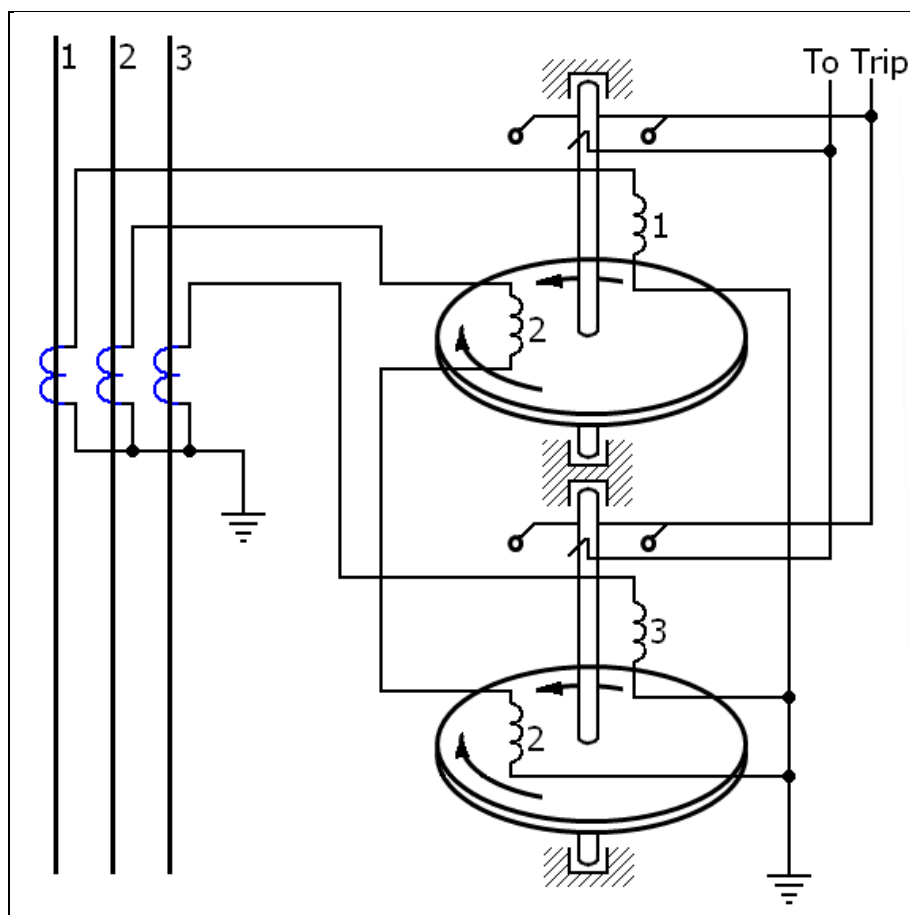
Fig. 2.7-3 Two Induction Discs CM-Relay Operation

CONSTRUCTION

The relay consists of two main current units. An indicating contactor switch (ICS) or seal-in unit is provided (Fig. 2.7-4).

When the switch is energized, the moving contacts bridge the stationary contacts, completing the trip circuit. The ICS contacts are connected in parallel with the main relay contacts, relieving them of carrying heavy trip currents. The main contacts of the relay will close 30 amperes at 250 volts DC, and the indicating contactor switch contacts will carry this current for sufficient time.
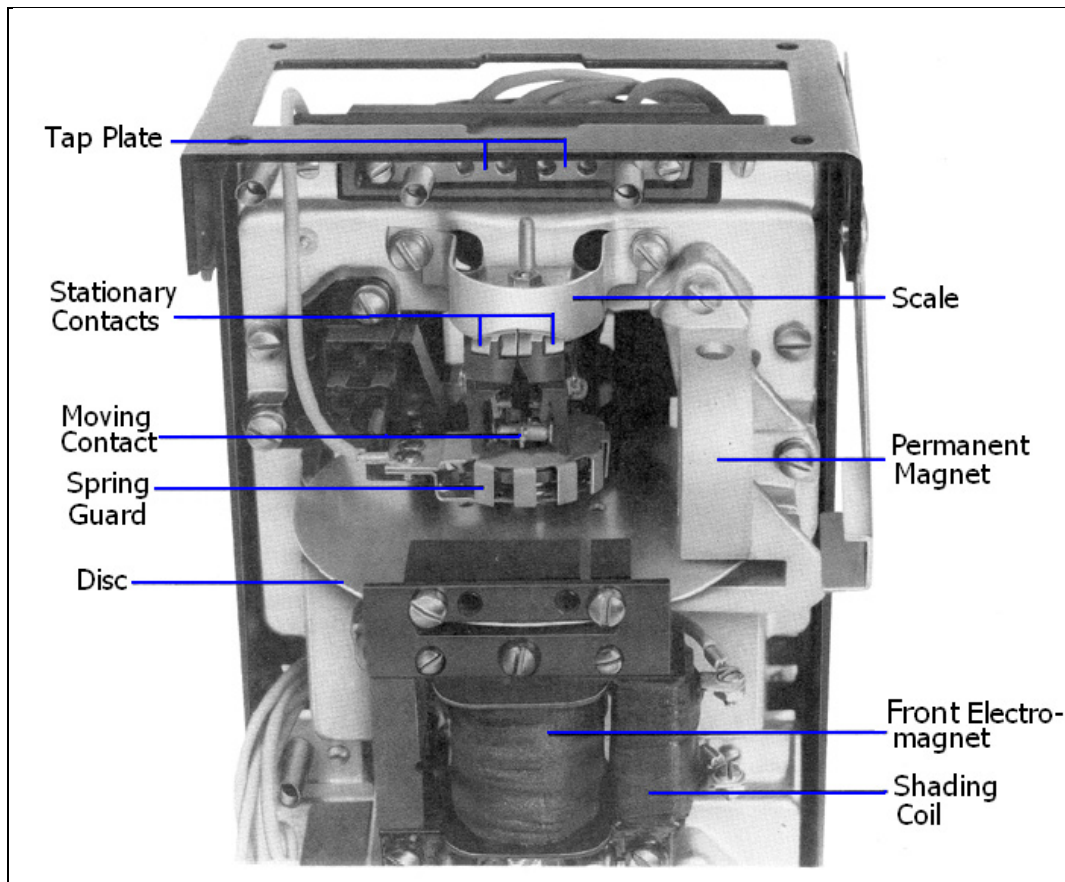
Fig. 2.7-4 Construction of Phase Balance Relay Type CM

CM-RELAY CONNECTION

As shown in Fig. 2.7-5 & Fig. 2.7-6, the relay may be used with either two or three current transformers. With two current transformers, the accuracy class must be at least 10H35 or 10L70. With three current transformers, the accuracy class must be at least 10H25 or 10L50. Otherwise, current transformer errors during motor starting may cause undesired CM tripping.
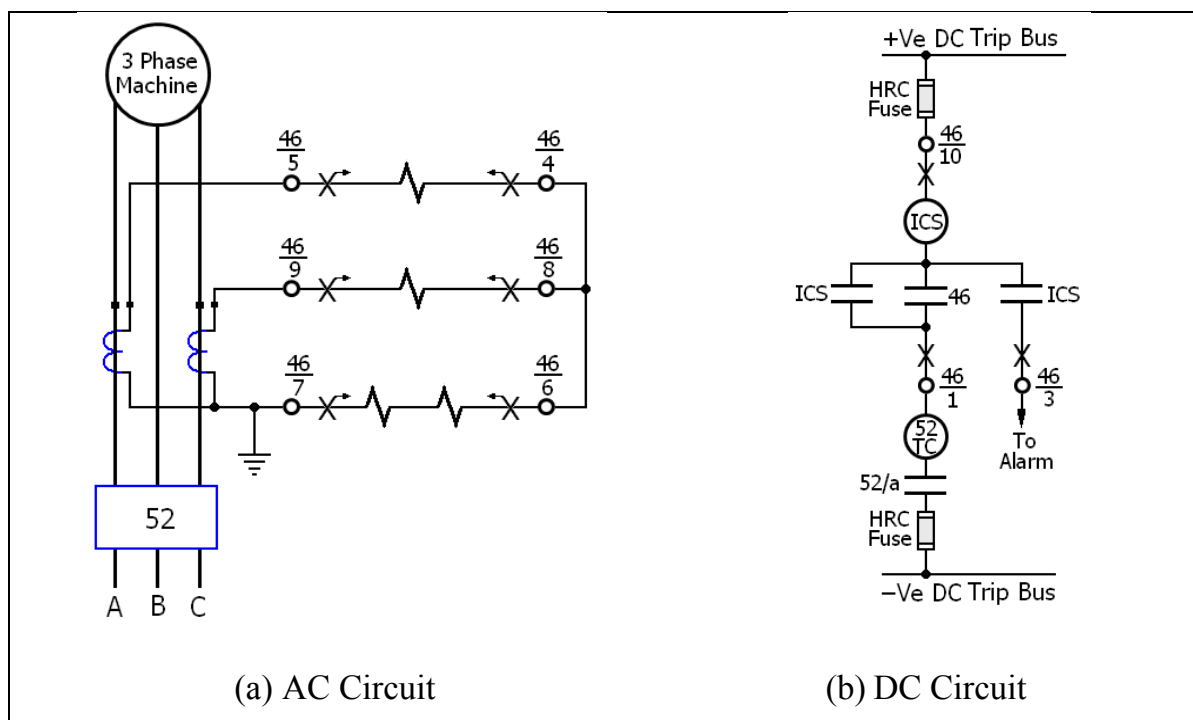
Fig. 2.7-5 Two CTs with Ungrounded Neutral System
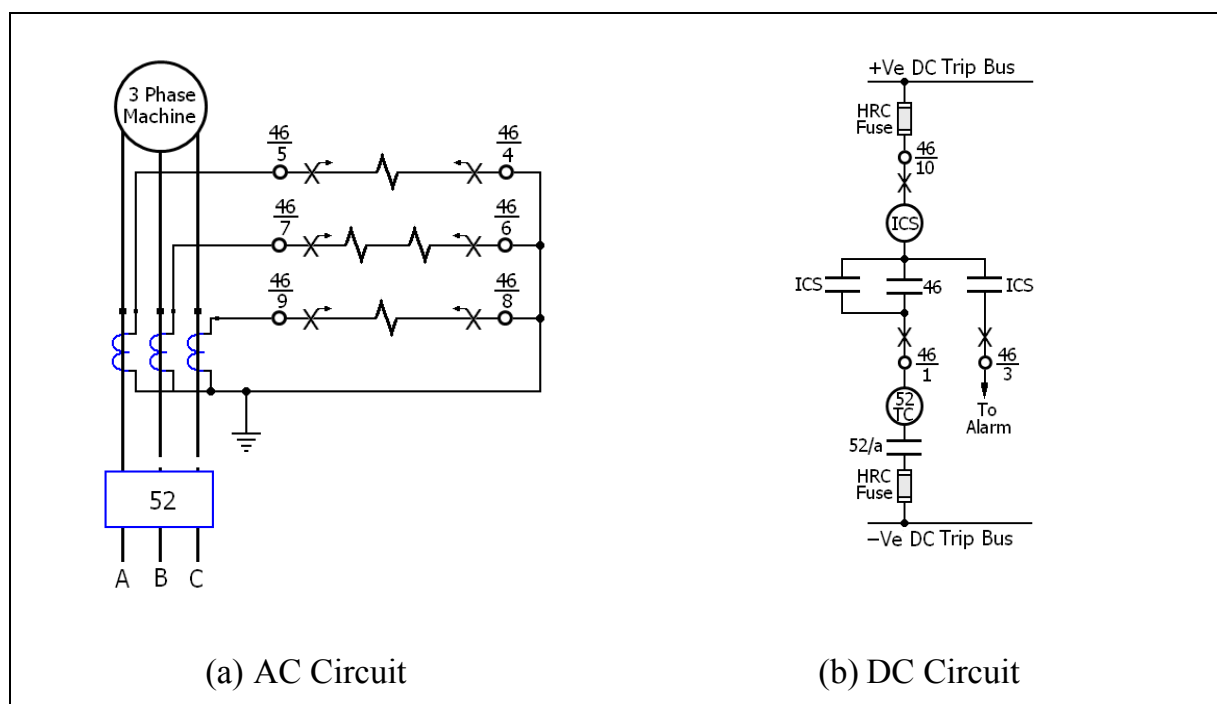
Fig. 2.7-6 Three CTs with Grounded Neutral System

DEVICE NUMBER CHART

46: Phase balance current relay.	52: AC power circuit breaker.
52a: Breaker auxiliary contact.	52TC: Breaker trip coil.
ICS: Indicating contactor switch.	

SUMMARY

- Phase balance relay is used for motor protection against unbalance or open phase.

- Phase balance relay may be fed from two CTs or three CTs.

- There are two types of phase balance relays that are normally used for current balance and negative sequence overcurrent.

- The current balance relay operates when the difference in the magnitude of rms currents in two phases exceeds a given percentage value.

- CM phase balance relay has two induction disc units.

- Each induction disc unit operates depending on the balance of two phases individually.

- CM Phase balance relay can operate with grounded or ungrounded neutral systems.

GLOSSARY

Phase balance: Equality of currents in each two phases.

Grounded neutral: Neutral point is connected to ground.

Ungrounded neutral: Neutral point is isolated.

REVIEW EXERCISE

Circle the letter a, b, c or d that correctly completes the statement and follow the directions to answer the other questions:

1. Current balance relays use: …………………………………………
   a) Hinged armature   b) Induction disc
   c) Induction cup   d) All of the above

2. How many torques are produced in phase balance relay?
   a) One   b) Two
   c) Three   d)Four

3. What is the function device number of phase balance relay?
   a)66   b)67
   c)46   d)64

4. DC. operated indicating contactor switch is: …………………
   a) Damping magnet unit   b) Induction disc unit
   c) Induction cup unit   d) Clapper type unit

5. How many indicating contactor switches (ICS) are there in the phase balance relay?
   a) One   b) Two
   c) Three   d) Four

6. How many CTs and VTs are required for the phase balance relay?
   a) One CT & one VT   b) Two CTs & two VTs
   c) Three CTs   d) Three VTs

7. Phase balance relay is used to protect : ………………………………

    a) Power transformers   b) Large motors

    c) Bus bars   d) Feeders

8. Phase balance relay operates when ………………………… occurs:

   a) Unbalance in three phase currents   b) A phase to ground fault

   c) A change in frequency   d) A phase to phase fault

9. Open circuit in one phase lets the phase balance relay:

     (To operate – Not operate).

10. The phase balance relay operates when the ……………………………:

     a. Sum of three phase currents exceeds a given percentage value.

     b. Phase rotation of the three phases is reversed.

     c. Difference in rms currents in two phases exceeds a given percentage value.
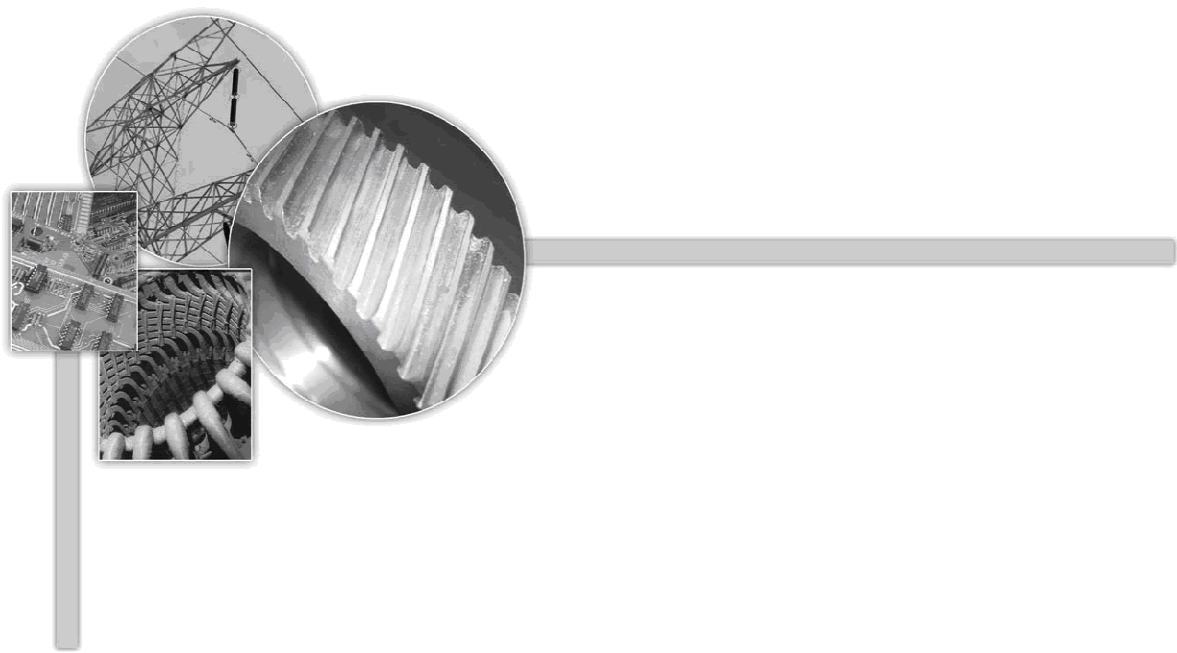
UNIT 3

INTRODUCTION TO DIGITAL SYSTEMS

UNIT 3

INTRODUCTION TO DIGITAL SYSTEMS

OVERVIEW

This unit discusses the importance of using digital systems in protection. It starts with the number system, which convert the instructions and data into 1s & 0s. The unit also describes logic gates as the basic element of digital circuits.

It continuous with combination between logic gates to form a complete hardware of the digital relay. The unit also focuses on the famous logic circuits, which exists in the digital hardware circuits of the digital relay.

OBJECTIVES

Upon completion of this unit, the trainees will be able to:

- Identify the number systems.

- Describe the logic gates and integrated circuits (ICs).

- Illustrate flip-flops and shift registers.

- Verify the applications of clock circuits.

- Demonstrate the function of decoder, encoder, multiplexer, and demultiplexer.

SAFETY PRECAUTIONS FOR DIGITAL ELECTRONICS WORKSHOP

1. Be sure that all powered equipment is connected to the same power source. This will establish a common reference and prevent ground loops.

2. Make sure you do NOT inadvertently insert a ground into the circuit under test. This could occur, for example, if your test equipment reference (ground) lead is earth grounded.

   Use an ohmmeter, set to R x 1, to see if the equipment reference lead is earth grounded. Measure between reference lead and the center prong on the power plug. If the reading is zero, your equipment is earth grounded. If it is earth grounded, all measurements MUST be referenced to ground.

3. The accuracy of your experiments may vary slightly with those of other students or examples given in the test. This is because of component part tolerances, meter calibration, and the individual interpolation of the meter's reading.

LESSON 3.1

NUMBER SYSTEMS

LESSON 3.1

NUMBER SYSTEMS

OVERVIEW

This lesson discusses the importance of number systems, which are used in digital systems. The lesson browses decimal, binary, and hexadecimal number systems.

The conversion from a number system to another and binary coded decimal number system are also discussed in this lesson.

OBJECTIVES

Upon completion of this lesson, the trainees will be able to:

- Identify binary number system.

- Familiarize with hexadecimal number system.

- Convert from any number system to another.

- Familiarize with binary coded decimal number system.

INTRODUCTION

Almost all digital computers and systems are based on binary (two-state) operation. For instance, the switch can be opened or closed; therefore, a switch is one example of a natural binary device.

Even the transistor circuits used in digital computers and systems are designed to operate in either of two states, typically at cutoff or saturation. As a result, the output of a transistor circuit is either a low or a high voltage. When you look at digital signals with an oscilloscope, you find that each voltage is either low or high. These digital signals change during a computer run, so that they appear like pulses.

In conclusion, switches, transistors and almost all other digital components are based on binary operation. This is why it is convenient to use binary numbers when analyzing or designing digital circuits. Besides knowing how to count with binary numbers, it is necessary to learn how to convert from binary to decimal, and vice versa.

BINARY SYSTEM

The expression for binary system is (the power of 2) $N = 2^n$.

Power of 2		Decimal	
2^0	=	1	
2^1	=	2	
2^2	=	4	
2^3	=	8	etc,

Using this rule, the binary number can rapidly be evaluated in terms of its decimal equivalent as shown below.

BINARY NUMBERING SYSTEM					
2^5	2^4	2^3	2^2	2^1	2^0
32NDS	16THS	8THS	4THS	2'S	1'S
6TH NUMBER	5TH NUMBER	4TH NUMBER	3RD NUMBER	2ND NUMBER	1ST NUMBER

DECIMAL TO BINARY CONVERSION							
DECIMAL			BINARY NUMBER				
			2^4	2^3	2^2	2^1	2^0
HUNDREDS	TENS	UNITS	16'S	8'S	4'S	2'S	1'S
		0					0
		1					1
		2				1	0
		3				1	1
		4			1	0	0
		5			1	0	1
		6			1	1	0
		7			1	1	1
		8		1	0	0	0
		9		1	0	0	1
	1	0		1	0	1	0
	1	1		1	0	1	1
	1	2		1	1	0	0
	1	3		1	1	0	1
	1	4		1	1	1	0

CONVERSION TABLE OF DECIMAL AND BINARY NUMBERS						
Decimal Numbers	2^5 (32)	2^4 (16)	2^3 (8)	2^2 (4)	2^1 (2)	2^0 (1)
0	0	0	0	0	0	0
1	0	0	0	0	0	1
2	0	0	0	0	1	0
3	0	0	0	0	1	1
4	0	0	0	1	0	0
5	0	0	0	1	0	1
6	0	0	0	1	1	0
7	0	0	0	1	1	1
8	0	0	1	0	0	0
9	0	0	1	0	0	1
10	0	0	1	0	1	0
20	0	1	0	1	0	0
30	0	1	1	1	1	0
40	1	0	1	0	0	0
41	1	0	1	0	0	1
42	1	0	1	0	1	0
50	1	1	0	0	1	0
56	1	1	1	0	0	0

Example 1: The decimal equivalent of the binary number 11101:

$$= (1 \times 2^4) + (1 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0)$$
$$= 16 + 8 + 4 + 0 + 1$$
$$= 29$$

Example 2: The decimal equivalent of 100100:

$$= (1 \times 2^5) + (0 \times 2^4) + (0 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0)$$
$$= 32 + 0 + 0 + 4 + 0 + 0$$
$$= 36.$$

Example 3: The decimal equivalent of 110.0101:

$$= (1 \times 2^2) + (1 \times 2^1) + (0 \times 2^0) \; . \; (0 \times 2^{-1}) + (1 \times 2^{-2}) +$$
$$(0 \times 2^{-3}) + (1 \times 2^{-4})$$
$$= 4 + 2 + 0 \; . \; 0 + 0.25 +$$
$$0 + .0625$$
$$= 6.3125$$

BINARY-TO-DECIMAL CONVERSION

A binary number is a weighted number. The value of a given binary number in terms of its decimal equivalent can be determined by adding the products of each bit and its weight. The right-most bit is the **least significant bit (LSB)** in a binary number and has a weight of $2^0 = 1$. The weights increase by a power of two for each bit from right to left. The method of converting a binary number to decimal is illustrated by the following example.

Example: Convert the binary number 1101101 to decimal:

Binary weight:	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Weight value:	64	32	16	8	4	2	1
Binary number:	1	1	0	1	1	0	1

Deci. equivalent.: $1 \times 64 + 1 \times 32 + 0 \times 16 + 1 \times 8 + 1 \times 4 + 0 \times 2 + 1 \times 1$

$\qquad = 64 + 32 + 0 + 8 + 4 + 0 + 1$

Decimal number: 109_{10}.

The subscript 10 identifies the number as a decimal number to avoid confusion with other number systems.

Example: Determine the decimal value of the fraction binary number 0.1011

Binary weight: $\qquad 2^{-1} \qquad 2^{-2} \qquad 2^{-3} \qquad 2^{-4}$

Weight value: $\qquad 0.5 \qquad 0.25 \qquad 0.125 \qquad 0.0625$

Binary number: $\qquad 1 \qquad 0 \qquad 1 \qquad 1$

Deci. equivalent.: $1 \times 0.5 + 0 \times 0.25 + 1 \times 0.125 + 1 \times 0.0625$

$\qquad 0.5 + 0 + 0.125 + 0.0625$

Decimal number: 0.6875_{10}.

Note that to determine the decimal value of a binary number, fractional or whole, we simply add the weights of each 1 and ignore each 0 because the product of a 0 and its weight is 0.

Another method of evaluating a binary fraction is to determine the *whole-number value* of the bits and divide by the *total possible combinations* of the number of bits appearing in the fraction. For instance, for the binary fraction in previous example (0.1011):

1. If we neglect the binary point, the value of 1011_2, is 11_{10} in decimal.

2. With four bits, there are $2^4 = 16$ possible combinations.

3. Dividing, we obtain $11/16 = 0.6875_{10}$.

The following examples illustrate the evaluation of binary numbers in terms of their equivalent decimal values. The subscript 2 identifies binary numbers.

Example: The decimal value of 11101.011_2

$\qquad (16 + 8 + 4 + 1) \, . \, (0.25 + 0.125) = 29.375_{10}$

$\qquad$ Using the alternate method to evaluate the fraction, we have $3/8 = 0.375_{10}$

Example: The decimal value of 110101.11_2

$(32 + 16 + 4 + 1) . (0.5 + 0.25) = 53.75_{10}$

Using the alternate method to evaluate the fraction, we have $3/4 = 0.75_{10}$

DOUBLE-DABBLE METHOD

The double-dabble method may be used to convert binary numbers to decimal numbers following a few special rules.

1. Beginning with the one (1) at the most left position write a one (1) over that digit.
2. Move to the next digit.
   a. If the digit is a zero, double the number you wrote above the preceding digit and write it above the zero.
   b. If the digit is a one (1), double the number you wrote above the preceding digit and add one. Place this number above the one (1).

3. Continue this procedure through all digit in the binary number. The number you write above the last digit is the decimal equivalent.

Example: Convert 10001 base two to base ten

	1	2	4	8	17
10001 =	1	0	0	0	1

Therefore $10001_2 = 17_{10}$

DECIMAL-TO-BINARY CONVERSION

Now you will learn two ways of converting from a decimal number to a binary number.

SUM-OF-WEIGHTS METHOD

One way to find the binary number equivalent to a given decimal number is to determine the set of binary weight values whose sum is equal to the decimal number. For instance, the decimal number 9 can be expressed as the sum of binary weights as follows,

$$9 = 8 + 1 = 2^3 + 2^0$$

By placing a 1 in the appropriate weight positions, 2^3 and 2^0 and a 0 in the other positions, we have the binary number for decimal 9.

$$2^3 \quad 2^2 \quad 2^1 \quad 2^0$$

$$1 \quad 0 \quad 0 \quad 1_2 \quad \text{binary nine}$$

Example: Convert the following decimal numbers to binary:

> (a) 12,   (b) 25,   (c) 58,   (d) 82.

> (a) $12_{10} = 8 + 4 = 2^3 + 2^2$ $\Rightarrow$ 1100_2

> (b) $25_{10} = 16 + 8 + 1 = 2^4 + 2^3 + 2^0$ $\Rightarrow$ 11001_2

> (c) $58_{10} = 32 + 16 + 8 + 2 = 2^5 + 2^4 + 2^3 + 2^1 \Rightarrow$ 111010_2

> (d) $82_{10} = 64 + 16 + 2 = 2^6 + 2^4 + 2^1$ $\Rightarrow$ 1010010_2

REPEATED DIVISION BY 2 METHOD

A more systematic method of converting from decimal to binary is the *repeated division-by-2* process. For example, to convert the decimal number 12 to binary, we

begin by dividing 12 by 2 and then dividing each resulting quotient by 2 until there is a 0 quotient. The remainders generated by each division form the binary number: the first remainder produces the least significant bit (LSB) in the binary number. This procedure is shown below:

Example: Convert 19 to binary number:

$$
\begin{array}{llll}
2 \,)\, 19 & & & \\
\quad 2 \,)\, 9 & \rightarrow & 1 & \text{(LSB)} \\
\quad 2 \,)\, 4 & \rightarrow & 1 & \\
\quad 2 \,)\, 2 & \rightarrow & 0 & \\
\quad 2 \,)\, 1 & \rightarrow & 0 & \\
& & 1 & \text{(MSB)} \\
& & \downarrow & \\
& & 10011_2 &
\end{array}
$$

Example: Convert 45 to binary number:

$$
\begin{array}{llll}
2 \,)\, 45 & & & \\
\quad 2 \,)\, 22 & \rightarrow & 1 & \text{(LSB)} \\
\quad 2 \,)\, 11 & \rightarrow & 0 & \\
\quad 2 \,)\, 5 & \rightarrow & 1 & \\
\quad 2 \,)\, 2 & \rightarrow & 1 & \\
\quad 2 \,)\, 1 & \rightarrow & 0 & \\
& & 1 & \text{(MSB)} \\
& & \downarrow & \\
& & 101101_2 &
\end{array}
$$

CONVERTING DECIMAL FRACTIONS TO BINARY

The previous examples demonstrated whole number conversions. Now, fractional conversions are examined.

The *sum-of-weights* method can be applied to fractional decimal numbers as shown in the following example:

$$0.625_{10} = 0.5 + 0.125 = 2^{-1} + 2^{-3} = 1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3} = 0.101_2$$

As you have seen, decimal whole numbers can be converted to binary by repeated division-by-2. Decimal fractions can be converted to binary by *repeated multiplication-by*-2. For example, to convert the decimal fraction 0.3125 to binary, we begin by multiplying 0.3125 by 2 and then multiplying each resulting fractional part of the product by 2 until the fractional product is zero. The *carries* are generated by each multiplication form the binary number. The first carry produced is the MSB. This procedure is shown in the following steps:

			Carry	Fractional Part	
0.3125	×	2	=	0.625	0	(MSB)
0.625	×	2	=	1.25	1	
0.25	×	2	=	0.50	0	
0.50	×	2	=	1.00	1	(LSB)

$$0.3125_{10} = 0.0101_2$$

EXERCISES

1. Convert each decimal number to binary by using the sum-of-weights method. (a) 23, (b) 57, (c) 45.5
2. Convert each decimal number to binary by using the repeated division-by-2 method (repeated multiplication-by-2 for fractions).

 (a) 14 (b) 21 (c) 0.375

ADDITION

There are four basic rules for adding binary digits:

$$0 + 0 = 0$$
$$0 + 1 = 1$$
$$1 + 0 = 1$$
$$1 + 1 = 10_2$$

Notice that three of the addition rules result in a single bit, and that the addition of two 1s yields a binary two (10_2). When binary numbers are added, the latter condition creates a sum of 0 in a given column and a carry of 1 over to the next higher column, as illustrated below:

```
  1 1    (carry)
  0 1 1
 +0 0 1
  1 0 0
```

In the right column, $1 + 1 = 0$ with a carry of 1 to the next column to the left. In the next column, $1 + 1 + 0 = 0$ with a carry of 1 to the next column to the left.

In the left column, $1 + 0 + 0 = 1$.

When there is a carry, we have a situation where three bits are being added (a bit in each of the two numbers and a carry bit). The rules for this are as follows:

$1 + 0 + 0$	=	01_2	1 with a carry of 0
$1 + 1 + 0$	=	10_2	0 with a carry of 1
$1 + 0 + 1$	=	10_2	0 with a carry of 1
$1 + 1 + 1$	=	11_2	1 with a carry of 1

The following example will illustrate binary addition with the equivalent decimal addition also shown.

(a) 11_2 3_{10} (b) 100_2 4_{10}

$+11_2$	$+3_{10}$		$+10_2$	$+2_{10}$
110_2	6_{10}		110_2	6_{10}

(c) 1111_2 15_{10} (d) 11100_2 28_{10}

 $+1100_2$ $+12_{10}$ $+10011_2$ $+19_{10}$

 11011_2 27_{10} 101111_2 47_{10}

SUBTRACTION

There are four basic rules for subtracting binary digits:

$$0 - 0 \quad = 0$$
$$1 - 1 \quad = 0$$
$$1 - 0 \quad = 1$$
$$10_2 - 1 \quad = 1$$

When subtracting numbers, we sometimes have to borrow from the next higher column. A borrow is required in binary only when we try to subtract a 1 from a 0.

In this case, when a 1 is borrowed from the next higher column, a 10_2 is created in the column being subtracted, and the last of the four basic rules listed above must be applied. The following examples illustrate binary subtraction with the equivalent decimal subtraction shown.

(a) 11_2 3_{10} (b) 11_2 3_{10}

 -01_2 -1_{10} -10_2 -2_{10}

 10_2 2_{10} 01_2 1_{10}

No borrows were required in the above examples. 01_2 is the same as 1_2.

(c) 101_2 5_{10}

 -011_2 -3_{10}

 010_2 2_{10}

Let us examine exactly what was done to subtract the two binary numbers.

When 1 is borrowed, a 0 is left.
$(0 - 0 = 0)$

Borrow 1 from next column
making a 10 in this column
$(10 - 1 = 1)$

$${}^{0}1 \quad {}^{1}0 \quad 1$$
$$-0 \quad 1 \quad 1$$

MULTIPLICATION

The following are four basic rules for multiplying binary digits:

$$0 \times 0 = 0$$
$$0 \times 1 = 0$$
$$1 \times 0 = 0$$
$$1 \times 1 = 1$$

Multiplication is performed in binary in the same manner as with decimal numbers. It involves forming the partial produces, shifting each successive partial product left one place, and then adding all the partial products. A few examples will illustrate the procedure and the equivalent decimal multiplication.

(a) $\quad 11_2 \qquad\qquad 3_{10}$

$\quad \underline{\times 1_2} \qquad\qquad \underline{\times 1_{10}}$

$\quad 11_2 \qquad\qquad 3_{10}$

(b) $\quad 11_2 \qquad\qquad 3_{10}$

$\quad \underline{\times 11_2} \qquad\qquad \underline{\times 3_{10}}$

$\quad 11_2 \qquad\qquad 9_{10}$

$\quad \underline{11_2}$

$\quad 1001_2$

(c) $\quad 111_2 \qquad\qquad 7_{10}$

$\quad \underline{\times 101_2} \qquad\qquad \underline{\times 5_{10}}$

$\quad 111_2 \qquad\qquad 35_{10}$

$\quad 000_2$

$\quad \underline{111_2}$

$\quad 10011_2$

(d) $\quad 1011_2 \qquad\qquad 11_{10}$

$\quad \underline{\times 1001_2} \qquad\qquad \underline{\times 9_{10}}$

$\quad 1011_2 \qquad\qquad 99_{10}$

$\quad 0000_2$

$\quad 0000_2$

$\quad \underline{1011_2}$

$\quad 1100011_2$

DIVISION

Division in binary follows the same procedure as division in decimal.

(a) $\qquad 10_2 \qquad\qquad 2_{10}$ (b) $\qquad 11_2 \qquad\qquad 2_{10}$

$\qquad 11\sqrt{110} \qquad 3\sqrt{6} \qquad\qquad 10\sqrt{110} \qquad 2\sqrt{6}$

$\qquad\quad \underline{110} \qquad\quad \underline{6} \qquad\qquad\quad \underline{100} \qquad\quad \underline{6}$

$\qquad\quad 000 \qquad\quad 0 \qquad\qquad\qquad 10 \qquad\quad 0$

$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad \underline{10}$

$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad 00$

(c) $\qquad 11_2 \qquad\qquad 2_{10}$ (d) $\qquad 10.1_2 \qquad\qquad 2.5_{10}$

$\qquad 100\sqrt{1100} \qquad 4\sqrt{12} \qquad\quad 110\sqrt{1111.0} \qquad 6\sqrt{15.0}$

$\qquad\quad \underline{100} \qquad\quad \underline{12} \qquad\qquad\quad \underline{110} \qquad\quad \underline{12}$

$\qquad\quad 100 \qquad\quad 0 \qquad\qquad\qquad 11\,0 \qquad\quad 3\,0$

$\qquad\quad \underline{100} \qquad\qquad\qquad\qquad\qquad \underline{11\,0} \qquad\quad \underline{3\,0}$

$\qquad\quad 000 \qquad\qquad\qquad\qquad\qquad 00\,0 \qquad\quad 0$

EXERCISE

1. Perform the following additions:

   (a) $1101_2 + 1010_2$ (b) $1011_2 + 1101_2$

2. Perform the following subtractions:

   (a) $1101_2 - 0100_2$ (b) $1001_2 - 0111_2$

3. Perform the indicated operation:

   (a) $110_2 \times 111_2$ (b) $1100_2 \div 11_2$

BINARY CODED DECIMAL (BCD)

As you have learned, decimal numbers can be represented by binary digits. Not only numbers, but also letters and other symbols, can be represented by 1s and 0s. In fact, any being expressible as numbers, letters, or other symbols can be represented by binary digits, and therefore can be processed by digital logic circuits. Combinations of binary digits that represent numbers, letters, or symbols are digital codes. In many applications, special codes are used for such auxiliary functions as error detection.

THE 8421 CODE

The 8421 code is a type of binary coded decimal (BCD) code and is composed of four bits representing the decimal digits 0 through 9. The designation 8421 indicates the binary weights of the four bits (2^3, 2^2, 2^1, 2^0). The ease of conversion between 8421 code numbers and the familiar decimal numbers is the main advantage of this code. The 8421 code is the predominant BCD code, and when we refer to BCD, we always mean the 8421 code unless otherwise stated.

Binary coded decimal means that each decimal digit is represented by a binary code of four bits. All you have to remember are the ten binary combinations that represent the ten decimal digits as shown in Table below.

You should realize that with four bits, sixteen numbers (2^4) can be represented, and that in the 8421 code only ten of these are used. The six code combinations that are not used (1010, 1011, 1100, 1101, 1110, and 1111) are invalid in the 8421 BCD code.

8421 (BCD)	Decimal
0000	0
0001	1
0010	2
0011	3
0100	4

0101	5
0110	6
0111	7
1000	8
1001	9

To express any decimal number in BCD, simply replace each decimal digit by the appropriate four-bit code, as shown by the following example.

Example: Convert each of the following decimal numbers into BCD:

    (a) 3   (b) 9.2   (c) 18   (d) 34.8   (e) 65

    (f) 92   (g) 150   (h) 321   (i) 1472.

(a)   3   (b)   9.2

      0011   1001 . 0010

(c)   18   (d)   34.8

    0001   1000   0011 0100 . 1000

(e)   65   (f)   92

    0110   0101   1001   0010

(g)   150   (h)   321

   0001 0101 0000   0011 0010 0001

(i)   1472

    0001 0100 0111 0010

It is equally easy to determine a decimal number from a BCD number. Start at the decimal point and break the code into groups of four bits. Then write the decimal digit represented by each four-bit group. An example illustrates.

Examples: Find the decimal numbers represented by the following BCD codes:

(a) 1000 0110   (b) 0011 0001   (c) 0101 0011   (d) 1001 0111 0100

(e) 0001 1000 0110 0000 . 0111

(a) 1000 0110 (b) 0011 0001 (c) 0101 0011 (d) 1001 0111 0100
    8   6   3   1   5   3   9   7   4

(e) 0001 1000 0110 0000 . 0111
    1   8   6   0 . 7

BCD ADDITION

BCD is a numerical code, and many applications require that arithmetic operations be performed. Addition is the most important operation because the other three operations (subtraction, multiplication, and division) can be accomplished using addition. Here is how to add two BCD numbers:

1. Add the two numbers, using the rules for binary addition given before.

2. If a four-bit sum is equal to or less than 9, it is a valid BCD number.

3. If a four-bit sum is greater than 9, or if a carry-out of the group is generated, it is an invalid result. Add 6 (0110_2) to the four-bit sum in order to skip the six invalid states and return the code to 8421. If a carry results when 6 is added, simply add the carry to the next four-bit group.

Several examples illustrate BCD addition for the case in which the sum of any four-bit column does not exceed 9.

Example: Add the following BCD numbers:

(a) 0011   3   (b) 0110   6   (c) 0010 0011   23
  +0100   +4   +0010   +2   0001 0101   +15
   0111   7   1000   8   0011 1000   38

(d) 1000   0110   86   (e) 0100 0101 0000   450
     0001   0011   +13   +0100 0001 0111   +417
     1001   1001   99   1000 0110 0111 867_{10}

(f) 1000 0111 0011   873

$$+\underline{0001} \quad \underline{0001} \quad \underline{0010} \qquad +\underline{112}$$

$$1001 \quad 1000 \quad 0101 \qquad 985_{10}$$

Note that in each case the sum in any four bit column does not exceed 9, and the results are valid BCD numbers.

Next, we deal with the case of an invalid sum (greater than 9 or a carry) by illustrating the procedure with several examples.

Example: Add the following BCD numbers:

(a)

1001		9
+0100		+4
1101	Invalid BCD number (>9)	13_{10}
+0110	Add 6.	
0001 0011	Valid BCD number.	
1 $\qquad$ 3$_{10}$		

(b)

1001		9
+1001		+9
1 $\quad$ 0010	Invalid because of carry	18_{10}
+0110	Add 6.	
0001 1000	Valid BCD number.	
1 $\qquad$ 8$_{10}$		

(c)

0001 $\quad$ 0110		16
+0001 $\quad$ 0101		+15
0010 $\quad$ 1011	Right group is invalid (>9)	31_{10}
	Left group valid. Add 6 to invalid code.	
0001 $\quad$ +0110	Add carry, 0001 to next group	
0011 $\quad$ 0001	Valid BCD number.	
3 $\qquad$ 1$_{10}$		

(d)

0110 $\quad$ 0111		67
+0101 $\quad$ 0011		+53
1011 $\quad$ 1010	Both groups are invalid (>9).	120_{10}
+0001 $\quad$ 0110 $\quad$ +0110	Add 6 to both groups	
0001 $\quad$ 0010 $\quad$ 0000	Valid BCD number.	
1 $\qquad$ 2 $\qquad$ 0$_{10}$		

HEXADECIMAL NUMBERS

The hexadecimal system has a base of sixteen; that is, it is composed of 16 digits and characters. Many digital systems process binary data in groups that are multiples of four bits, making the hexadecimal number very convenient because each hexadecimal digit represents a four-bit binary number (as listed in Table below).

Decimal	Binary	Hexadecimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

BINARY-TO-HEXADECIMAL CONVERSION

Converting a binary number to hexadecimal is a straightforward procedure. Simply break the binary number into four-bit groups starting at the binary point, and replace each group with the equivalent hexadecimal symbol.

Example: Convert the following binary numbers to hexadecimal:

(a) 1100101001010111_2 (b) $11111100010110 1001_2$

(c) 1110011000.111_2

(a) 1100 1010 0101 0111_2 (b) 0011 1111 0001 0110 1001_2
       C   A   5 7_{16} 3   F   1   6 9_{16}

(c) 0011 1001 1000 . 1110_2
       3   9   8 . E_{16}

HEXADECIMAL-TO-BINARY CONVERSION

To convert from a hexadecimal number to a binary number, reverse the process and replace each hexadecimal symbol with the appropriate four bits.

Example: Determine the binary numbers for the following hexadecimal numbers:

  (a) $10A4_{16}$ (b) $CF83_{16}$ (c) 9742_{16} (d) $D2E.8_{16}$

(a).   1   0   A 4_{16} (b).   C   F   8 3_{16}

     1   0000   1010 0100_2 1100   1111   1000   0011

(c).   9   7   4 2_{16} (d).   D   2   E   . 8_{16}

     1001   0111   0100   0010   1101   0010   1110   .   1000

The use of letters to represent quantities may seem strange at first, but keep in mind that any number system is only a set of sequential symbols. If we understand what these symbols mean in terms of quantities represented, then the form of the symbols themselves is unimportant once we get accustomed to using them.

It should be clear that it is much easier to write the hexadecimal number than the equivalent binary number, and since conversion is so easy, the hexadecimal system is a "natural" for representing binary numbers and digital codes.

COUNTING IN HEXADECIMAL

How do we count in hexadecimal once we get to F? simply start over with another column and continue as follows:

10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F,

20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, 2E, 2F,

30, 31, and so on.

With two hexadecimal digits, we can count up to FF_{16}, which is 255_{10}. To count beyond this, three hexadecimal digits are needed. For instance, 100_{16} is decimal 256_{10}, 101_{16} is decimal 257_{10}, and so on. The maximum three-digit hexadecimal number is FFF_{16}, or 4095_{10}. The maximum four-digit hexadecimal number is $FFFF_{16}$, which is $65,535_{10}$.

HEXADECIMAL-TO-DECIMAL CONVERSION

One way to evaluate a hexadecimal number in terms of its decimal equivalent is to first convert the hexadecimal number to binary and then convert from binary to decimal. The following example illustrates this procedure.

Example: Convert the following hexadecimal numbers to decimal:

        (a) $1C_{16}$ (b) $A85_{16}$

(a).   1 C_{16} (b).   A   8 5_{16}

     0001 1100_2 1010 1000 0101_2

     $2^4 + 2^3 + 2^2$ $2^{11} + 2^9 + 2^7 + 2^2 + 2^0$

     $16 + 8 + 4$ $2048 + 512 + 128 + 4 + 1$

     28_{10} 2693_{10}

Another way to convert a hexadecimal number to its decimal equivalent is by multiplying each hexadecimal digit by its weight and then taking the sum of these products. The weights of a hexadecimal number are increasing powers of 16 (from right to left). For a four-digit hexadecimal number the weights are:

16^3	16^2	16^1	16^0
4096	256	16	1

The following example shows this conversion method.

Example: Convert (a) $E5_{16}$ and (b) $B2F8_{16}$ to decimal.

(a) $E5_{16} = E \times 16^1 + 5 \times 16^0 = 14 \times 16 + 5 \times 1 = 224 + 5 = 229_{10}$.

(b) $B2F8_{16} = B \times 16^3 + 2 \times 16^2 + F \times 16^1 + 8 \times 16^0 = 14 \times 16 + 5 \times 1$

$$= 11 \times 4096 + 2 \times 256 + 15 \times 16 + 8 \times 1 = 45816_{10}.$$

DECIMAL-TO-HEXADECIMAL CONVERSION

Repeated division of a decimal number by 16 will produce the equivalent hexadecimal number formed by the remainders of each division. This is similar to the repeated division-by-2 for decimal-to-binary conversion and repeated division-by-8 for decimal-to-octal conversion.

The following example illustrates this procedure.

Example: Convert 650_{10} to hexadecimal by repeated division by 16_{10}.

$$
\begin{array}{r}
40 \\
16\,\overline{)650} \\
\underline{640} \\
10 \quad \rightarrow \quad A \quad \text{(LSD)} \\
\end{array}
$$

$$
\begin{array}{r}
2 \\
16\,\overline{)40} \\
\underline{32} \\
\end{array}
$$

$$8 \quad \rightarrow \quad 8$$

$$0$$

$$16\sqrt{2}$$

$$\underline{0}$$

$$2 \quad \rightarrow \quad 2 \quad \text{(MSD)}$$

Therefore, $650_{10} = 28A_{16}$

SUMMARY

- Number system is the coded language to understand the instructions and data of the protection system.

- Binary number system is a conversion of any decimal value into two characters 1s & 0s.

- Hexadecimal number system is a conversion of any decimal value into 16 characters (0, 1, 2, 3, 9, A, B, C, D, E, & F).

- Any numerical value can be converted from one number system to another.

REVIEW EXERCISE

Circle the letter a, b, c or d that correctly completes the statement and follow the directions to answer the other questions:

1. Convert the following Binary numbers to Decimal:

     a. 100101101

     b. 11100.1001

2. Convert the following Decimal numbers to Binary:

     a. 127_{10}

     b. 38.3125_{10}

     c. 23.25_{10}

3. Convert the following Decimal numbers to 8421 BCD Code:

     a. 1049_{10}

     b. 267_{10}

4. Perform the following Additions:

     a. $00010110_2 + 00010101_2$

     b. $01100111_2 + 01010011_2$

5. Convert the following 8421 BCD Code numbers to Decimal:

    a. $1010 \ 1100 \ 0100_2$

    b. $0111 \ 0001 \ 0100 \ 0011_2$

6. Convert the following numbers to Hexadecimal:

    a. 215.0625_{10}

    b. $1111 \ 0100 \ 1111.101101_2$

7. Convert the following Hexadecimal numbers to Decimal:

    a. $7A.F_{16}$

    b. $CF83_{16}$

8. Perform the following Operations:

    a. $1011_2 + 01101_2$

    b. $1001_2 - 0111_2$

    c. $1011_2 \times 1001_2$

    d. $1100_2 \div 011_2$

LESSON 3.2

LOGIC GATES & DIGITAL INTEGRATED CIRCUITS

LESSON 3.2

LOGIC GATES & DIGITAL INTEGRATED CIRCUITS (ICs)

OVERVIEW

This lesson discusses the types and function of logic gates. It browses the elementary structures of integrated circuits, which operate as logic gates.

OBJECTIVES

Upon completion of this lesson, the trainees will be able to:

- Understand the elementary structure of AND & OR logic gates.

- Identify the function and applications of AND & OR logic gates.

- Identify the function and applications of NAND & NOR logic gates.

- Demonstrate the function and applications of NOT logic gate.

- Identify the function and applications of X-OR & X-NOR logic gates.

INTRODUCTION

A logic gate is an elementary building block of a digital circuit. Most logic gates have two or more inputs and only one output. At any given moment, every terminal is in one of the two binary conditions low (0) or high (1), represented by two voltage levels. The logic state of a terminal can, and generally does, change often, as the circuit processes data.

In most logic gates, the low state is approximately zero volts (0V), while the high state is approximately five volts positive (+5V).

There are seven basic logic gates: AND, OR, X-OR, NOT, NAND, NOR and X-NOR.

AND Gate

The AND gate performs logical multiplication, more commonly known as the AND function. It is composed of two or more inputs and a single output, as indicated by the standard logic symbols shown in Fig. 3.2-1.

Any zero gives zero, all one's give one.

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

$$A \cdot B = Y$$

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

$$A \cdot B \cdot C = Y$$
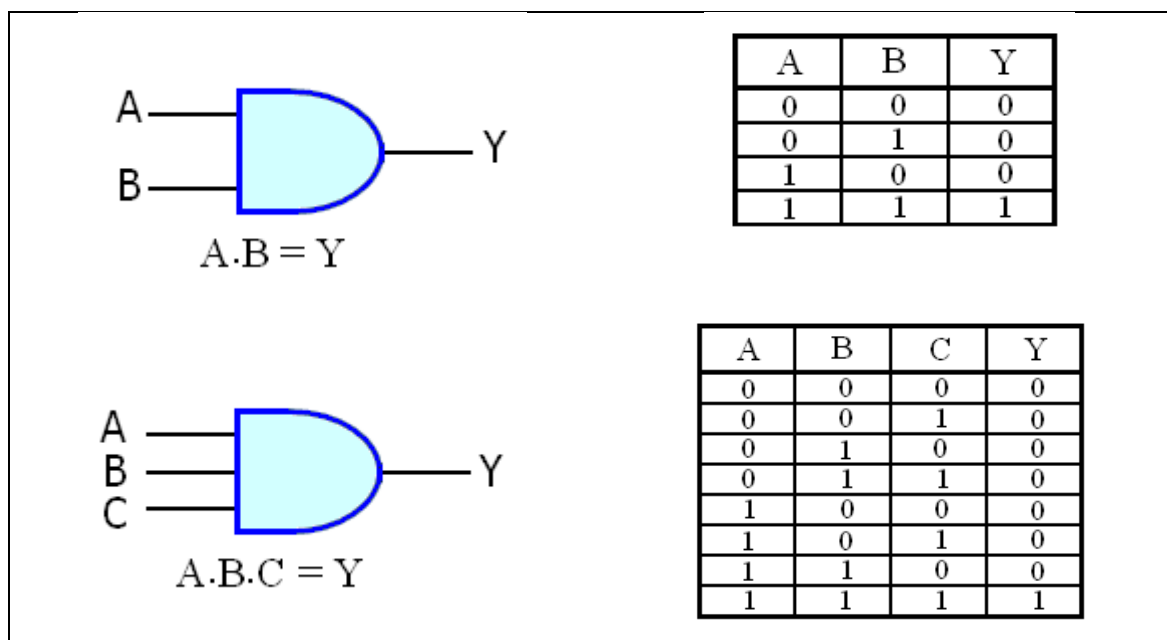
Fig. 3.2-1 Standard Logic Symbols for 2 & 3-Inputs AND Gate with Truth Table

AND Gate Representation

Fig. 3.2-2 shows representation of AND gates using switches, diodes and transistor. In (A), the lamp is ON when switch A AND switch B are closed, the output at (C) is high when the voltages (signals) A AND B are high; in (C), the output at C is high when switch-A AND switch-B are closed.
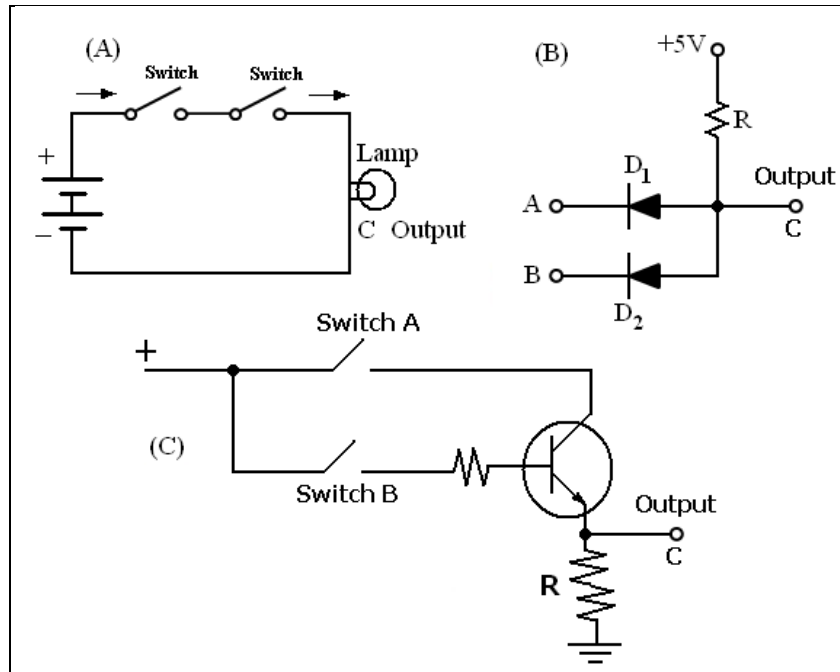
Fig. 3.2-2 Examples of AND Gate

EXAMPLE: If the two waveforms are applied to the AND gate as in Fig. 3.2-3, what is the resulting output waveform?
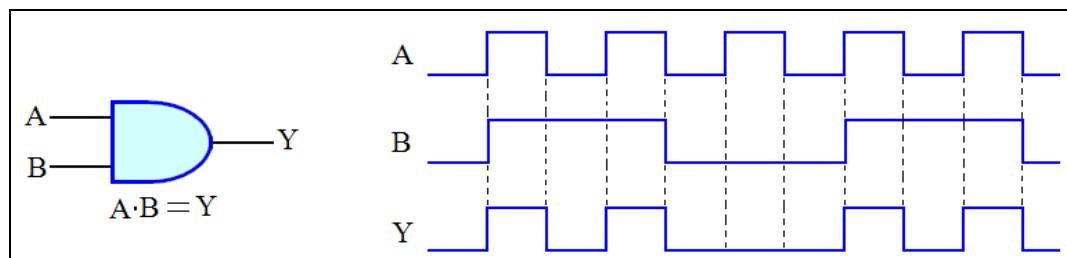
Fig. 3.2-3 Timing Diagram of 2-Inputs AND Gate

It is very important, when analyzing the pulsed operation of logic gates, to pay very careful attention to the time relationship of all the inputs with respect to each other and with respect to the output.

EXAMPLE

For the three-input AND gate in Fig. 3.2-4, determine the output waveform in proper relation to the inputs.
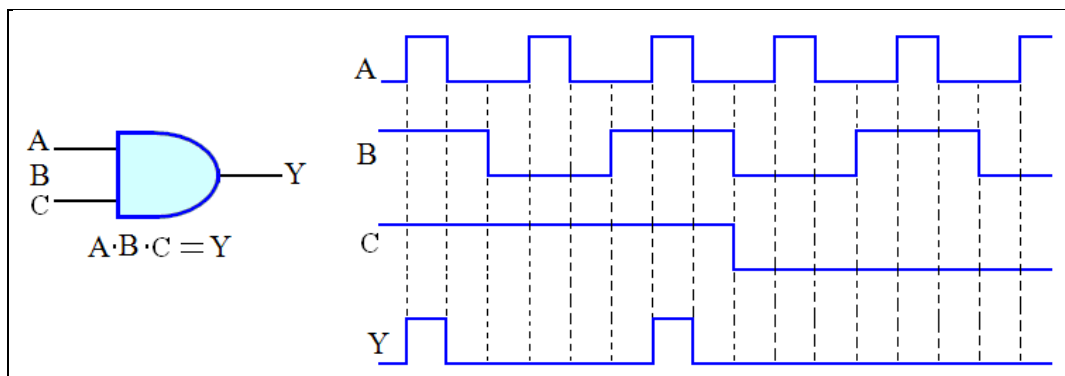
Fig. 3.2-4 Timing Diagram of 3-Inputs AND Gate

Referring to Fig. 3.2-4, the output of a three-input AND gate is HIGH only when all three inputs are HIGH.

AND Gate Applications

In a simple application, an AND gate can be used to detect the presence of a specified number of conditions and, in response, to initiate an appropriate action.

For example, an automobile's safety system may require that an audible signal be produced to warn the driver that the seat belt is not engaged. The conditions for this are that the ignition switch be on, the seat belt be unbuckled, and the warning signal last for a specified time and then turn off automatically. The first two conditions can be represented by switch positions and the third by a timing circuit. Fig. 3.2-5 shows an AND gate whose HIGH output activates a buzzer when these three conditions are met on its inputs. When the ignition switch is represented by S_1 in Fig. 3.2-5, is on, a HIGH is connected to the gate input A.

When the belt is not properly buckled, switch S_2 is off and a HIGH is connected to the gate input B. At the instant the ignition switch is turned on, the timer is activated and produces a HIGH on gate input C. The resulting HIGH gate output activates the alarm. After a specified time, the timer output goes LOW, disabling the AND gate and turning off the alarm. If the seat belt is buckled when the ignition is turned on, a LOW is applied to input B, keeping the gate output LOW, thus preventing the alarm from sounding.
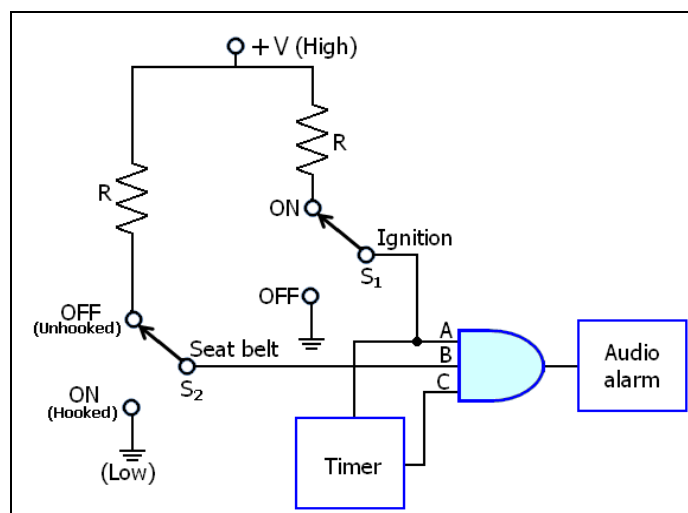
Fig. 3.2-5 Example of an AND gate application

OR Gate

The OR gate performs logical addition, more commonly known as the OR function. An OR gate has two or more inputs and one output, as indicated by the standard logic symbols in Fig. 3.2-6, with two and three inputs OR gates associated with truth tables.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1
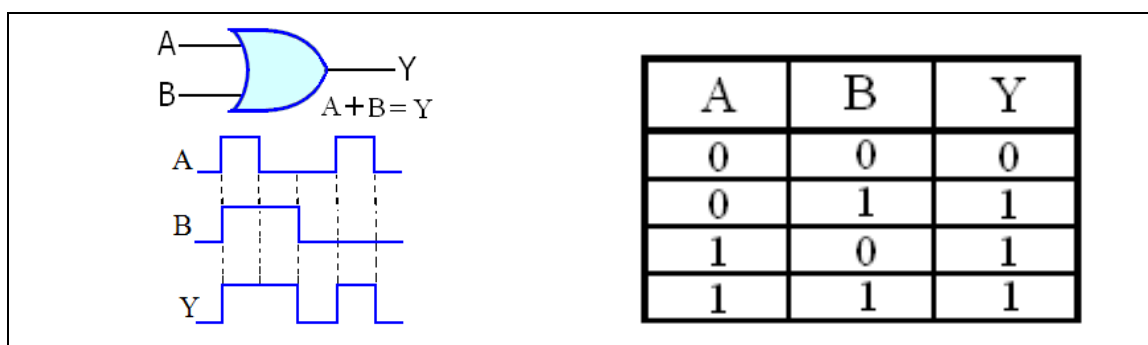
Fig. 3.2-6 2-Input OR Gate with Timing Diagram and Truth Table

It should be noted that the output of OR gate is high when any of the inputs are high.

EXAMPLE: For the three-input OR gate in Fig. 3.2-7, determine the output waveform in proper relation to the inputs.
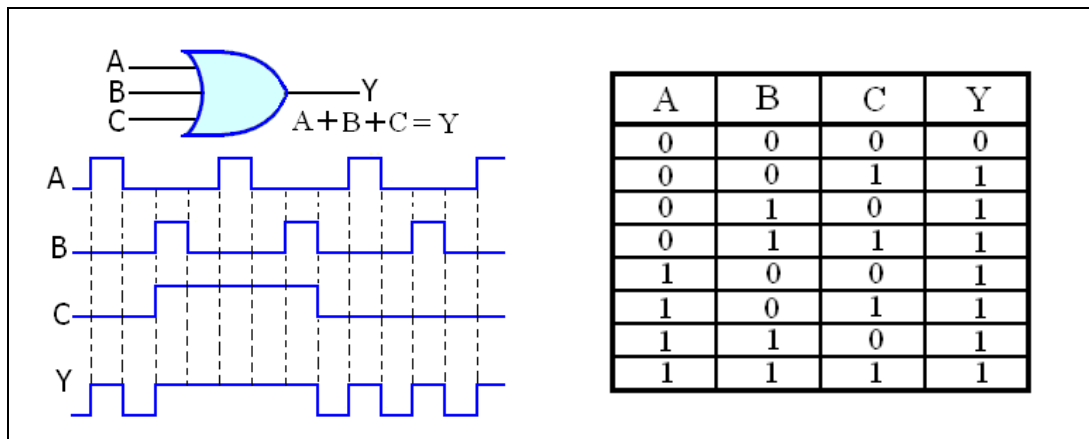
Fig. 3.2-7 Triple-Input OR Gate with Timing Diagram and Truth Table

Referring to Fig. 3.2-7, the output is HIGH when any of the inputs are HIGH.

OR Gate Representation

The OR logic gate can be represented by diodes, switches or transistor, (Fig. 3.2-8).
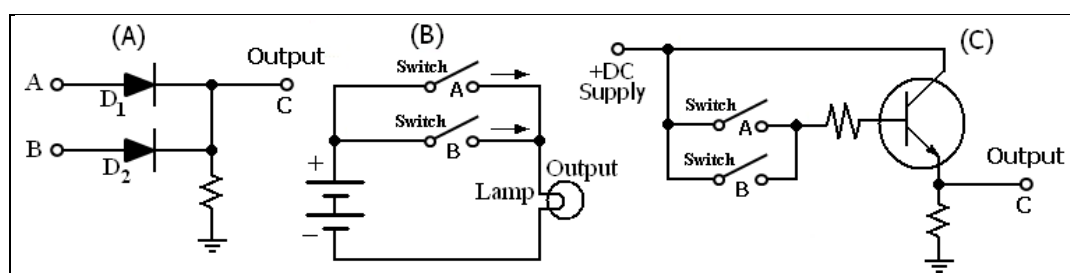
Fig. 3.2-8 OR Gate Representation

OR Gate Application

As an example application of an OR gate, let us assume that in a room with three doors, an indicator lamp must be turned on when any of the doors is not completely

closed. The sensors are switches that are open when a door is ajar or open. This open switch creates the HIGH level for the OR gate input, as shown in Fig. 3.2-9. If any or all of the doors are open, the gate output is HIGH. This HIGH level is then used to illuminate the indicator lamp. The gate is capable of supplying sufficient current to the lamp.
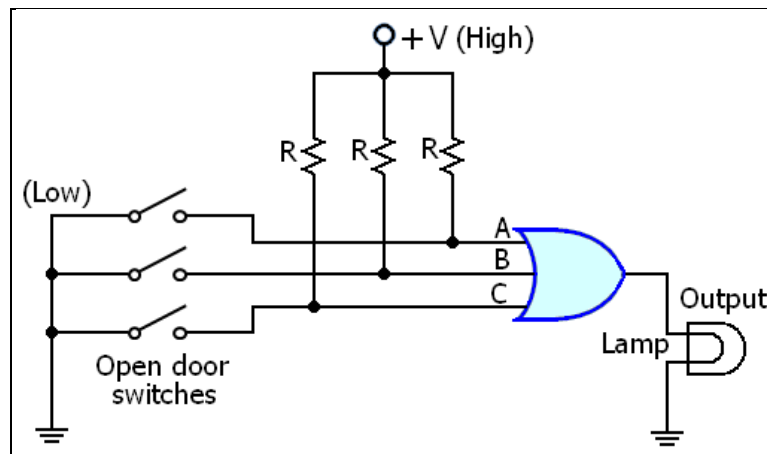
Fig. 3.2-9 Application of OR Gate

INVERTER (NOT Gate)

The inverter (NOT circuit) performs a basic logic function called **inversion** or **complementation**. The purpose of the inverter is to change one logic level to the opposite level. In terms of bits, it changes a 1 to a 0 and a 0 to a 1. The standard logic symbol for the inverter is shown in Fig. 3.2-10.

Input A	Output Y
0	1
1	0
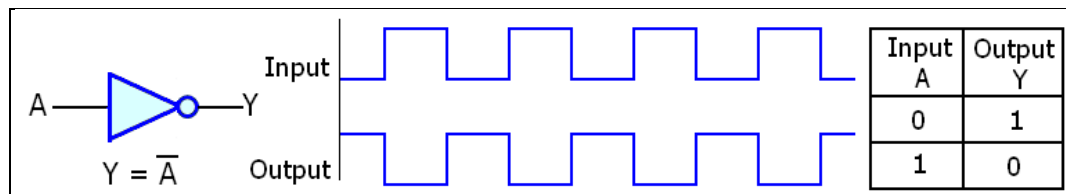
Fig. 3.2-10 Inverter Gate with Truth Table and Timing Diagram

NOT Gate Representation
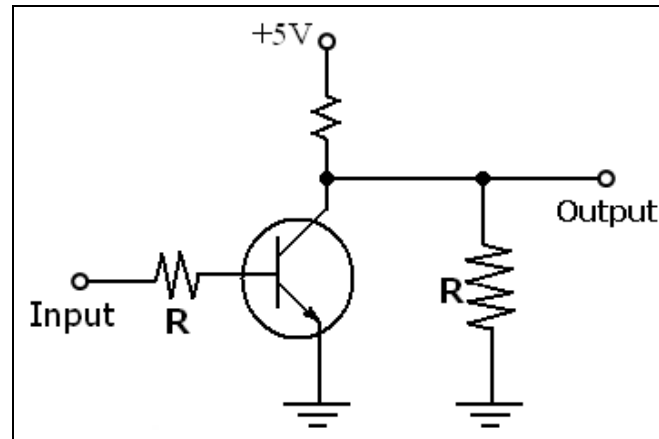
Fig. 3.2-11 Transistor Representation of NOT Function

NAND Gate

The term NAND is a abbreviation of NOT-AND and implies an AND function with a complemented (inverted) output. A standard logic symbol for a two-input NAND gate and its equivalency to an AND gate followed by an inverter are shown in Fig. 3.2-12.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0
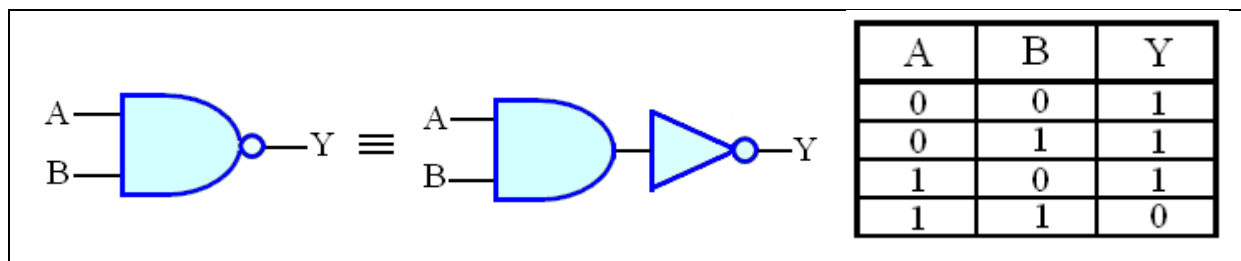
Fig. 3.2-12 NAND Gate Equivalent Logic Symbol and Truth Table

Note: 1 = High; 0 = Low.

The NAND gate is a very popular logic function because it is a "universal" function; that is, it can be used to construct an AND gate, an OR gate, an inverter, or any combination of these functions.

Timing Diagram for NAND Gate

EXAMPLE

If the two waveforms shown in Fig. 3.2-13 are applied to the NAND gate, determine the resulting output waveform.
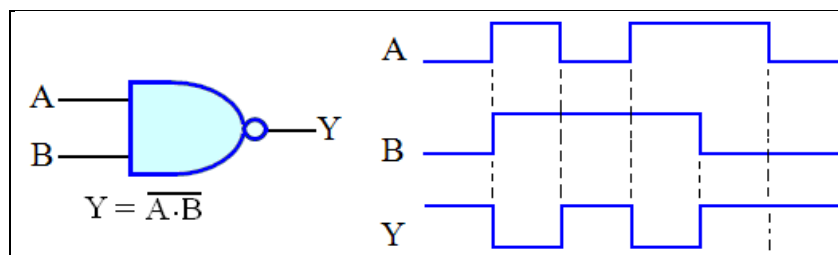
Fig. 3.2-13 Timing Diagram for 2-Inputs NAND Gate

NOR Gate

The term NOR is a abbreviation of NOT-OR and implies an OR function with an inverted output. A standard logic symbol for a two-input NOR gate and its equivalent OR gate followed by an inverter are shown in Fig. 3.2-14.

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

$$Y = \overline{A+B+C}$$
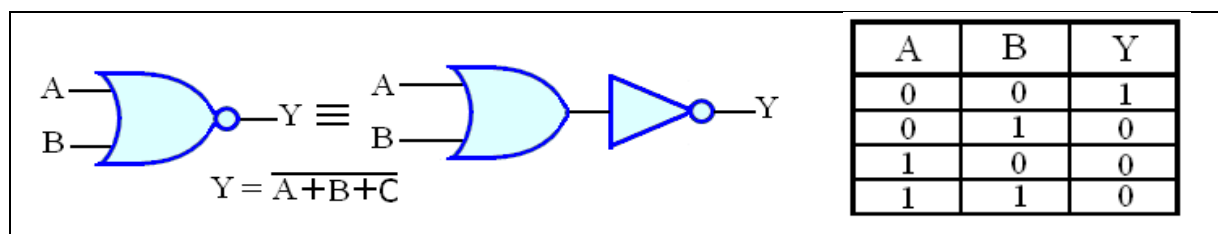
Fig. 3.2-14 Standard NOR Gate Logic Symbols and Truth Table

EXAMPLE

If the two waveforms shown in Fig. 3.2-15 are applied to the NOR gate, what is the resulting output waveform?
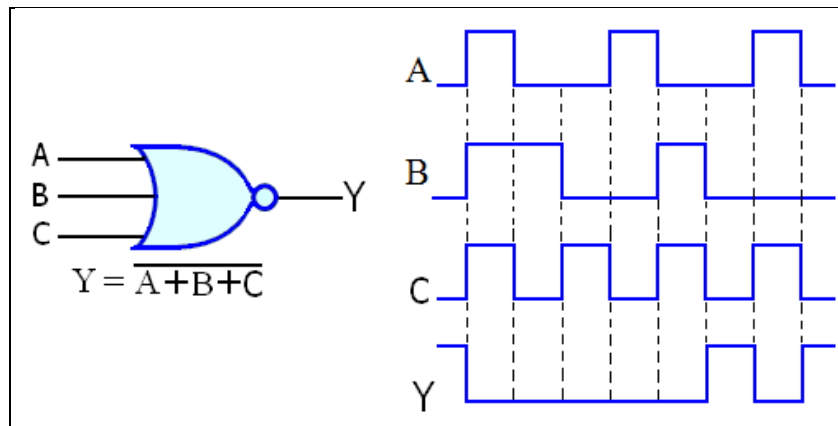
Fig. 3.2-15 Timing Diagram of 3-Inputs NOR Gate

Whenever any input of a NOR gate is HIGH, the output is LOW (Fig 3.2-15).

EXCLUSIVE-OR (X-OR) Gate

X-OR gate is used to produce logic 1 when the input 1s are odd numbers, or to produce logic 0 when the input 1s are even numbers.
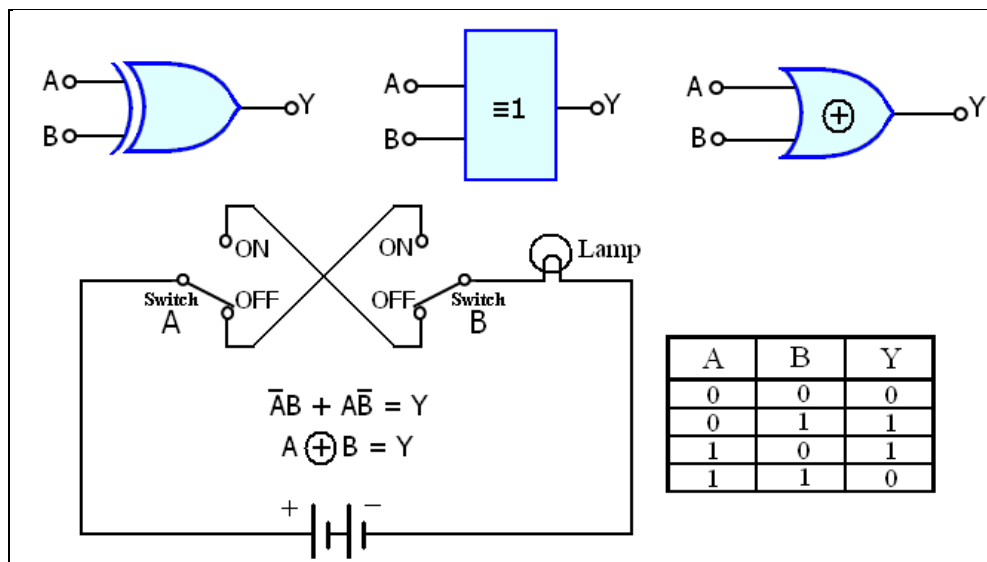
Fig. 3.2-16 Representation of 2-Inputs X-OR Logic Gate

The lamp lights in Fig. 4.2-16 if switch B is set at "ON" and switch A at "OFF" or switch A at "ON" and switch B at "OFF".

Exclusive OR function can be performed in using the following logic function (Fig. 3.2-17).
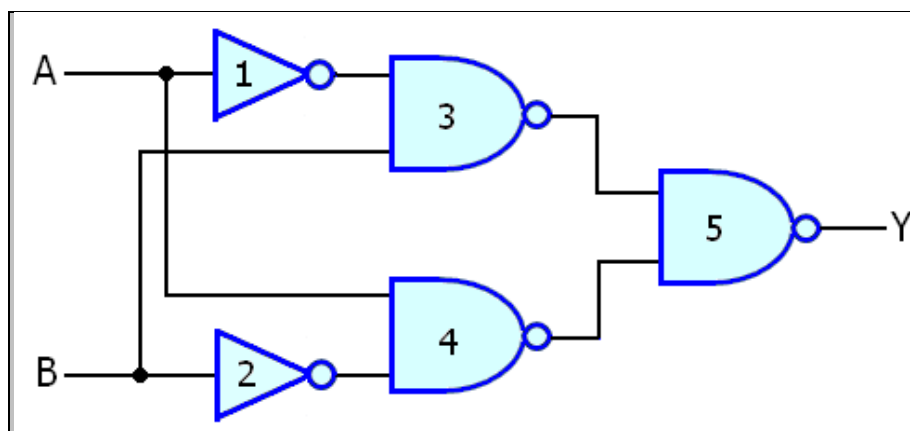
Fig. 3.2-17 Equivalent Circuit of X-OR Gate

X-NOR Gate

The X-NOR gate (NOT exclusive-OR) is an exclusive OR gate with the output inverted. It is used to produce logic 1 when the input 1s are even numbers, or to produce logic 0 when the input 1s are odd numbers, as shown in Fig. 3.2-18.

$$Y = \overline{A \oplus B}$$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1
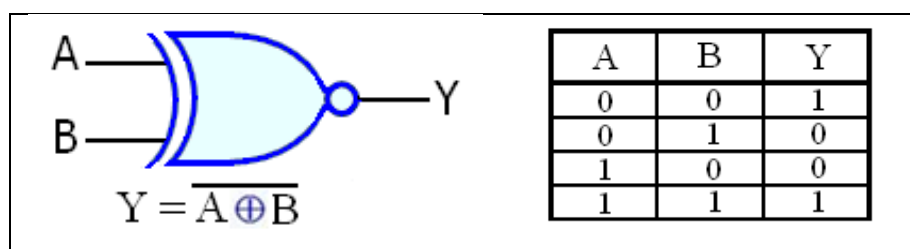
Fig. 3.2-18 X-NOR Gate and Truth Table

Transistor-Transistor Logic (TTL) Logic Family

Quad 2 input NAND gates are packed in a single integrated circuit. It has the same truth table as the NAND circuit you learnt. The industry-standard IC NAND gate (7400) has four complete NAND circuits inside a single IC package. All four circuits are separate. Only the ground and power connections are common to all NAND gates.

Fig. 3.2-19 shows the IC lead connections and the schematic for each NAND gate. The circuit schematic shows that more parts are used including many transistors. By using the IC NAND gate, the size of the unit can often be made much smaller.
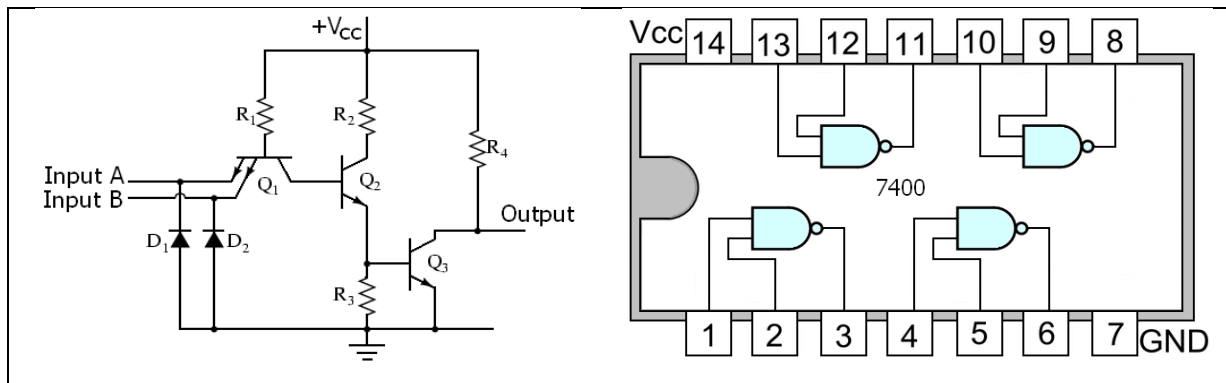
Fig. 3.2-19 Logic NAND Circuit Schematic and Pin-out

Families of Logic Circuits

The logic functions can be achieved by applying the following elements. Accordingly, the family of logic circuit is named. Diode-Transistor Logic (DTL) incorporates diodes and transistors to achieve the logic function. Transistor-Transistor Logic (TTL) incorporates transistors. Transistor-Transistor Logic (TTL), a widely used family of digital devices. TTL is fast, inexpensive, and easy to use.

Complementary Metal Oxide Semiconductor (CMOS) Family
FET & MOSFET

Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) or FETs can be either P-type or N-type devices and they are smaller and consume less power than bipolar transistors. Because of the FETs small size and low power capabilities, they are preferred in digital integrated circuitry. The N-type and P-type FETs, during manufacturing can be combined in the same package to form a complementary pair. The pair is called a CMOS device. CMOS technology reduced the amount of circuitry required and the size of the components, (Fig. 3.2-20).
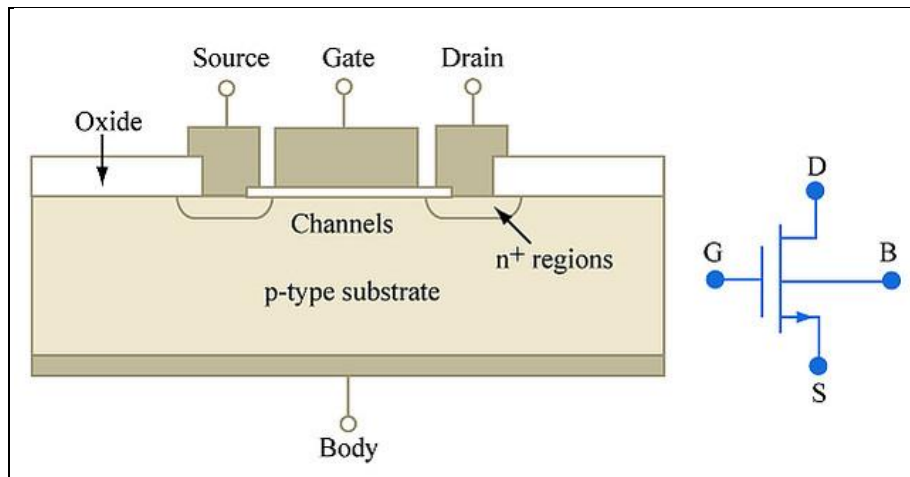
Fig. 3.2-20 N-channel Enhancement Mode MOSFET

Therefore, CMOS devices are smaller, consume less power, than either the bipolar transistor or FET, and have taken over a large share of the digital computer market. The only advantages the discrete bipolar transistor has over FETs and CMOS are their power handling capabilities and speed of operation. In digital computers, high power handling capability is not normally a requirement, or considered an advantage.

CMOS Characteristics

Supply voltage   :   +3 to +15 volts.

Power Dissipation :   10 microwatts (static)

Logic levels   :   binary 0 = 0 volts, binary 1 = $+V_{DD}$

Basic gate form   :   positive NOR/negative NAND

HEX INVERTER

This integrated circuit contains six inverters. After applying +5 V (the supply voltage for all TTL devices) to pin 14 and grounding pin 7, you can connect any or all of the inverters to other TTL devices. For instance, if you only need one inverter, you can connect an input signal to pin 1 and take the output signal from pin 2. The inputs of other unused inverters can be left unconnected or grounded for noise protection, (Fig. 3.2-21).
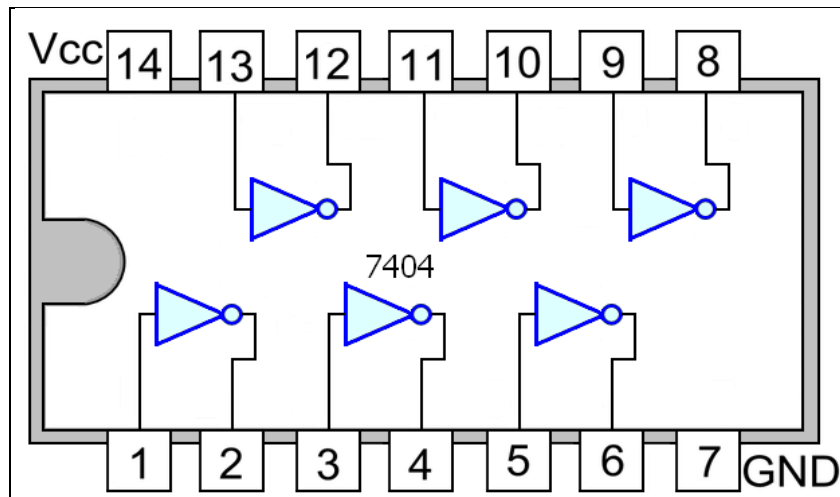
Fig. 3.2-21 Pin out Diagram of a TTL hex inverter (7404)

AND Gate

Several configurations of AND gates are available in IC form. The 7408 has four 2-input AND gates (quad 2-input AND); the 7411 has three 3-input AND gates (triple 3-input AND); and the 7421 has two 4-input AND gates (dual 4-input AND). These gates are shown in Fig. 3.2-22.
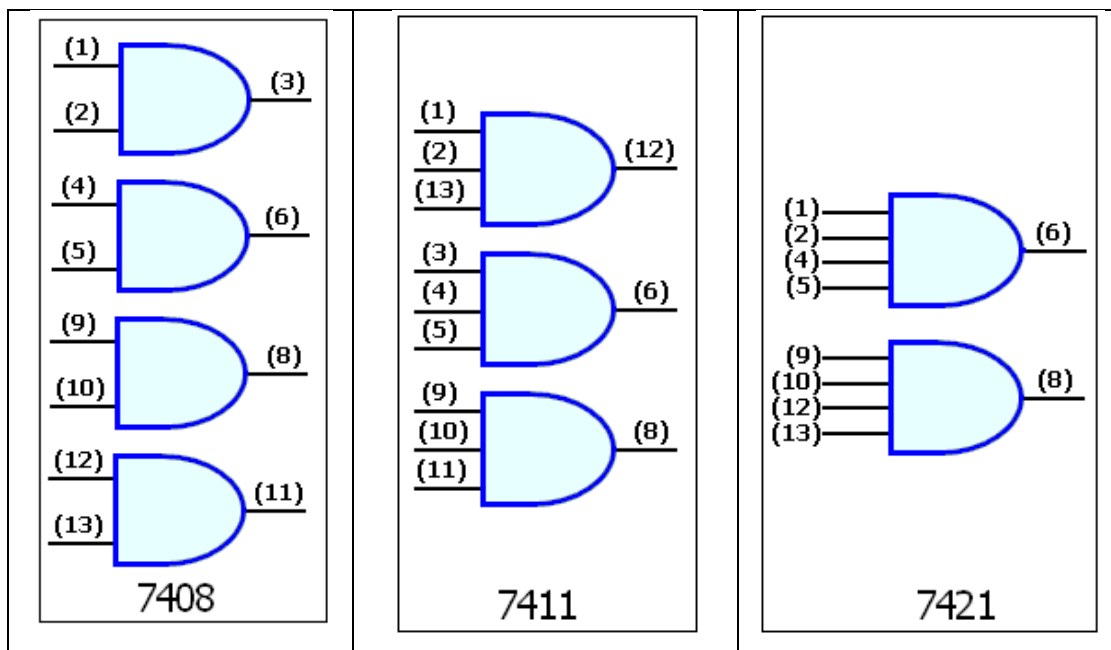
Fig. 3.2-22 Standard TTL AND Gates

NAND gate

A variety of NAND gates are available, including the 7400 with quad 2-input gates, the 7410 with three 3-input gates, the 7420 with two 4-input gates, (Fig. 3.2-23).

The 7430 with single 8-input gate, and the 74133 with single 13-input gate. These gates are shown in Fig. 3.2-24. The 74133 is in a 16-pin DIP.
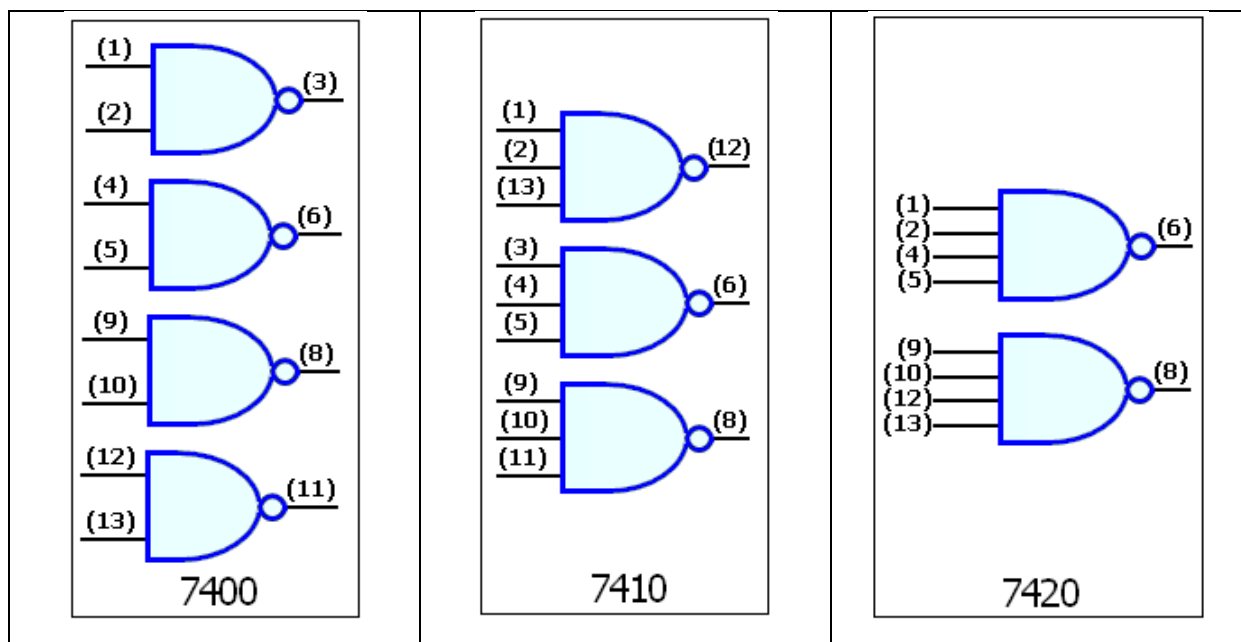
Fig. 3.2-23 Standard TTL NAND Gates
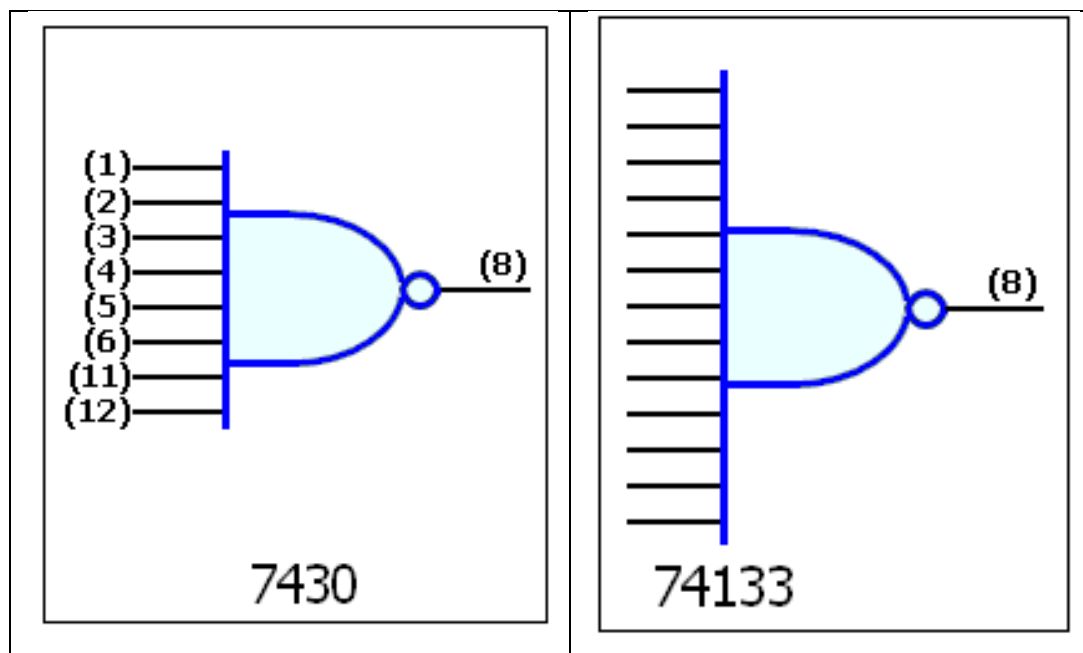
Fig. 3.2-24 Large Input Numbers of TTL NAND Gates

OR Gates

The 7432 has quad 2-input OR gates, as shown in Fig. 3.2-25.
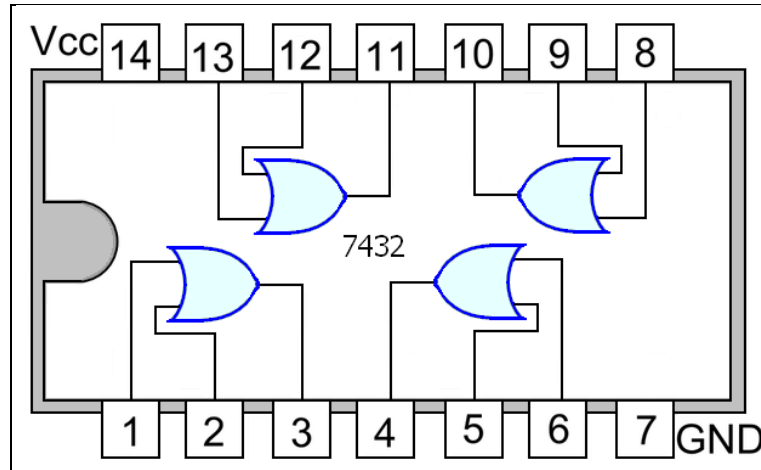
Fig. 3.2-25 7432 Quad 2-input OR Gates

NOR Gate

Examples of NOR gate configurations are shown in Figure 3.2-26. The 7402 has quad 2-input NOR gates, and the 7427 has triple-input gates.
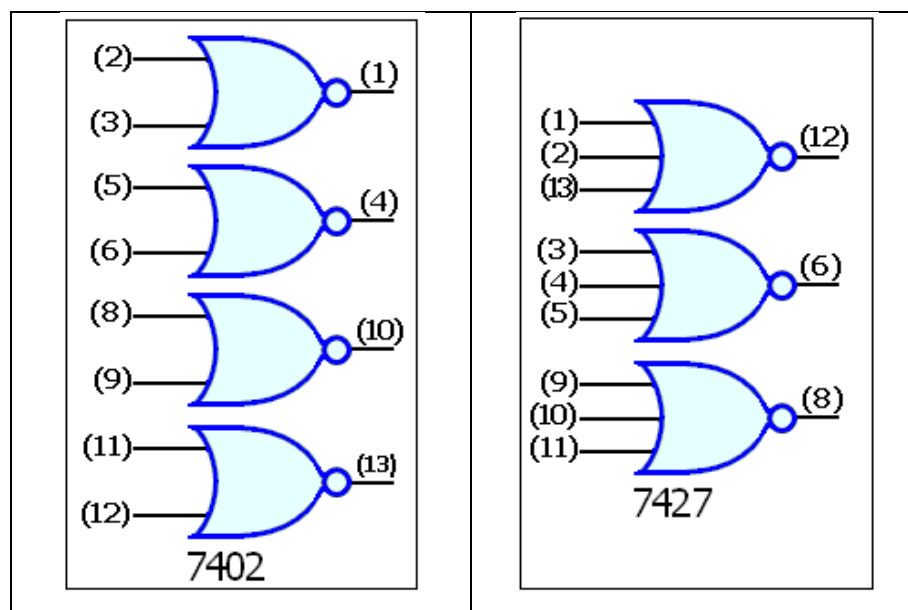
Fig. 3.2-26 Standard TTL NOR Gates

SUMMARY

- A logic gate is an elementary building block of a digital circuit.

- The AND gate performs logical multiplication, more commonly known as the AND function. It is composed of two or more inputs and one single output.

- The OR gate performs logical addition, more commonly known as the OR function. An OR gate has two or more inputs and one output.

- The inverter (NOT circuit) performs a basic logic function called inversion or complementation. The purpose of the inverter is to change one logic level to the opposite level.

- The term NAND consists of NOT-AND and implies an AND function with a complemented (inverted) output.

- The term NOR consists of NOT-OR and implies an OR function with an inverted output. A standard logic symbol for a 2-input NOR gate and its equivalent OR gate followed by an inverter.

- X-OR gate is a special gate. It is used when the logic desired is that only one of two states is true at any given time.

- The X-NOR gate (NOT exclusive-OR) is an exclusive OR gate with the output inverted.

- Transistor-Transistor Logic Circuit family is exclusively of Integrated Circuits (ICs) and is not possible with discrete components.

- The FET is a MOSFET (Metal Oxide Semiconductor Field-Effect Transistor). FETs can be either P-type or N-type devices and they are smaller and consume less power than bipolar transistors.

GLOSSARY

Quad 2-input gates:	Four similar gates with two inputs for each.
Triple 3-input gates:	Three similar gates with three inputs for each.
Drain:	Supply terminal.
Enhancement:	Development.
Truth table:	Operating roles.
IC:	Integrated circuit
Hex inverters:	Six similar inverter gates in one IC.

REVIEW EXERCISE

1.   Draw the symbol and truth table for a 3-input **AND Gate A, B, & C** and **X** is the output.

2.   Draw the symbol and truth table for 4-input **OR Gate** with inputs A, **B, C, & D** and **X** is the output.

3.   With a 3-input **AND Gate** having inputs **0, 1,** and **1** the output:

    a.   Binary **0**   b.   Binary **1**

4.   With a 4-input **NOR Gate** having inputs **1, 0, 1,** and **1** the output:

    a.   Binary **0**   b.   Binary **1**

5.   The figure shown is …………………
   a. Switch contact **AND Gate**.
   b. Switch contact **OR Gate**.
   c. Diode **OR Gate**.
   d. Diode **AND Gate.**
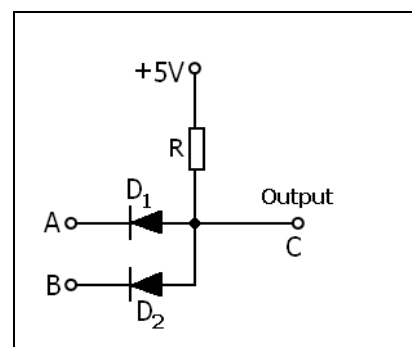
6. The ability of a logic circuit to reject unwanted signals is expressed as:

    a. noise margin.

    b. propagation delay.

    c. power dissipation.

    d. logic levels.

7. The most widely used high speed high power digital circuit is the:

    a. CMOS.

    b. MOS.

    c. TTL.

    d. ECL.

8. Draw the output waveform for the following two figures:
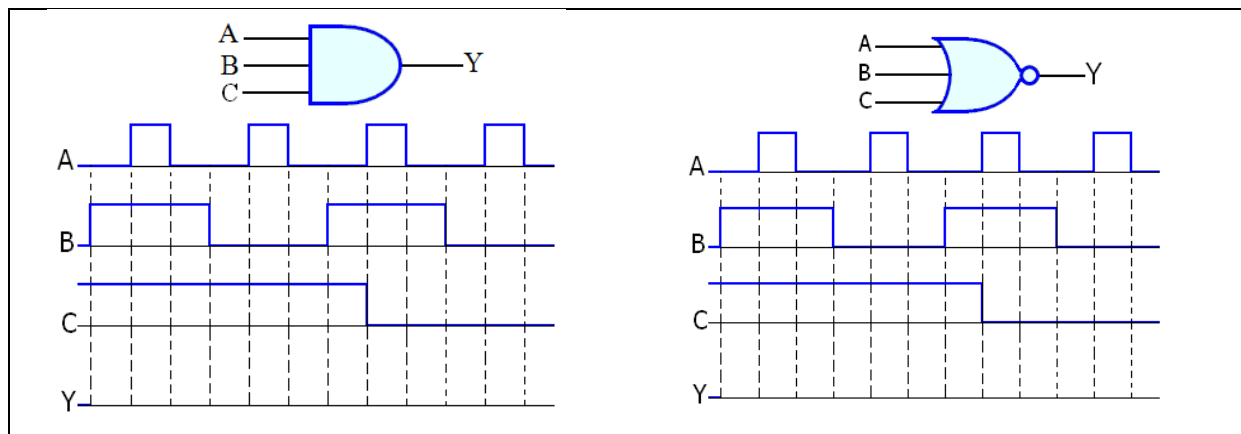
9. Name two families of logic circuits.

    a. ……………………………………   b. ………………………………………….

10. Draw the symbol and construct a truth table for Exclusive-NOR (X-NOR) gate with two inputs.

TASK 3.2-1

TTL Logic Gates

OBJECTIVE

Upon completion of this task, the trainees will be able to:

- Demonstrate the operation and applications of a TTL logic gates.

TOOLS, MATERIALS, & REQUIREMENTS

- Heathkit ET-3200 Digital Design Experimenter
- DC Voltmeter or logic probe.
- SN74LS00N (7400) quad-two input TTL integrated circuit (443-728).
- 1N4149 silicon diode (56-56).
- 560 ohm resistor.
- Personal safety equipment as recommended in digital electronic workshop.
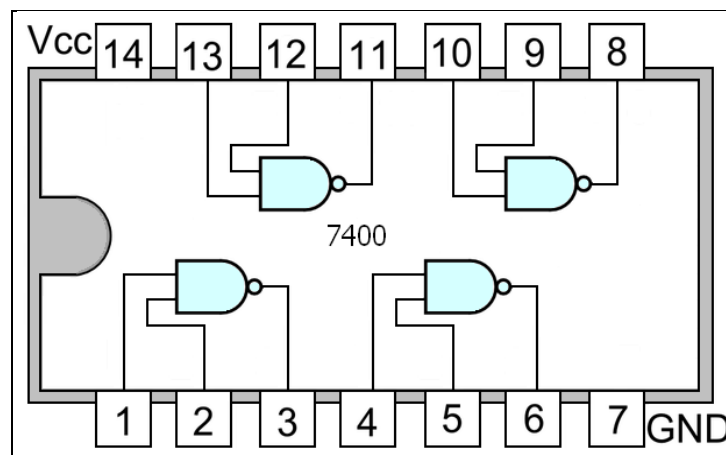
Fig. 1-1 Pin connections for 7400 TTL IC

PROCEDURE

1. Mount the 7400 TTL integrated circuit on the socket breadboard. Be sure that it is seated firmly straddling the notch in the socket and that none of the pins are bent.

Connect pin 14 to +5 volts and pin 7 to GND to power supply. Fig. 1-1 shows the pin connections.

2. Connect one of the four gates in the IC, as shown in Fig. 1-2. The input comes from data switch SW1. You will monitor the input and output states with the L1 and L2 LED indicators and your DC voltmeter.
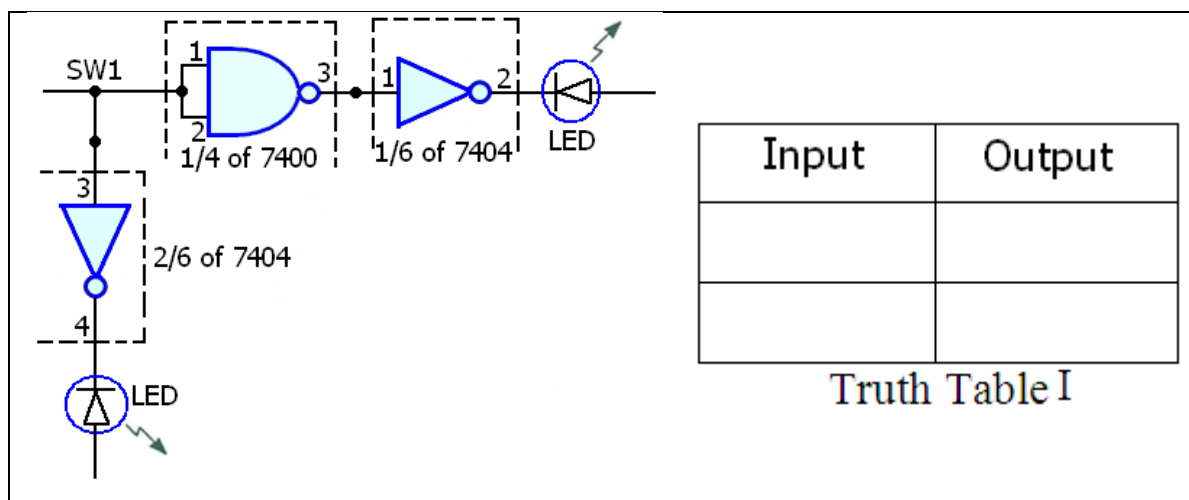
Fig. 1-2 7400 TTL Integrated Circuit used as Inverter

3. Set SW1 to the down position then the up position. Measure the DC input (pins 1 and 2) and output (pin 3) voltage for each position. Record your data in (Table I) by following the LED indicator input/output states.

4. Assuming positive logic, the output logic levels are:

    Binary 0 = _____ volts.

    Binary 1 = _____ volts.

5. Study Table I. What logic function is being performed?

    _____ .

6. Connect the diode-resistor circuit shown in Fig. 1-3 to the output of the TTL gate. This circuit simulates a load of about 7 TTL gate inputs. Again measure the input and output voltages of the circuit for both positions of SW1. Record your data in Table II.
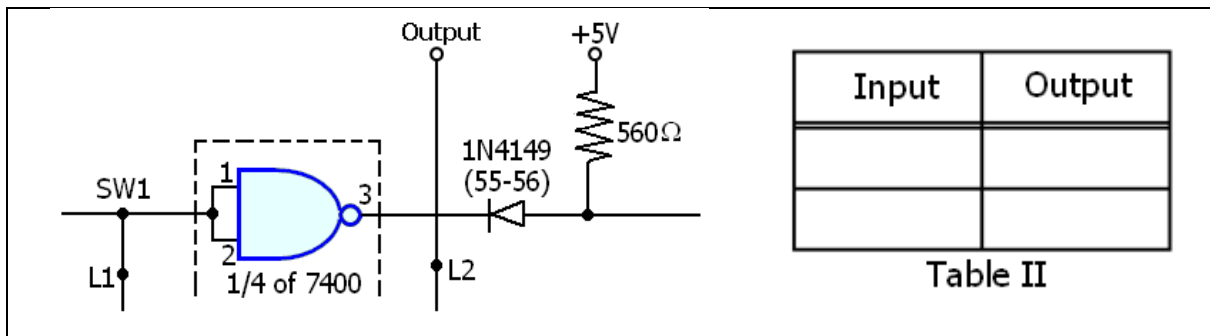
Fig. 1-3

7. Compare the output data in Tables I and II and account for any differences. Does the loading affect the binary 0 or binary 1 output state most? _____.

8. Wire the circuit shown in Fig. 1-4. Remove the 1N4149 and 560Ω resistor load used in the previous steps. The inputs come from SW1 and SW2. You will measure the output voltage C at pin 3 of the 7400 IC.
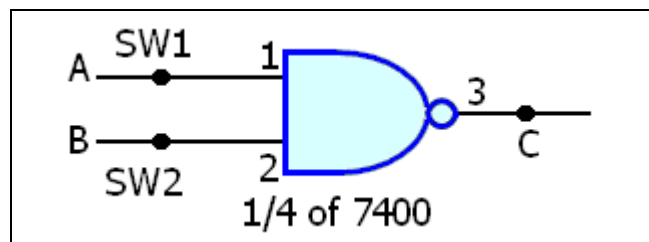
Fig. 1-4

9. With SW1 and SW2, apply the input voltages given in Table III.

Input		Output
A (SW1)	B (SW2)	C
0V	0V	
0V	+5V	
+5V	0V	
+5V	+5V	

Table III

A	B	C
0	0	
0	1	
1	0	
1	1	

Table IV

10. Using positive logic convert your electrical truth table of Table III into 1s and 0s in Table IV.

11. Study Table IV. What logic function is being performed? _____

12. Using negative logic, convert the data in Table III into 1s and 0s and record in Table V.

A	B	C

Table V

13. Study Table V. What logic function is being performed? _____ .

14. Remove the wires connecting pins 1 and 2 of the IC to SW1 and SW2. Let the gate input hang free. Note the output state.

    With open inputs, the TTL gate output is _____ volts or binary _____ for positive logic. This means that an open input acts like a binary _____.

15. Wire the circuit shown in Fig. 1-5. With SW1 (A) and SW2 (B), apply the states shown in Table VI. Record the state for each set of inputs. Observe LED indicators L1, L2, and L3 to obtain your input and output data. Use positive logic (binary 1 = ON, binary 0 = OFF).

16.

A	B	C
0	0	
0	1	
1	0	
1	1	

Table VI

Fig. 1-5

17. Study the circuit in Fig. 1-5 and the data in Table VI. What logic function is being performed? ……………………..

18. Connect the circuit shown in Fig. 1-6. Monitor the inputs and output on LED indicators L1, L2, and L3. With SW1 (A) and SW2 (B), apply the inputs shown in Table VII. Record the output state corresponding to each set of inputs. Use positive logic.

A	B	C
0	0	
0	1	
1	0	
1	1	
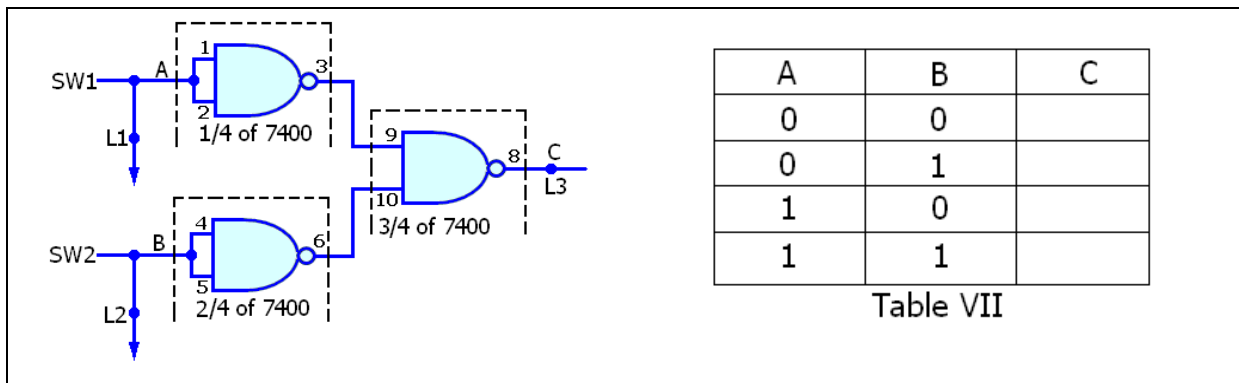
Table VII

Fig. 1-6

19. Study Fig. 1-6 and Table VII. What logic function is being performed?

20. Modify your circuit in Fig. 1-6 by adding the fourth gate in the 7400 to the output, as shown in Fig. 1-7. Only the output change is shown. The rest of the circuit stays as in Fig. 1-6.

A	B	C
0	0	
0	1	
1	0	
1	1	
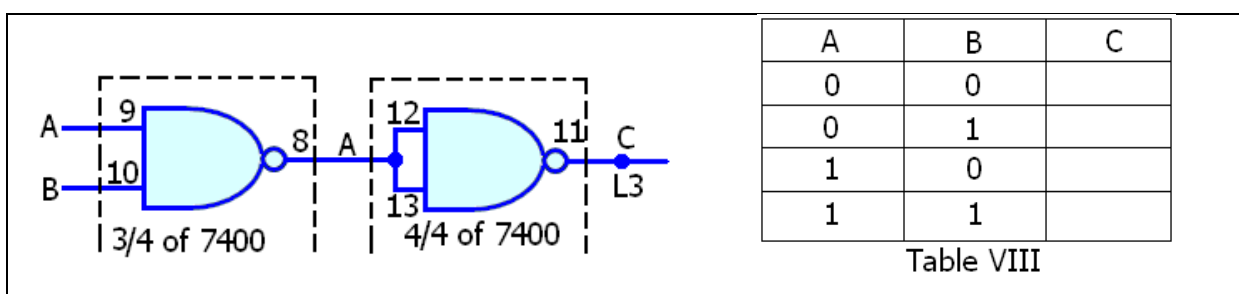
Table VIII

Fig. 1-7

21. Using SW1 (A) and SW2 (B) data switches and monitoring LED indicators L1, L2, and L3, apply the states shown in Table VIII. Record the output state for each set of inputs.

TASK 3.2-2

CMOS Logic Gates

OBJECTIVE

Upon completion of this task, the trainees will be able to:

- Demonstrate the operation and applications of CMOS logic gates.

TOOLS, MATERIALS, & REQUIREMENTS

- Heathkit ET-3200 Digital Design Experimenter.
- DC Voltmeter or logic probe.
- 1 - CD4001 AE (4001) quad two input.
- CMOS integrated circuit (443-695).
- Personal safety equipment as recommended in digital electronic workshop.

PROCEDURE

1. Mount the 4001 CMOS integrated circuit on the breadboard socket. Be sure that it is seated firmly straddling the notch in the socket and that none of the pins are bent. Connect pin 14 to +5 volts and pin 7 to GND to power supply. Fig. 2-1 shows the pin connections.
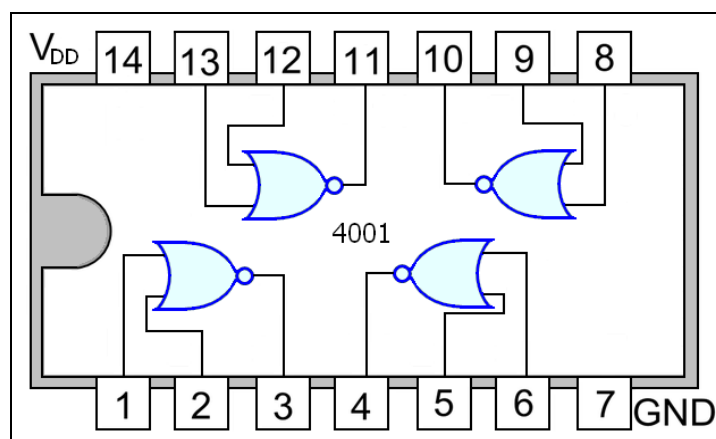
Fig. 2-1 Pin connections for 4001 CMOS IC

2. Connect one of the four gates in the IC, as shown in Fig. 2-2. The input comes from data switch SW1. You will measure the input and the output states with your DC voltmeter.

Input	Output
0	
1	
Table I	
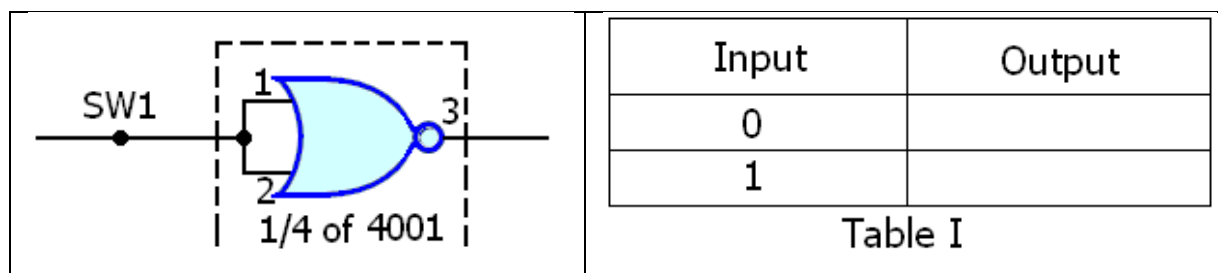
Fig. 2-2

3. Set SW1 first to the down position then the up position. Measure the DC input (pins 1 and 2) and output voltage (pin 3) for each position. Record your data in Table I.

4. Assuming positive logic, the output logic levels are:

    Binary 0 = _____ volts.

    Binary 1 = _____ volts.

5. Study Table I. What logic function is being performed? _____.

6. Wire the circuit shown in Fig. 2-3. The inputs come from SW1 and SW2. You will measure the output voltage C at pin 3 of the 4001 IC.

Input		Output
A (SW1)	B (SW2)	C
0V	0V	
0V	+5V	
+5V	0V	
+5V	+5V	
Table II		
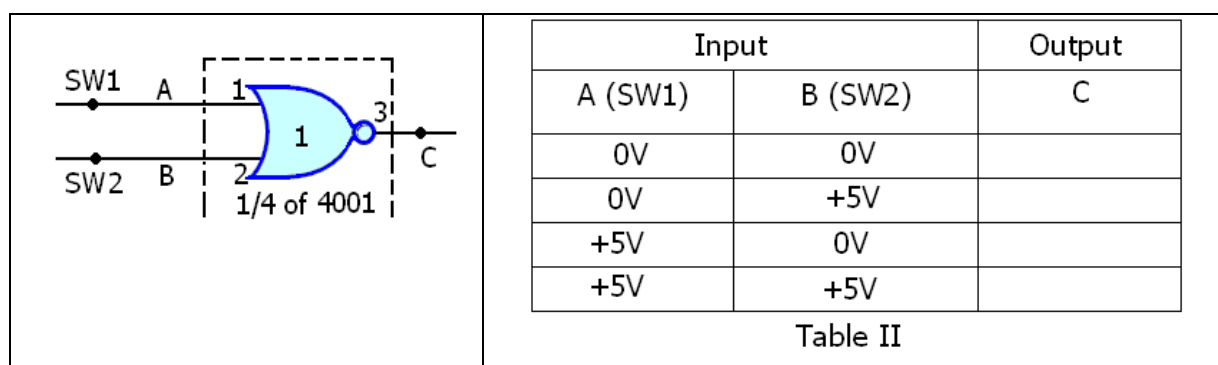
Fig. 2-3

7. With SW1 and SW2, apply the input voltages given in Table II. Measure and record the output voltage for each set of inputs.

8. Using positive logic, convert your electrical truth table in Table II into 1s and 0s in Table III.

A	B	C

Table III

9. Study Table III. What logic function is being performed? ……………………..

10. Using negative logic, convert the data in Table II into 1s and 0s and record in Table IV.

A	B	C

Table IV

11. Study Table IV. What logic function is being performed? ………………………

12. Remove the wire connecting pins 1 and 2 of the IC to SW1 and SW2. Let the gate inputs hang free. Measure the output voltage. With open inputs, the CMOS gate output is………………..volts or binary ……………… for positive logic. This means that an open input acts like a binary ……………………

13. Wire the circuit shown in Fig. 2-4 with SW1 (A) and SW2 (B); apply the input states shown in Table V. record the output state for each set of inputs. Observe LED indicators L1, L2, and L3 to obtain your input and output data. Use positive logic (binary 1 = ON, binary 0 = OFF).
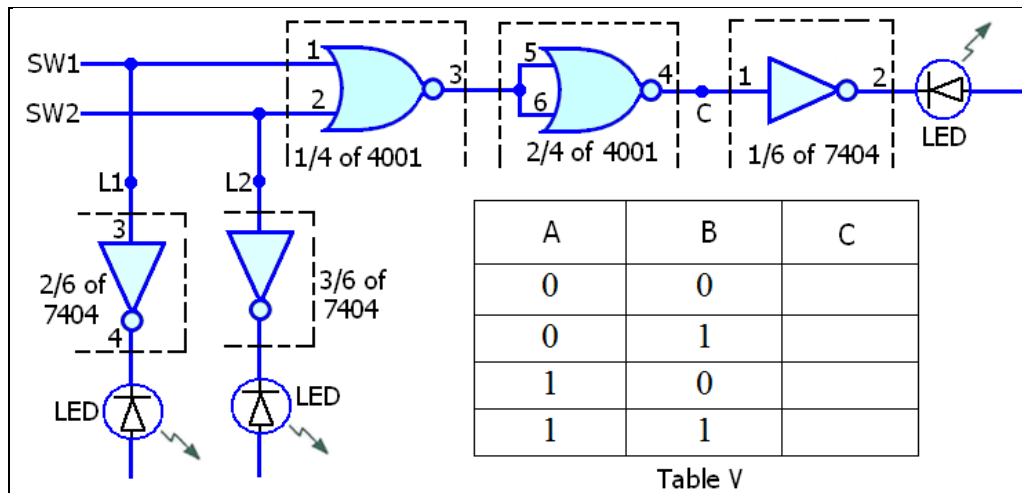
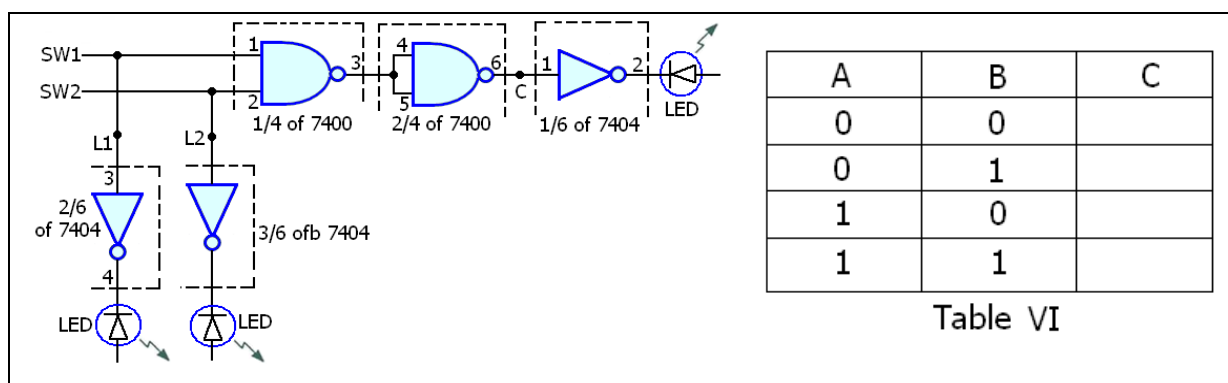Fig. 2-4

14. Study the circuit in Fig. 2-4 and the data in Table V. what logic function is being performed? ………………………………………….

15. Connect the circuit shown in Fig. 2-5. Monitor the inputs and output on LED indicators L1, L2, and L3. With SW1 (A) and SW2 (B), apply the inputs shown in Table VI. Record the output state (C) corresponding to each set of inputs. Use positive logic.

16.
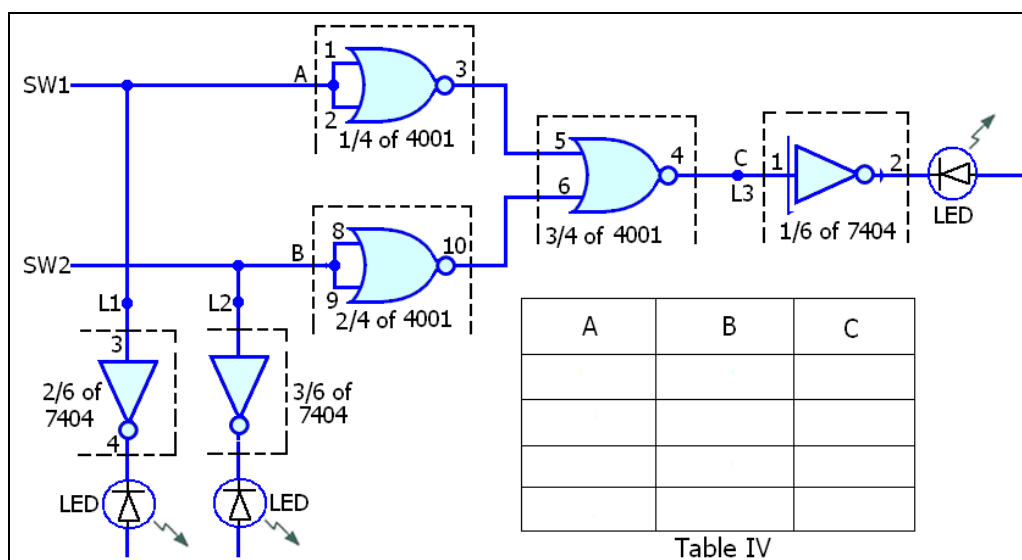
Fig. 2-5

17. Study Fig. 2-5 and Table VI. What logic functions is being performed?
    ……………

18. Modify your circuit in Fig. 2-5 by adding the fourth gate in the 4001 to the output, as shown in Fig. 2-6. Only the output change is shown.

A	B	C
0	0	
0	1	
1	0	
1	1	
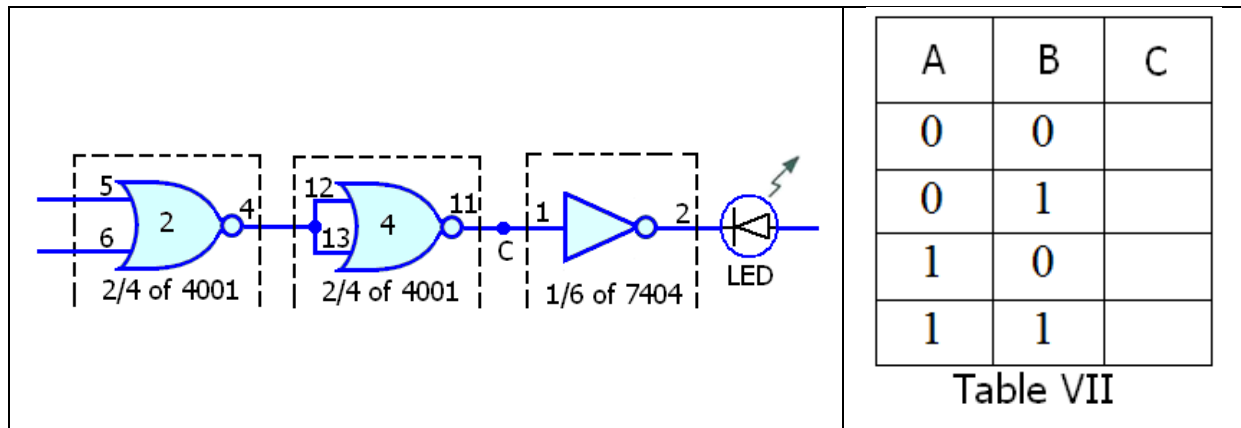
Table VII

Fig. 2-6

19. Using SW1 (A) and SW2 (B) data switches and monitoring LED indicators L1, L2, and L3, apply the states shown in Table VII. Record the output state (C) for each set of inputs.

20. Study Table VII. What logic function is being performed? ……….

LESSON 3.3

FLIP-FLOPS

LESSON 3.3

FLIP-FLOPS

OVERVIEW

This lesson examines the construction, functional description and truth tables of the three basic types of flip-flops-RS, D-Type and JK. The applications of flip-flops in different types of storage registers are introduced. The trainees learn how to apply flip-flops truth tables to analyze output waveforms for digital logic troubleshooting. The trainees would learn how to implement shift registers in hardware equipment, test their operations and have hands on experience to work with IC shift registers.

OBJECTIVES

Upon completion of this lesson, the trainee should be able to:

- Define Flip/Flop.
- Draw the schematic symbols of RS, D-Type and JK-flip/flops.
- Explain the operation of three types of flip/flops.
- Write the truth tables for the three types of flip-flops.
- Draw the output waveforms of RS, D-Type and JK-flip/flops from truth tables.
- Analyze the simple applications of the three types of flip/flops.
- Define a shift register.
- List different types of shift registers relative to their applications.
- Explain the operating principle of a shift register with simple examples.

Task 3.3-1: Set-Reset Flip/Flop

Task 3.3-2: JK Flip/Flop

INTRODUCTION

A flip-flop is a bi-stable digital logic circuit with two complementary outputs **(Q and $\overline{Q}$)** to serve as a basic memory cell capable of storing a single bit of binary data **(0 or 1)**. It can assume either of two stable states, representing binary **1** or **0**.

If the flip-flop is put into one of its two stable states, it will remain there as long as power is applied or until it is changed. A flip-flop remembers its previous output states, **Set** (Q=1, $\overline{Q}$=0) or **Reset** (Q=0, $\overline{Q}$=1). Retaining the previous state in a flip-flop is known as **latching** and hence the name **Latch**. By applying appropriate logic inputs to a flip-flop, we can set or reset the output Q. To determine the value of the bit stored in the flip-flop, we can measure the outputs, **Q** and $\overline{Q}$ with a logic probe, an Oscilloscope or a **DVM**. The three basic types of flip-flops are:

- Latch RS.
- JK-Flip/Flop.
- D-type Flip/Flop.

RS FLIP/FLOP USING NAND GATES

Fig. 3.3-1 shows the Set-Reset flip-flop, called the **RS** latch using NAND gates with schematic symbol in **(a)** and internal wiring in **(b)**. The **RS**-flip/flop, using **NAND** gates, has two **active low** inputs, Set **($\overline{S}$)** and Reset **($\overline{R}$)**, and two outputs **Q** and $\overline{Q}$.

The **active low** inputs mean that the inputs to the flip-flop are normally held high (1) with pull-up resistors or with the outputs of other gates and when activated go low (0) **only one at a time**. Some manufacturers list the Reset **($\overline{R}$)** input as Clear **($\overline{C}$)** in the data sheets. Applying the active low pulse to either the $\overline{S}$ or $\overline{R}$ input will put the latch into Set state **(Q=1)** or the Reset state **(Q=0)**, respectively, as shown in Table 3.3-1 for the truth table. The active low $\overline{S}$ input is used to set the flip-flop by a low going pulse. When **RS**-flip/flop is set, it is said to be storing a binary **1** at the Q-output with complementary output $\overline{Q}$ = 0.

The $\overline{R}$ input is used to reset the flip-flop by a low going pulse.

When **RS**-flip/flop is reset, it is said to be storing a binary **0** at the Q-output with complementary output $\overline{Q} = 1$. Once the output **(Q)** is set or reset, any repetitive signal to the respective input terminal does not affect the output.

Fig. 3.3-1 RS-Flip/Flop using SN7400 TTL Series NAND Gates

INPUTS		OUTPUTS		REMARKS
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	
0	0	1	1	NOT ALLOWED ‹INVALID
0	1	1	0	SET
1	0	0	1	RESET
1	1	N/C	N/C	NO CHANGE

Table 3.3-1 NAND Gate RS Flip-Flop Truth Table

As illustrated above, the two **NAND** gate outputs are cross-wired back to the **NAND** gate inputs so that the output of one feeds the input of the other.

Fig. 3.3-2 Schematic Diagrams of RS Flip-Flop using NAND Gates

As shown in Fig. 3.3-2, different digital logic designers draw the flip-flop logic diagrams depending on the choice only but are technically the same in operation and performance. If both $\overline{S}$ and $\overline{R}$ inputs are grounded (active low), both outputs Q and $\overline{Q}$ are forced high and this abnormal condition is undesired and invalid due to undefined outputs and should not be allowed.

When both $(\overline{S}$ & $\overline{R})$ inputs are binary **1s** (open/deactivated/High) as the normal condition for NAND gate latch, the outputs will retain the previous states and remain unchanged. When the $\overline{S}$ input (pin 1) is active **(0)**, the output from U1 NAND gate goes high **(Q =1)** and the RS latch is set. This output (pin 3) is fed back to the input (pin 5) of U2 NAND gate. The lower input $\overline{R}$ (pin 4) of U2 NAND gate is a binary **1** (open/High) so that output $\overline{Q}$ (pin 6) is low **(Q=0)**.

The output $\overline{Q}=0$ (pin 6) from U2 NAND gate is fed to the lower input (pin 2) of U1 gate as latching input to keep the Q-output high. Because of this feedback arrangement, the flip-flop is latched into SET state and will stay set until the reset input $\overline{R}$ (pin 4) of U2 NAND gate is active low (0). Another low pulse to the $\overline{S}$ input (pin 1) will have no effect on Q-output because the other input (pin 2) is low (0). Similarly, a low level to the $\overline{R}$ input (pin 4), while the latch is reset, will have no effect on Q-output because the other input (pin 5) is low (0). Fig. 3.3-3 describes the dynamic waveforms showing the effects of two inputs $\overline{R}$ & $\overline{S}$ on the outputs Q and $\overline{Q}$. Looking at the waveforms, we can determine the state of the flip-flop output prior to the application of negative going trigger pulse at time **(t_1)** where the latch is in the reset state storing a binary **0**. When the negative going trigger pulse **(t_1)** occurs on the $\overline{S}$-input, the latch sets the output **(Q = 1)** at the leading edge storing a binary 1.

The trigger Pulse at time (t_2) next on the $\overline{R}$-input resets the latch (Q = 0). The Pulse at time **(t_3)** on the $\overline{S}$-input again sets the flip-flop.

Note that pulse at time **(t_4)** that may be a random noise pulse also occurs on the $\overline{S}$-input consecutively that does not affect the complementary outputs and therefore, RS flip-flop acting as noise filter. Since the flip-flop is already set, the outputs remain unchanged (Q = 1 and $\overline{Q}$ = 0). The trigger Pulse at time **(t_5)** resets the latch output (Q = 0) at the low going leading edge storing binary **0**.

Fig. 3.3-3 NAND Gate RS Flip-Flop Waveforms

Note that pulse at time (t_6) that may be a **random noise** pulse also occurs on the $\overline{R}$-input consecutively that does not affect the complementary outputs and therefore, RS flip-flop acting as noise filter. Finally, a pulse at time (t_7) again on the $\overline{S}$ input sets the latch and little later $\overline{R}$-input goes low while $\overline{S}$-input is still active. With both $\overline{S}$ and $\overline{R}$-inputs low, simulating **abnormal** operation of the flip-flop, the **Q** and $\overline{Q}$ outputs are both high and are no longer complementary to each other, as indicated in Fig. 3.3-3. It may be in any unclear state, depending on which input occurs first, indicating neither set nor reset condition that is **undesired** and **invalid** for NAND gate RS flip-flop. The complete operation of a **NAND** gate latch is summarized by the Truth Table 3.3-1 above listing all possible input conditions and resulting output states.

RS FLIP-FLOP USING NOR GATES

Fig. 3.3-4 shows the Set/Reset flip-flop, called the RS-latch using NOR gates with schematic symbol in (a) and internal wiring in (b). The RS flip-flop, using NOR gates, has two active high inputs, Set (S) and Reset (R), and two outputs Q & $\overline{Q}$.

The active high inputs mean that the inputs to the flip-flop are normally held low (0) with pull-down resistors or with the outputs of other gates and when activated, go high (1) only one at a time. Applying the active high pulse to either the S or R input will put the latch into Set state (Q=1) or the Reset state (Q=0), respectively, as shown in Table 3.3-2 for the truth table. The active high S-input is used to set the flip-flop by a

high going pulse. When RS-flip/flop is set, it is said to be storing a binary 1 at the Q-output with complementary output $\overline{Q} = 0$. The R-input is used to reset the flip-flop by a high going pulse. When RS-flip/flop is reset, it is said to be storing a binary 0 at the Q-output with complementary output $\overline{Q} = 1$. Once the output (Q) is set or reset, any repetitive signal to the respective input terminal does not affect the output.
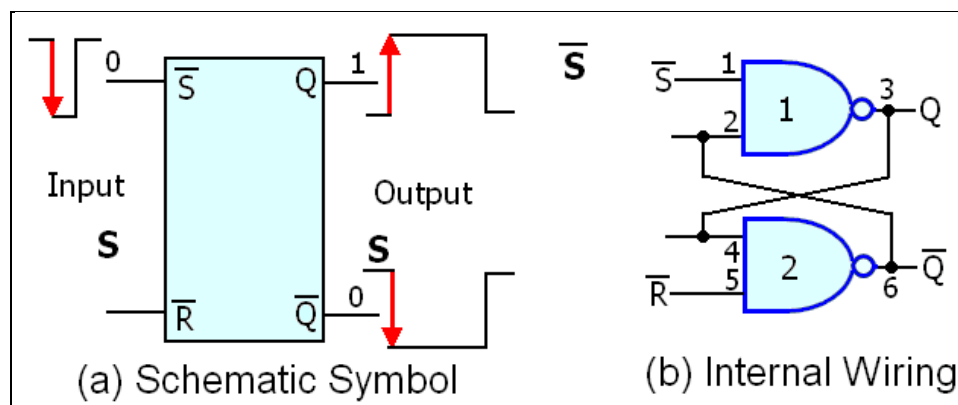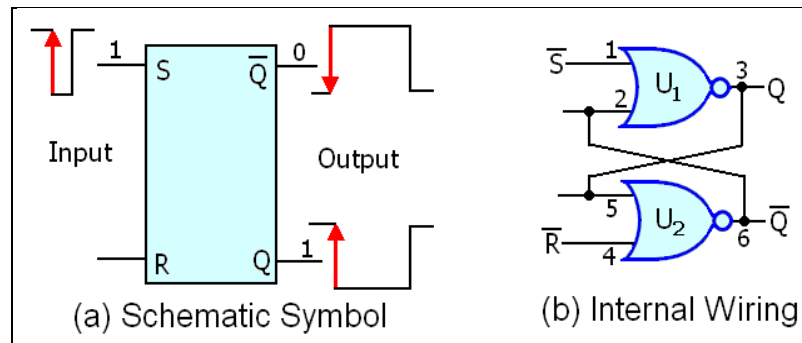

Fig. 3.3-4 RS-Flip/Flop using SN7402 TTL Series NOR Gates

INPUTS		OUTPUTS		REMARKS
S	R	Q	$\overline{Q}$	
0	0	N/C	N/C	NO CHANGE
0	1	0	1	RESET
1	0	1	0	SET
1	1	0	0	NOT ALLOWE

Table 3.3-2 NOR Gate RS-Flip/Flop Truth Table

As illustrated above, the two **NOR** gate outputs are cross-wired back to the **NOR** gate inputs so that the output of one feeds the input of the other.
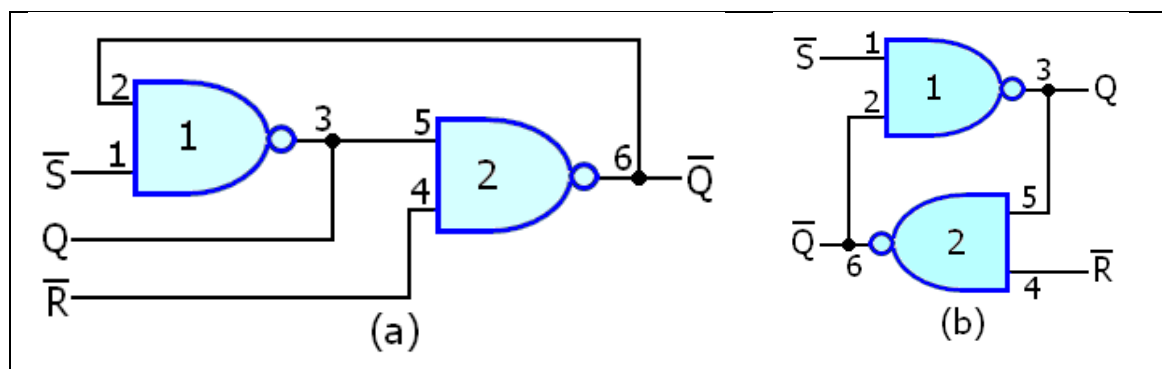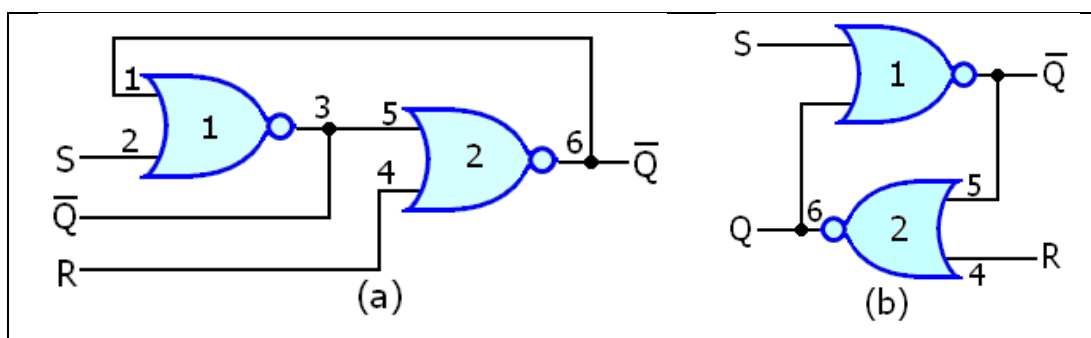

Fig. 3.3-5 Schematic Diagrams of RS Flip-Flop Configurations using NOR Gates

As shown in Fig. 3.3-5, different digital logic designers draw the flip-flop logic diagrams depending on the choice only but are technically the same in operation and performance. If both S and R inputs are active high, both outputs Q and $\overline{Q}$ are forced low and this abnormal condition is undesired and invalid due to undefined outputs and should not be allowed.

When both (**S & R)**-inputs are binary **0s** (open/deactivated/Low) as the normal condition for NOR gate latch, the outputs will retain the previous states and remain unchanged. When the **S**-input (pin 1) is active high **(1)**, the output at pin 3 from U1 NOR gate goes low **($\overline{Q}$=0)** that is fed back to the input (pin 5) of U2 NOR gate. The lower input **R** (pin 4) of U2 NOR gate is a binary **0** (grounded) so that output **Q** (pin 6) is high and the RS-latch is set **(Q=1)**. The output **Q=1** (pin 6) from U2 NOR gate is fed to the lower input (pin 2) of U1 gate as latching input to keep the $\overline{Q}$-output low.

Because of this feedback arrangement, the flip-flop is latched into **SET** state and will stay set until the reset input **R** (pin 4) of U2 NOR gate is active high **(1)**. Another high pulse to the **S** input (pin 1) will have no effect on Q-output because the other input (pin 2) is high **(1)**.

Similarly, a high level to the **R**-input (pin 4) while the latch is reset will have no effect on Q-output because the other input (pin 5) is high **(1)**. Fig. 3.3-6 depicts the dynamic waveforms showing the effects of two inputs (**R)** and (**S)** on the outputs (**Q** & $\overline{\mathbf{Q}}$).
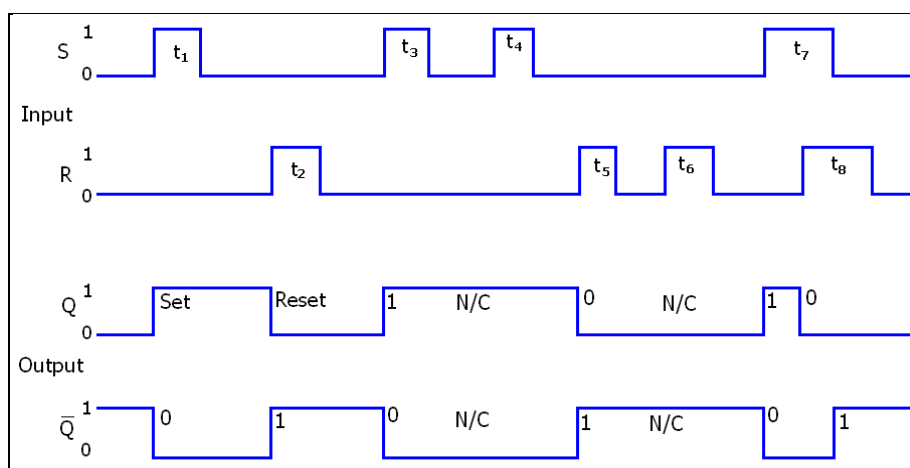
Fig. 3.3-6 NOR Gate RS-Flip/Flop Waveforms

Looking at the waveforms, we can determine the state of the flip-flop output prior to the application of positive going trigger pulse at time (t_1) where the latch is in the reset state storing a binary 0. When the positive going trigger pulse (t_1) occurs on the S input, the latch sets the output (Q=1) at the leading edge storing a binary 1. The trigger Pulse at time (t_2) next on the R input resets the latch (Q=0). The Pulse at time (t_3) on the S-input again sets the flip-flop. Note that pulse at time (t_4) that may be a random noise pulse also occurs on the S-input consecutively that does not affect the complementary outputs and therefore RS-flip/flop acting as noise filter. Since the flip-flop is already set, the outputs remain unchanged (Q=1 and $\overline{Q}$=0). The trigger Pulse at time (t_5) resets the latch output (Q=0) at the high going leading edge storing binary 0. Note that p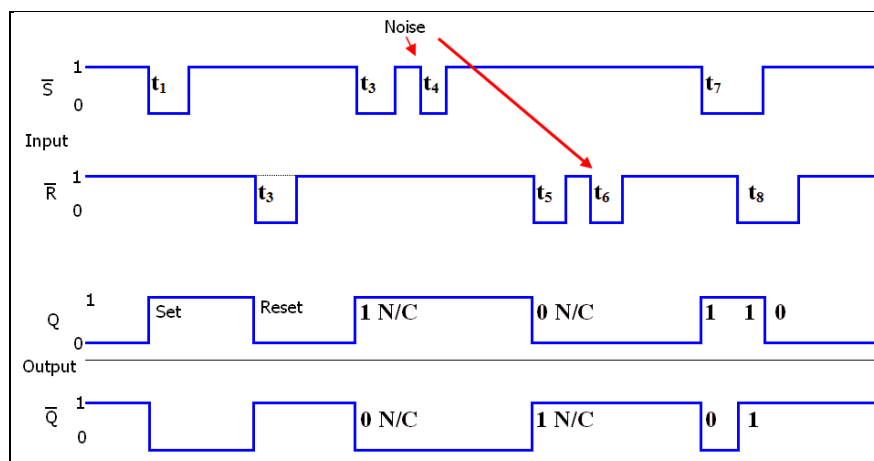ulse at time (t_6) that may be a random noise pulse also occurs on the R-input consecutively that does not affect the complementary outputs and therefore RS-flip/flop acting as noise filter.

Finally, a pulse at time t_7 again on the S input sets the latch and little later R input goes high while S input is still active. With both S and R inputs active (1), simulating abnormal operation of the flip-flop, the Q and $\overline{Q}$ outputs are both low (0) and are no longer complementary to each other, as indicated. It may be in any ambiguous state, depending in which input occurs first, indicating neither set nor reset condition that is undesired and invalid for NOR gate RS-flip/flop similar to NAND gate RS-flip/flop. The inputs on the S & R terminals of a NOR gate RS-flip/flop must not be active simultaneously. The complete operation of a NOR gate latch is summarized by the Truth Table 3.3-2 above listing all possible input conditions and resulting output states.

START/STOP APPLICATION OF NOR GATE LATCH

Fig. 3.3-7 shows the NOR gate RS-flip/flop circuitry for START/STOP static operation, totally eliminating bouncing effect. The capacitor is charging to V_{CC}, when the switch is closed for logic 1 and discharging through the resistor to ground when open for logic 0. The debouncing with RS-Flip/Flop requires two N/O SPST push button contact switches (S0-1) connected to V_{CC}.
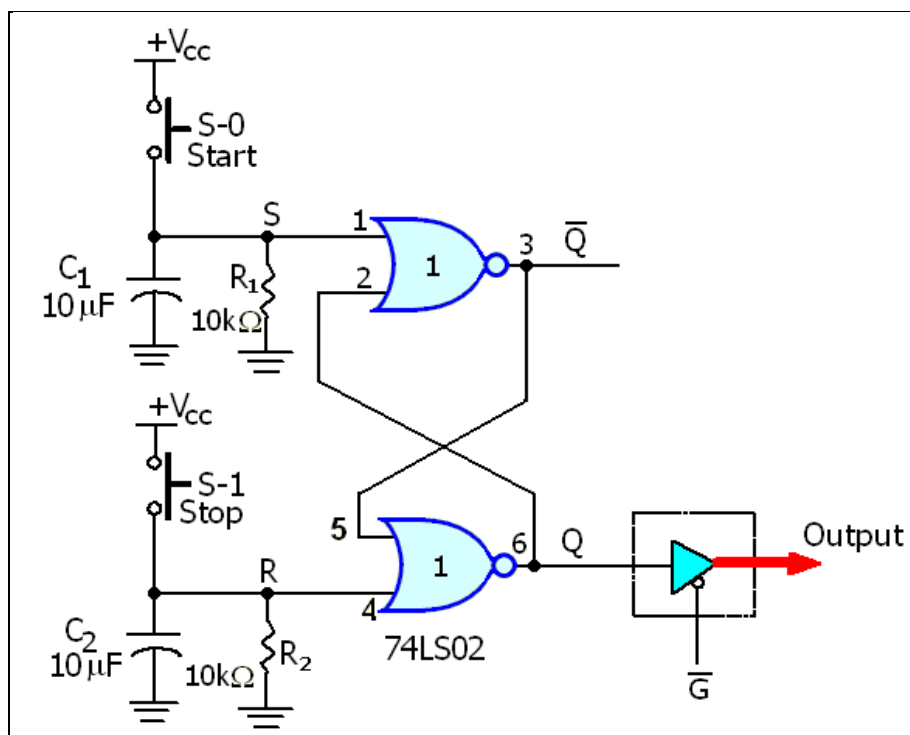
Fig. 3.3-7 RS NOR Gate Flip-Flop for START/STOP Application

The capacitors also protect the inputs from electrostatic in CMOS applications when the pushbutton switches are away from the circuitry on the control panel with long leads. When the START pushbutton is pressed, the input S goes high (pin 1) forcing the $\overline{Q}$-output (pin 3) to low (0) at U1 NOR gate. Q-output (pin 3) feeding back to the input (pin 5) of U2 NOR gate latches the Q-output (pin 6) to high (1) driving the output to the load through the buffer. When STOP pushbutton is pressed, the reverse occurs to turn the load off by putting logic 0 at the Q-output (pin 6).

RST-FLIP/FLOP

An **RST**-flip/flop is an extension of the basic **RS**-flip/flop with leading edge trigger and a real time clock **(T)** for synchronization. It forms the basis of understanding the operation of more advanced and reliable flip-flops, such as D-type and JK flip-flops used in critical timing and shift register applications.

RST-flip/flop may be constructed utilizing only NAND gates or NOR gates at the input of the basic RS-flip/flop, as follows.

RST FLIP-FLOP USING NAND GATES

Fig. 3.3-8 shows the RST-flip/flop using NAND gates for schematic symbol in (a) and internal wiring in (b). The RST-flip/flop, using NAND gates, has two active high inputs, Set (S) and Reset (R), and two outputs Q and $\overline{Q}$. The active high inputs mean that the inputs to the flip/flop are normally held low (0) with pull-down resistors or with the outputs of other gates and when activated go high (1) only one at a time.

Applying the active high pulse to either the S or R-input prior to the clock (T) will put the latch into Set state (Q=1) or the Reset state (Q=0), respectively, at the leading edge of the clock, as shown by the arrows upward.

Once the flip/flop output is set or reset, any repetitive clock signal to the respective input terminal does not affect the output. As shown the Table 3.3-3 for the truth table, when the S or R-input is high (1) and the clock goes high (1) at the leading edge, then and only then the Q-output is set or reset

(a) Schematic Symbol   (b) Internal Wiring
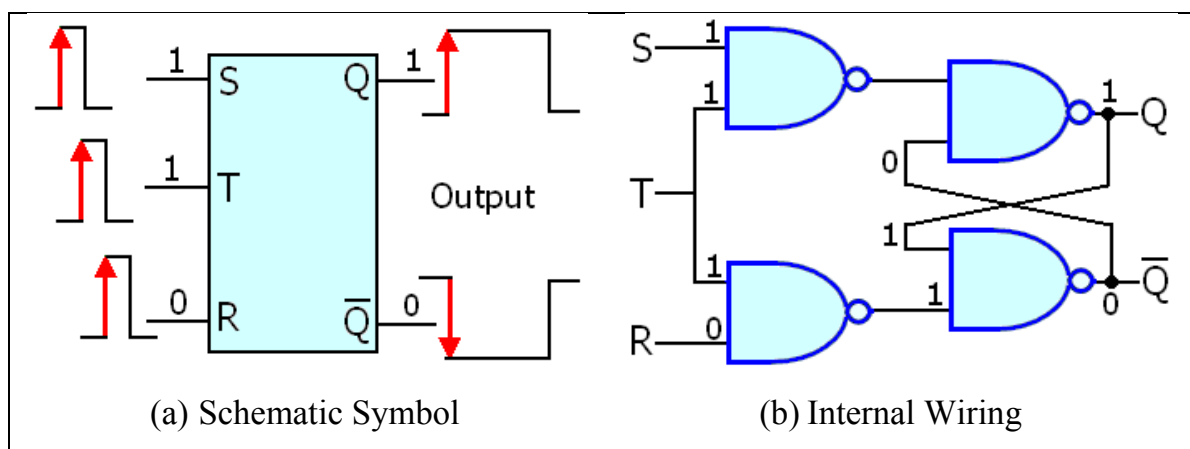
Fig. 3.3-8 RST-Flip/Flop using SN7400 TTL Series NAND Gates

When either or both inputs (S or R) are low and the clock is also low at logic 0, the Q-output remains unchanged as before as indicated in the truth table above. Inherent to RST flip-flop, when both inputs are high and the clock is also high, both Q and $\overline{Q}$ outputs are high that are invalid and undesired. The last condition with both inputs high must be avoided or the outputs may be undefined.

INPUTS					OUTPUTS		REMARKS
S	R	T	$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$	
0	0	0	1	1	N/C	N/C	NO CHANGE
0	0	0	1	1	N/C	N/C	NO CHANGE
0	1	0	1	0	N/C	N/C	NO CHANGE, READY TO BE RESET
0	1	1	1	0	0	1	**RESET**
1	0	0	0	1	0	1	NO CHANGE, READY TO BE SET
1	0	1	0	1	1	0	SET
1	1	0	0	0	1	0	NO CHANGE, NOT ALLOWED
1	1	1	0	0	1	1	NOT ALLOWED ‹INVALID

Table 3.3-3 NAND Gate RST Flip-Flop Truth Table

D-TYPE FLIP-FLOP

As shown in Fig. 3.3-9 for schematic symbol in (a) and internal wiring in (b), the D-type flip-flop has data input (D) and clock input (T) with complementary outputs Q and $\bar{Q}$.

(a) Schematic Symbol   (b) Internal Wiring
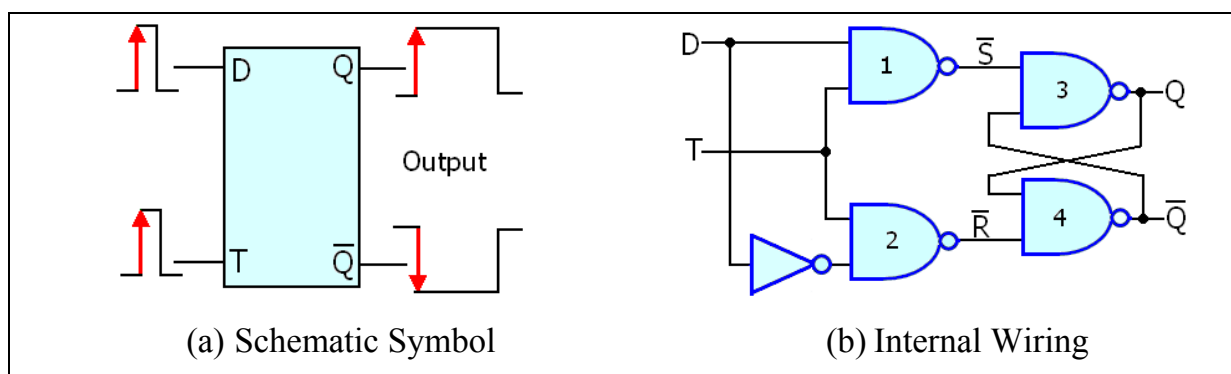
Fig. 3.3-9 D-Type Flip/Flop using NAND Gates

The **D** input is where you apply the data or bit to be stored. The **T**-input line controls the flip/flop. If the **T**-input line is high or binary **1**, the data on the **D**-line is stored in the flip/flop. As long as the **T**-line is high, the normal output will simply follow or track the **D**-input. If the **T**-line is low or binary **0**, the **D**-input line is not recognized.

Negated OR **(NAND)** gates 3 and 4 form a latch where the bit is stored. **NAND** Gates 1 and 2 are enabling gates that pass or inhibit the input. The inverter makes sure that the $\overline{\text{S}}$ and $\overline{\text{R}}$-inputs to the latch are always complementary. With a low input on the **T** line, the outputs of NAND gates 1 and 2 are high. This is the normal state for the inputs of a **NAND** latch to assume. In this state, the latch is undisturbed. Suppose a binary **1** is applied to the **D** input. Of course, nothing happens if the **T** input is still low. Now, make the **T** input go high to enable both gates 1 and 2. The binary **1** on the **D**-input makes gate 1 output go low. The inverter puts a low on the input to gate 2 so that its output stays high. The low output of gate 1 **($\overline{\text{S}}$)** sets the latch causing it to store the binary **1**. Returning the **T**-input low disables the input, but the binary **1** is retained. Now look at the waveforms in Fig. 3.3-10.
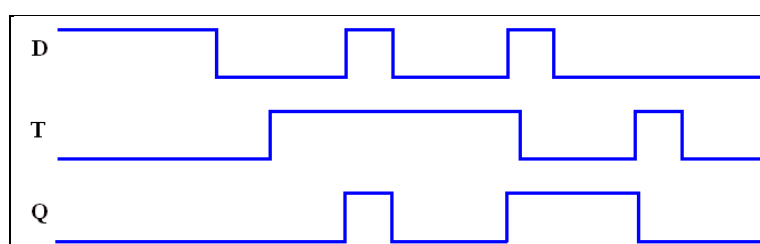
Fig. 4.3-10 D-Type Flip/Flop Waveforms

These represent the **D** and **T** inputs and the **Q** output of a D-flip/flop. The output is identical to the **D** input as long as the **T** input is high. When the **T** line goes low, the flip-f top stores the last state it sees on the **D** input. The operation of a D-type flip-flop is completely described by the Truth Table 3.3-4.

INPUTS		OUTPUTS		REMARKS
D	T	Q	$\overline{\text{Q}}$	
0	0	X	$\overline{\text{X}}$	NO CHANGE
0	1	0	1	RESET
1	0	X	$\overline{\text{X}}$	NO CHANGE
1	1	1	0	SET

Table 3.3-4 D-Type Flip-Flop Truth Table

JK FLIP-FLOP

The JK flip/flop is the most versatile type of binary storage element in common use. It can perform all of the functions of the **RS** and **D-type flip/flops** described earlier plus it can do several other things that the simple flip/flops cannot. Naturally, it is more complex and expensive than the other types. An integrated circuit JK-flip/flop, as shown in Fig. 3.3-11(a) for schematic symbol and Fig. 3.3-11(b) for internal circuitry, consists of two flip/flops in one, one feeding the other, with appropriate input on each. The arrangement is called a Master-Slave JK-flip/flop where each signal designated indicates an active high or low state. The slave flip-flop is the latch from which the outputs **(Q_2/ Q_2)** are taken.

The slave latch gets its complimentary active low inputs **($\overline{R2}$/ $\overline{S2}$)** from the master latch. The logic gates are the positive **NAND-type**. Gates 3 and 4 make up the master latch while gates 1 and 2 control its input. The slave latch is made up of gates 7 and 8. Gates 5 and 6 control the transfer of the master latch state to the slave latch.

(a) Schematic Symbol   (b) Internal Wiring
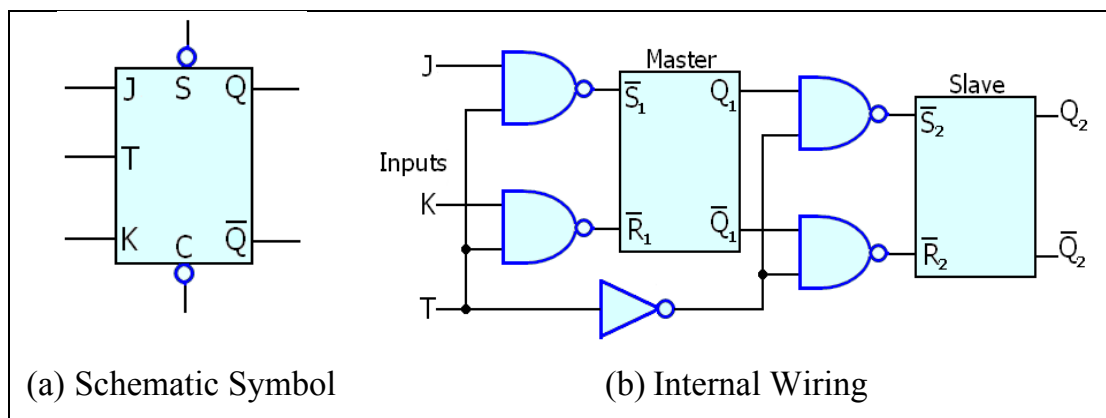
Fig. 3.3-11 Basic Master-Slave JK-Flip/Flop without Set and Clear Inputs

JK-FLIP/FLOP (SYNCHRONOUS OPERATION)

As shown in Fig. 3.3-12, the master flip/flop at the input circuit is an **RST** type where the logic signals to the JK-flip/flop are applied to set or reset its output. Depending on the states of JK inputs (active high), the clock **T** transfers **J** or **K** bit (whichever is high) to the master flip-flop output **(Q)** at the leading edge of the clock pulse **(↑)**.
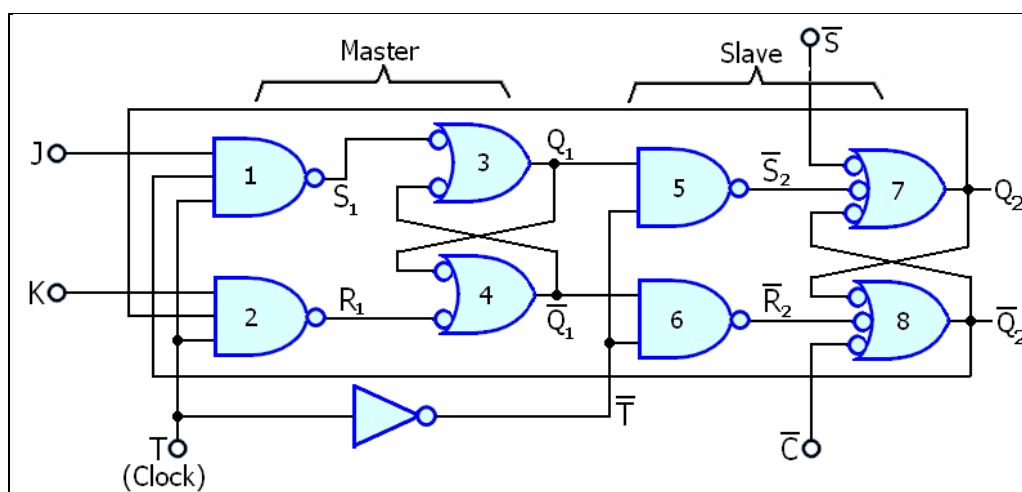
Fig. 3.3-12 Master-Slave JKFlip/Flop with Set and Clear Inputs

When the T-clock goes low, the master flip/flop is disabled at the input side and the inverted clock $\overline{T}$ transfers the master output data to the slave flip-flop output (Q) at the trailing edge of the clock pulse ($\downarrow$). Note that clock signal T controls the input gating of JK bits to the master flip-flop. The inverted clock signal $\overline{T}$ disables the slave input gates while transferring data to the master flip/flop. The active low Set ($\overline{S}$) and Clear ($\overline{C}$) inputs directly connected to the slave control NAND gates may be used to apply forced-Set or Clear to the slave JK-flip/flop irrespective to the master outputs operating the slave flip-flop as RS latch. To set the slave latch, the $\overline{S}$ input should be low and the $\overline{C}$ input high. This forces the normal Q2 output to high logic storing a binary 1. To reset the slave latch, the $\overline{C}$ input should be low and the $\overline{S}$ input high. This forces the normal Q2 output to low logic storing a binary 0. Normally, the $\overline{S}$ and $\overline{C}$ inputs will be high when deactivated. This arrangement is identical to that for the NAND latch inputs. Now let's consider how the JK and T (clock) inputs affect the flip/flop. Referring to Fig. 3.3-12 for detailed internal circuitry with feedback connections, consider the time when the clock input is low. Gates 1 and 2 will be inhibited so the J and K inputs cannot control the state of the master latch when the master latch output may be in either state. At this time, the slave latch will have the same state as the master latch when the clock input is low. The output of the inverter in the clock line $\overline{T}$ is binary 1, causing the gates 5 and 6 to be enabled during this time. Therefore, the state of the master latch is simply transferred to the slave latch.

Now if the clock T goes high, gates 1 and 2 will be enabled. The output of the inverter $\overline{T}$ will inhibit gates 5 and 6. The master latch cannot further change the slave latch. But now with gates 1 and 2 enabled, the J & K-inputs can affect the state of the master latch. The JK-flip/flop outputs Q_1 and $\overline{Q_1}$ are fed back to gates 1 and 2 additional inputs and they too determine the state of the master latch. If both J & K-inputs are low, the outputs of NAND gates 1 and 2 will be held high, so no change takes place in the master latch. If the J and K inputs are both high (or open), then the state of the master latch will be determined by the Q_2 and $\overline{Q_2}$-outputs of the slave latch feeding back to gates 1 & 2.

For example, if the slave latch is set, the master latch will be reset and vice versa. Remember also with the J, K and T inputs high, the state of the master latch will be determined by the Q2 and $\overline{Q2}$ outputs feeding back to the master input gates. The state of the JK flip-flop is the state of the slave latch. The state of the master latch determines the state of the slave latch at the trailing edge of the clock signal (T). The state of the master latch output is, in turn, determined by the J and K inputs. Finally, the clock input determines which of these latches is affected. With the clock input high, only the master latch is affected. The inverter on the clock line blocks gates 5 and 6 so the slave latch is not disturbed. The states of the JK inputs will ultimately determine the output state only at the leading edge of the clock (T).

When the clock line switches from high to low (trailing edge), the state of the master latch is transferred to the slave latch. If the JK-inputs are high or open, the flip-flop output will change state each time, the clock input switches from high to low for toggling operation (continuous pulse train). To reset the JK-flip/flop, apply a 0 to the J input and a 1 to the K input and then apply a clock pulse to reset on the trailing edge ↓ of the clock signal. To set the JK-flip/flop, you apply a 1 to J and 0 to K and again apply a clock pulse to set on the trailing edge ↓ of the clock signal. Assuming the J and K inputs are open or high for toggle mode of operation, the waveforms, as shown in Fig. 3.3-13, represent the normal flip-flop output. The 0 to 1 transition (leading edge) of the clock pulse (T) does not affect the output when the master flip-flop is in action. The flip-flop output changes, when the clock switches from logic 1 to 0 (trailing edge).
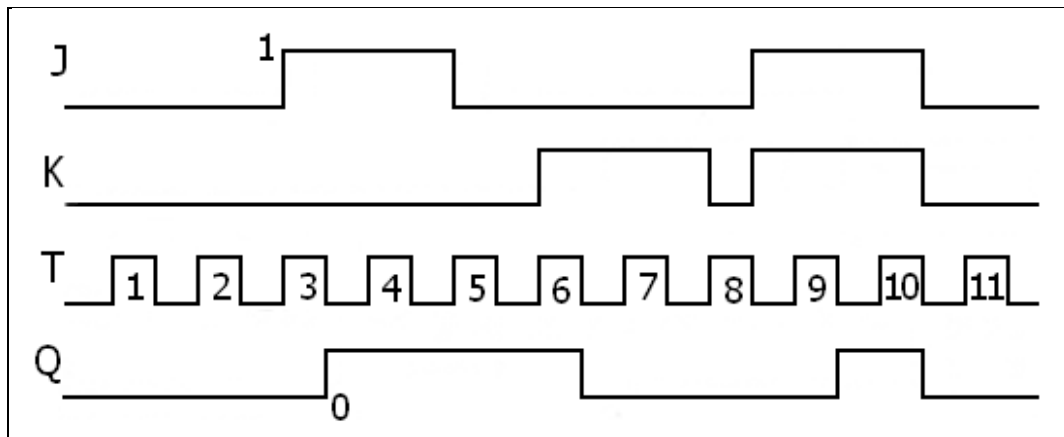
Fig. 3.3-13 Master-Slave JK Flip-Flop Random Input/ Output Waveforms

As shown in Fig. 3.3-14 for toggling mode (J=K=1), the Q output has a frequency one half the clock input.

Therefore, we call the **J** and **K** inputs synchronous because they cause state changes only on the occurrence of a specific clock transition (trailing edge) in synchronous with the clock.
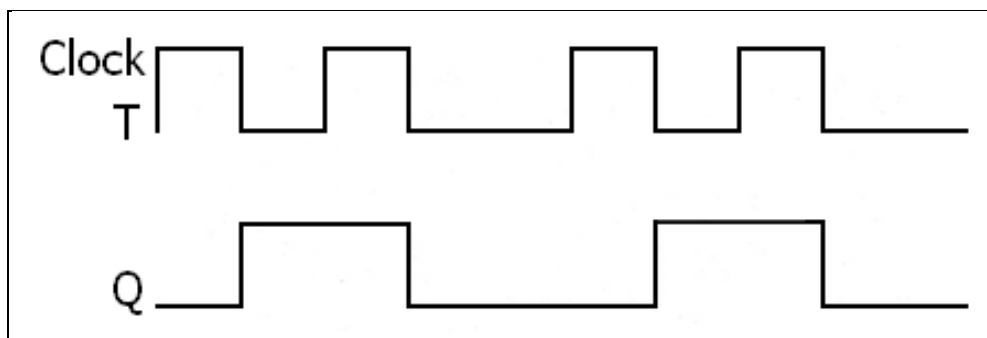
Fig. 3.3-14 Master-Slave JK Flip-Flop Input/ Output ÷2 Waveforms

It is on this transition that the content of the master latch is transferred to the slave latch. For some types of **JK**-flip/flops, toggling occurs on the leading or positive edge of the clock signal. The synchronous operation of the **JK**-flip/flop is summed up in the Truth Table 3.3-5 with all possible combinations of inputs. The Output State **X** represent either set (**1**) or reset (**0**). Referring to the Truth Table 3.3-5, when the **J** and **K**-inputs are both low, the clock does not affect the state of the flip/flop output. The flip/flop simply retains its previous condition that may be either set or reset state and is called the inhibit mode.

INPUTS			OUTPUTS (Master)		OUTPUTS (Slave)		REMARKS	
J	K	T	¹Q	¹$\overline{Q}$	²Q	²$\overline{Q}$	MASTER	SLAVE
0	0	0	X	$\overline{X}$	X	$\overline{X}$	NO CHANGE	NO CHANGE
0	0	0	X	$\overline{X}$	X	$\overline{X}$	NO CHANGE	NO CHANGE
0	1	0	X	$\overline{X}$	X	$\overline{X}$	NO CHANGE	NO CHANGE
0	1	1	0	1	X	$\overline{X}$	RESET	NO CHANGE
1	0	0	0	1	0	1	RESET	RESET
1	0	1	1	0	0	1	SET	RESET
1	1	0	1	0	1	0	SET	SET
1	1	1	0	1	1	0	(TOGGLE)RESET	SET
1	1	0	0	1	0	1	RESET	(TOGGLE)RESET

Table 3.3-5 JK-Flip/Flop Truth-table with JK-Inputs

JK FLIP-FLOP WITH SET AND CLEAR

The operation of a JK-flip/flop with $\overline{S}$ and $\overline{C}$ inputs is similar to RS-flip/flop, as shown in Truth Table 3.3-6, for asynchronous (independent) operation with all possible combinations of inputs.

INPUTS		OUTPUTS		REMARKS
$\overline{S}$	$\overline{C}$	Q	$\overline{Q}$	
0	0	1	1	UNDEFINED ،INVALID
0	1	1	0	SET
1	0	0	1	RESET
1	1	X	$\overline{X}$	NO CHANGE

Table 3.3-6 JK-Flip/Flop Truth Table with Set and Clear Inputs

The JK-flip/flop does have an undefined state unlike RS-flip/flop. If both $\overline{S}$ and $\overline{C}$ inputs are low, both **Q** and $\overline{Q}$ outputs will be high as **invalid** and **undefined** states. Therefore, care should be taken to see that this condition does not occur. The set **($\overline{S}$)** and clear **($\overline{C}$)** inputs are used to preset the flip/flop to some desirable condition prior to another operation. The most common operation is to reset the output stage and for that reason many **JK-**flip/flops have only a $\overline{C}$-input line.

SUMMARY

- A **Flip-Flop** is a bi-stable digital logic circuit with two complementary outputs (Q and $\overline{Q}$) to serve as a basic memory cell capable of storing a single bit of binary data (0 or 1).

- Retaining the previous state in a flip-flop is known as **latching** and hence the name **Latch**.

- If **both $\overline{S}$ & $\overline{R}$**-inputs to a NAND gate RS-flip/flop are grounded **(active low)**, both outputs Q and $\overline{Q}$ are forced **high** and this **abnormal** condition is undesired and **invalid** due to undefined outputs and should not be allowed.

- A **random noise** pulse occurring on the $\overline{S}$ or $\overline{R}$ inputs after the trigger pulse consecutively does not affect the complementary outputs and therefore RS-flip/flop acts as noise filter.

- When the button is depressed or released, the switch contacts do not make an immediate solid electrical or mechanical connection, but open and close for a brief period until stabilized this is known as **Contact Bounce**.

- RC network partially eliminates contact bounce whereas an RS flip-flop totally eliminates bouncing effect.

- If both S & R-inputs to a NOR gate RS flip-flop are **active high**, both outputs Q and $\overline{Q}$ are forced **low** and this **abnormal** condition is undesired and **invalid** due to undefined outputs and should not be allowed.

- An **RST** flip-flop, using NAND gates, has two **active high** inputs, Set **(S)** and Reset **(R)**, and two outputs **Q** and $\overline{\textbf{Q}}$.

- An **RST** flip-flop, using NOR gates, has two **active low** inputs, Set **($\overline{\textbf{S}}$)** and Reset **($\overline{\textbf{R}}$)**, and two outputs **Q** and $\overline{\textbf{Q}}$.

- The D-type flip/flop has two inputs data **(D)** and clock **(T)** with complementary outputs Q and $\overline{Q}$.

- D-type and JK-flip/flops do not have any ambiguous states.

- All Master-Slave D-type and JK-flip/flops trigger on the trailing edge of the clock pulse.

GLOSSARY

FLIP-FLOP: Bi-stable Latch with two states

RS FLIP-FLOP: Set-Reset Flip-Flop.

S: Set input to a flip-flop.

R: Reset input to a flip-flop.

TTL: Transistor-Transistor Logic.

CMOS: Complementary Metal Oxide Semiconductor Logic.

N/O: Normally open switch contact.

SPDT: Single-Pole-Double Throw pushbutton switch contact.

Strobe Line: Control line.

LSB: Least Significant Bit.

MSB: Most Significant Bit.

REVIEW EXERCISE

CHOOSE THE CORRECT ANSWER FOR EACH OF THE FOLLOWING:

1. The three basic types of flip/flops are:

    a) ------------------
    b) ------------------

    c) ------------------
    d) ------------------

2. The normal output level of a latch is _____ if it is set.

    a) High
    b) Low

    c) state-Tri
    d) state-Bi

3. The complement output of a latch is low. The bit value stored is _____.

    a) ٠Binary
    b) ١Binary

    c) ٠٠Binary
    d) ١١Binary

4. Both inputs of a NAND latch are low. The state of the latch is _____.

    a) Reset
    b) Ambiguous

    c) Unstable
    d) (c)and (b)Both

5. Both inputs to a NOR latch are high. The R input goes low and then the S input goes low. ._____ The bit value stored in the latch is

    a) ٠Binary
    b) ١ Binary

    c) ٠٠Binary
    d) ١١Binary

6. The T input of a D-type flip/flop determines its state.

    a) True
    b) False

7. On a Master-Slave negative-edge trigger JK-flip/flop, the S and C inputs are deactivated, J input is high, and K input is low. The state of the flip/flop when low clock pulse occurs on the T input is _____.

    a) Reset
    b) Set

    c) Illegal
    d) No change

8. Both J & K-inputs are held low. The S and C inputs are high. The Q output is 0. The state of the flip/flop output after three clock pulses is _____

    a. ·Binary   b. 'Binary

    c. Illegal   d. change No

9. When a JK-flip/flop operates as a RS NAND latch, the inputs used are _____.

    a) 1   b) J and K

    c) T   d) none of above

COMPLETE THE FOLLOWING:

10. D-type or JK-flip/flops are widely used to construct _____.

11. Complete the truth table for NAND gate D-type flip/flops.

INPUTS		OUTPUTS		REMARKS
D	**T**	**Q**	**$\bar{Q}$**	
0	0			
0	1			
1	0			
1	1			

Table 3.3-4 D-Type Flip/Flop Truth Table

TASK 3.3-1

JK Flip-Flops

OBJECTIVE

Upon completion of this task, the trainees will be able to:

- Demonstrate the operation and characteristics of a **JK**-flip/flop.

TOOLS, MATERIALS, & REQUIREMENTS

- 1 - ET-3200 Heathkit Digital Design Trainer
- 1 - 74LS76 JK Flip-Flop IC (443-829)
- Personal safety equipment as recommended in digital electronic workshop.

PROCEDURE

1. Connect the circuit shown in Fig. 1-1 using data switches for the J, K, S, and C inputs, logic switch A for the clock T input.

   Connect LED indicators to each output.

   The pin connections for 74LS76 dual JK-flip/flop are shown in Fig. 1-2.

   There are two identical JK-flip/flops in the 74LS76 IC, but we will use only one.

   Connect +5 volts to pin 5 and GND to pin 13.
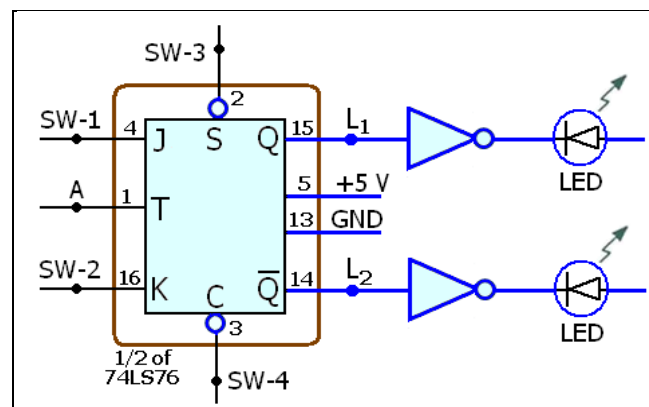
Fig. 1-1 Schematic Diagram of JK-Flip/Flop
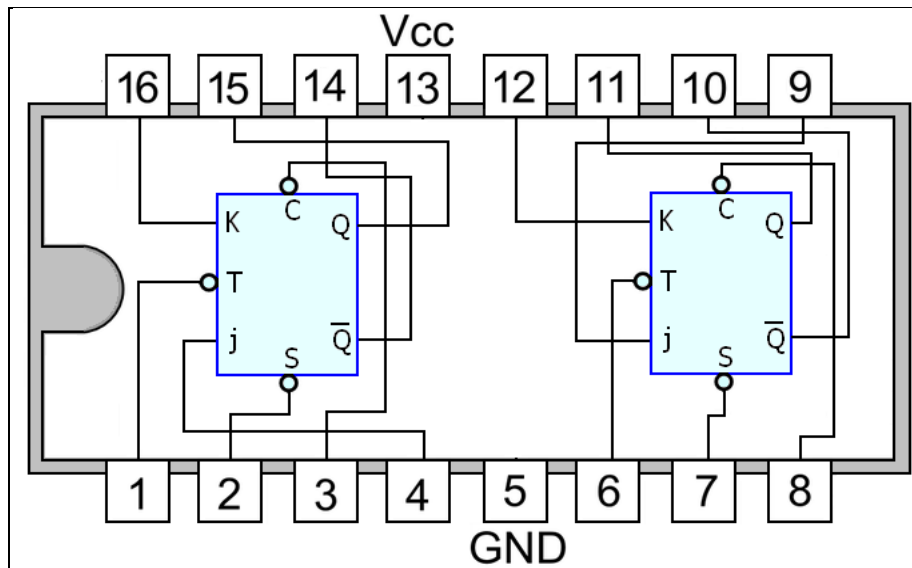
Fig. 1-2 Pin Connections for Dual TTL JK-Flip/Flop (74LS76)

2. Check the asynchronous operation of the JK-flip/flop. Set J = K = 1 with SW-1 and SW-2.

   Apply the levels indicated in **Table 1-1** to the **S** and **C** inputs.

   Note the output states and record them in **Table 1-1**.

   Repeat this step with **J= K = 0** and note the results.

INPUTS		OUTPUTS		REMARKS
$\overline{S}$	$\overline{C}$	Q	$\overline{Q}$	
0	0			
0	1			
1	0			
1	1			

Table 1-1 JK-Flip/Flop Truth Table with Set and Clear Inputs

Do the JK inputs affect the asynchronous operation? _____

3. Verify the synchronous operation of the JK-flip/flop Setting the S and C inputs to Binary 1.

   Apply the logic levels indicated in Table 1-2.

Note the normal output states (Q) and ($\overline{Q}$) before and after the application of a single clock pulse (T) from the A-logic switch.

After you have completed Table 1-2, repeat the inputs given and toggle the clock (T) input several times with the A-logic switch for each set of inputs.

Note the results on the LED logic indicators.

INPUTS			OUTPUTS (Master)		OUTPUTS (Slave)		REMARKS	
J	K	T	Q1	$\overline{Q1}$	Q2	$\overline{Q2}$	MASTER	SLAVE
0	0	0						
0	0	1						
0	1	0						
0	1	1						
1	0	0						
1	0	1						
1	1	0						
1	1	1						
1	1	0						

Table 1-2 JK-Flip/Flop Truth Table with JK Inputs (Synchronous Operation)

4. Set the J & K-inputs to Binary 1 with the logic switches.

   Remove the **A**-logic switch from the **T**-input and connect a 1Hz clock (CLK) signal to it.

   Also connect a LED logic indicator to the CLK signal.

   Observe the CLK input and Q and $\overline{Q}$ outputs on the LED indicators.

   Note the relationship between input and output frequencies.

5. Construct the circuit shown in Fig. 1-3. The circuit will be driven from the 1 Hz CLK signal. The A & B-logic switches will control the circuit. You will observe the output states on LED indicators L_1, L_3 and L_4.
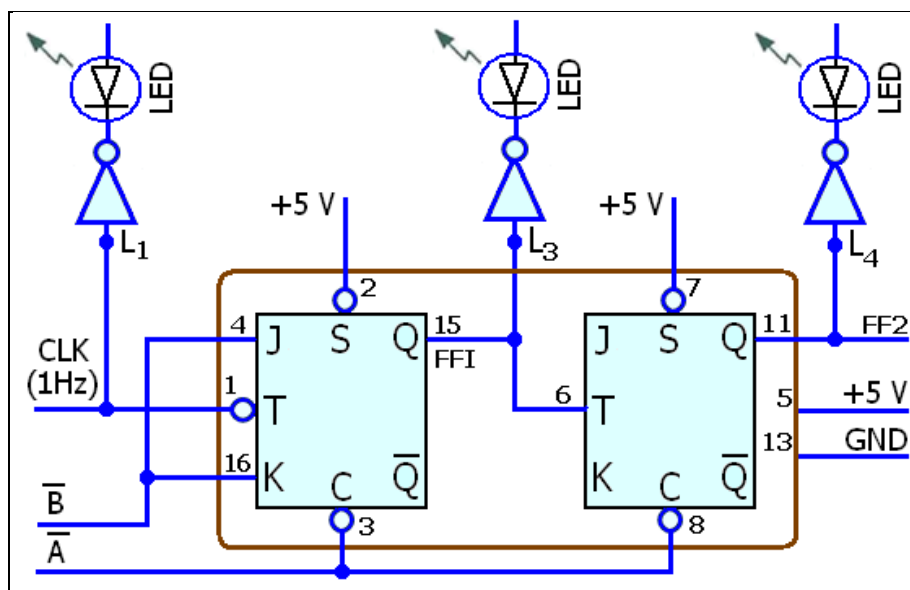
Fig. 1-3 Cascaded JK-Flip/Flops

6. Observe the relationship between the input **(L1)** and outputs **(L3-L4)** waveforms.

   You can do this by counting the number of input and output pulses.

   Sketch a timing diagrams illustrating this relationship in Fig. 1-4(a).

Fig. 1-3(a) Cascaded JK-Flip/Flop Output Waveforms

7. While the circuit is operating, depress the **B** logic switch. Note the effect on the circuit? (Note the output states). Release the B switch and repeat this step several times. Depress the A-logic switch while the circuit is operating.

   Note the effect on the outputs and repeat several times.
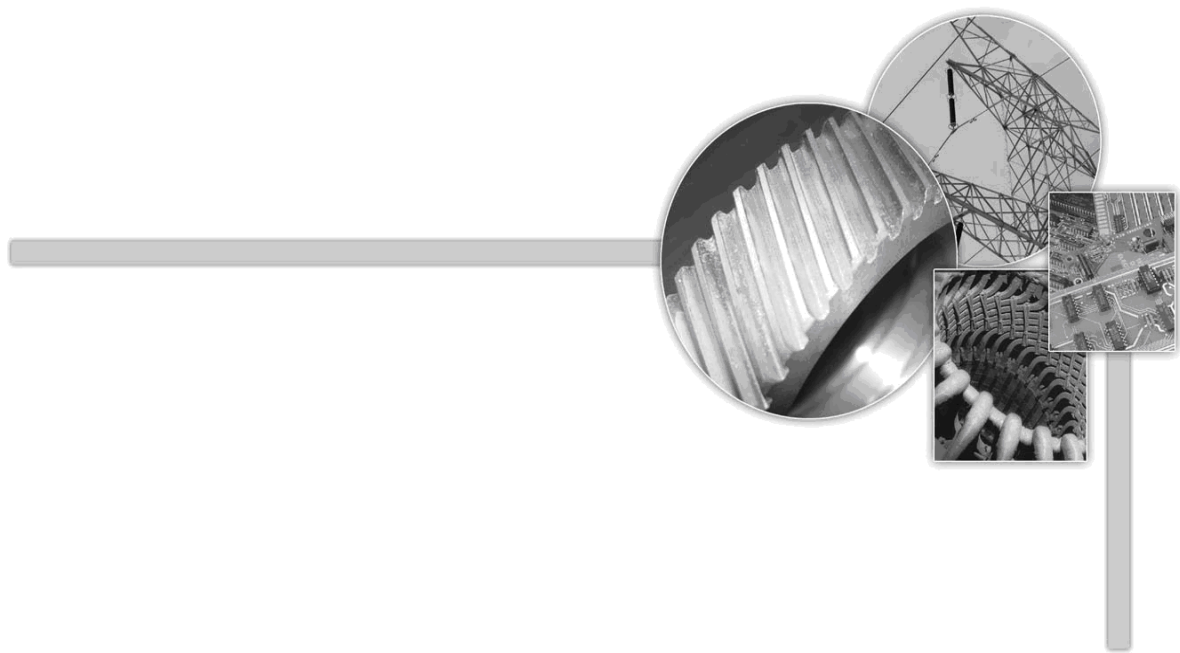
LESSON 3.4

COUNTERS & SHIFT REGISTERS

LESSON 3.4

COUNTERS & SHIFT REGISTERS

OVERVIEW

This lesson discusses the operation of Binary and BCD counters and the effects of cascaded Binary Counters on the output signal. The trainees will learn how to build and test simple Binary and/or BCD counters using flip-flops and/or IC counters and troubleshoot sequential circuits.

In this part of lesson we discuss the application of flip/flops in the construction of different types of shift registers depending on the application. The trainees would learn how to implement shift registers in hardware operations and test their operations and have hands-on experience to work with IC shift registers.

In this section we explain the operation of different clock circuits and their importance in digital circuits and systems.

OBJECTIVES

Upon completion of this lesson the trainees will be able to:

- Explain the operation of Binary and BCD Counters.
- Determine the maximum counting capability of a binary counter.
- Determine the count sequence of a counter.
- List the two types of Binary counters related to speed and reliability.
- List some applications of Binary Counters using simplified block diagrams and waveforms such as in a frequency counter.
- Analyze the operation of IC Counters in different modes of operation.
- Construct a Binary or BCD counter using only flip/flops and drawing necessary waveforms to demonstrate arithmetic frequency division.
- List different types of shift registers relative to their applications.
- Explain the operation of a shift register.

- Describe the main features of IC shift registers.

- List four applications for shift registers.

Task 3.4-1: Binary Counters

Task 3.4-2: Shift Registers

INTRODUCTION

The main circuit elements of **sequential logic** circuits, such as counters and shift registers, are flip/flops. These flip/flops store binary data and their states are changed by the logic input signal in accordance with the current information stored in them.

The sequential logic operations are generally sequenced by a periodic logic signal known as **Clock**. A digital clock is an oscillator that generates rectangular pulses at a fixed frequency. The most commonly used sequential circuits are available as a single ready to use Medium Scale Integration **(MSI)** logic **IC** package.

COUNTERS

A binary counter is a sequential logic circuit made up of flip/flops that is used to count the number of binary pulses applied to it. The pulses or logic level transitions to be counted are applied to the counter input. These pulses cause the flip-flops in the counter to change states. This is done in such a way that the binary number stored in the flip/flops represents the number of input pulses that have occurred.

By observing the flip/flop outputs we can determine how many pulses were applied to the input. If we let the counter count the input pulses for one second, the binary number stored in the flip/flops represents the frequency of the input signal as **pulses/sec** or **Hz**. There are several different types of counters used in digital circuits.

The most commonly used is the binary counter. This type of counter counts in the standard Binary Code. **BCD** counters that count in the standard 8421 Binary Coded Decimal **(BCD)** code are also widely used to output the data to printers and display boards. Special counters can be developed to count in any of the special binary or BCD codes in common use. Counters are available and can be programmed to count up or down.

BINARY RIPPLE ASYNCHRONOUS COUNTERS

The term ripple is derived from the fact that the flip/flops in the counter are cascaded, with the output of one driving the input of the next and so on. As the count pulses are applied to the first input flip/flop, the count ripples through the flip/flops. The term asynchronous comes as a result of the flip/flops not being controlled by a single common clock pulse. A Binary Counter is a sequential logic circuit that uses the standard pure binary code. Such a counter is made up by cascading JK-flip/flops, as shown in Fig. 3.4-1. The normal output of one flip/flop **(A-D)** is connected to the clock input **(T)** of the next flip-flop. The JK-inputs on each flip/flop are open or high (recommended to be tied to V_{CC}). The input pulses to be counted are applied to the clock input **(T)** of the A flip/flop.
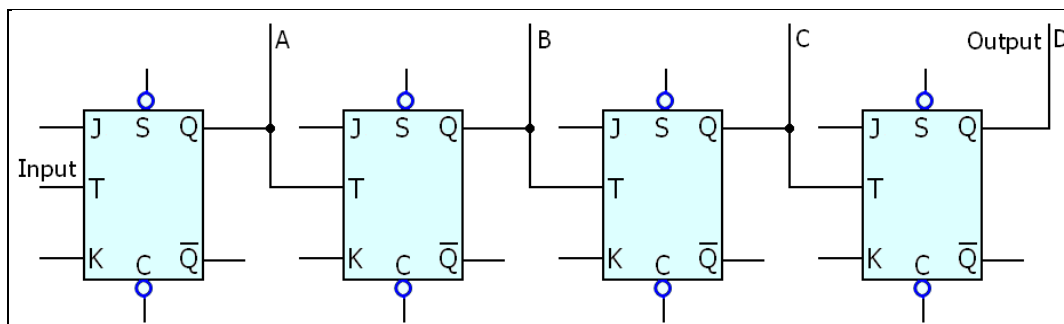
Fig. 3.4-1 Four Bit Binary Counter

The JK-flip/flop toggles or changes output state each time a trailing edge transition occurs on its T-input. The flip/flops will change state when the normal output of the previous flip/flop switches from binary 1 to binary 0. If we assume that the counter is initially reset, the normal outputs of all the flip/flops will be binary 0. When the first input pulse occurs, the A flip/flop will be set.

The binary number stored in the flip/flops indicates the number of input pulses that have occurred. To read the number stored in the counter, we simply observe the normal outputs of the flip/flops. The A flip/flop is the Least Significant Bit **(LSB)** of the word. Therefore, the four bit number stored in the counter is designated **DCBA.**

After the first input pulse, the counter state is **0001**, indicating that one input pulse has occurred. When the second input pulse occurs, the A flip/flop toggles and gets reset.

As it resets, its normal output switches from binary 1 to binary 0, causing the B flip-flop to set. Observing the new output state **0010**, we note that two input pulses have occurred. When the third input pulse occurs, the A flip/flop will again set from binary 0-1. This transition is ignored by the T-input of the B flip/flop and the number stored in the counter is **0011** or a decimal 3, indicating that three input pulses have occurred. When the fourth input pulse occurs, the A-flip/flop is reset.

Its normal output switches from binary 1 to binary 0, thereby toggling the B-flip/flop. This causes the B-flip/flop to reset. As it does, its normal output switches from binary 1 to binary 0, causing the C-flip/flop to set. The number now in the counter is **0100** or a decimal 4 and this process continues as the input pulses occur. The count sequence is the standard 4 bit binary code, as indicated in **Table 3.4-1**.

	D	C	B	A	DECIMAL
	0	0	0	0	0
	0	0	0	1	1
	0	0	1	0	2
R	0	0	1	1	3
E	0	1	0	0	4
C	0	1	0	1	5
Y	0	1	1	0	6
C	0	1	1	1	7
L	1	0	0	0	8
E	1	0	0	1	9
	1	0	1	0	10
	1	0	1	1	11
	1	1	0	0	12
	1	1	0	1	13
	1	1	1	0	14
	1	1	1	1	15

Table 3.4-1 Count Sequence of Four Bit Counter

An important point to consider is the action of the circuit when the number stored in the counter reaches **1111 (15)** in the last count. This is the maximum count that the four bit binary counter circuit can have. When the next input pulse is applied, all flip-

flops will change states from 1s to 0s, Clock pulse **(T)** resetting the A-flip/flop, the A-flip/flop resetting the B flip-flop, the B flip-flop resetting the C-flip/flop and finally the C-flip/flop resetting the D-flip/flop. As the resulting contents of the counter change to **0000,** as shown in Table 3.4-1, the counting cycle repeats again. The complete operation of the four bit binary counter is illustrated by the input and output waveforms in Fig. 3.4-2. The clock input in binary format is a series of pulses equally spaced to be counted. The normal outputs from the flip/flops are divide-by-2 waveforms as 1248 outputs A, B, C and D, respectively.
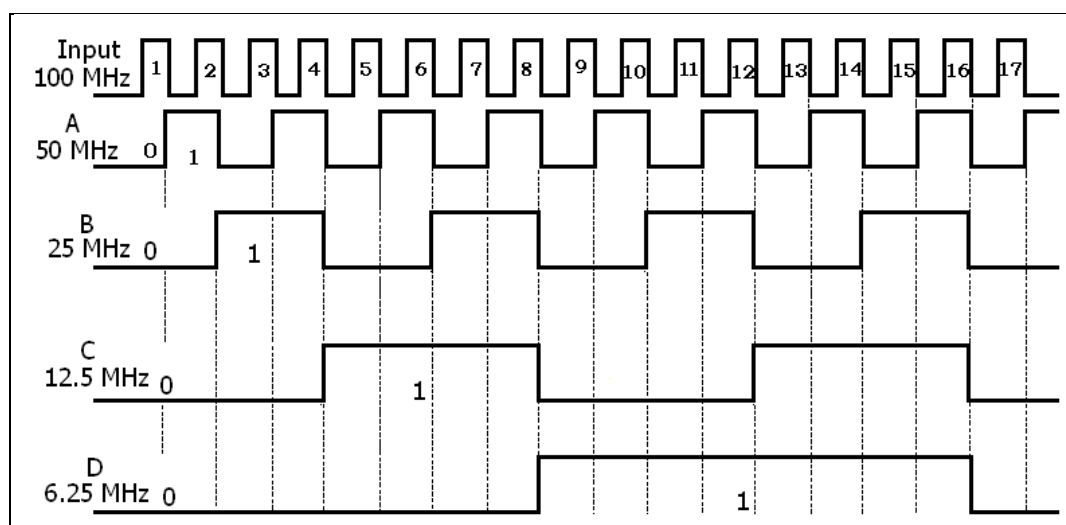
Fig. 3.4-2 Input and Output Waveforms of a Four bit Binary Counter

As shown in Fig. 3.4-2, first, all the flip-flops toggle (change state) on the trailing edge or the binary 1 to binary 0 transition of the previous flip-flop.

We can easily trace the output of the first A-flip/flop, by simply observing when the trailing edge of the input occurs. The output of the B-flip/flop is a function of its input as the output of the A-flip/flop. Note that its state change occurs on the trailing edge of the A-output. The same is true of the C & D-flip/flops.

The binary code after each input pulse is indicated on the waveforms corresponding to the binary count sequence in Table 3.4-1.

FREQUENCY DIVIDER APPLICATION

Another important fact that is clear from the waveforms in Fig. 3.4-2 is that the binary counter is also a frequency divider. The output of each flip/flop is one-half the frequency of its input. If the input is a 100kHz square wave, the outputs of the flip-flops are:

f_A = 50 kHz   ÷2 (1 Flip/Flop)

f_B = 25 kHz   ÷4 (2 Flip/Flops cascaded)

f_C = 12.5 kHz   ÷8 (3 Flip/Flops cascaded)

f_D = 6.25 kHz   ÷16 (4 Flip/Flops cascaded)

The output of a pure binary counter is always some sub-multiple of two.

The four bit counter divides the input by 16:

f_D = 100 kHz/16= 6.25 kHz

MAXIMUM COUNT

The maximum count capability of a binary counter is a function of the number of flip/flops in the counter. The maximum number that can be stored in a binary counter, before it recycles, is determined in the same way as we determine the maximum binary number that can be represented by a word with a specific number of bits.

The formula below expresses the relationship between the number of flip/flops in a counter and its maximum count capability:

$N = 2^n - 1$

Where N = The maximum count that occurs prior to the counter recycling.

n = The number of flip/flops.

Ex. 3.4-1

Determine the maximum number (N) that can be contained in a counter using four binary flip/flops.

SOLUTION

$N = 2^4 - 1 = 16 - 1 = 15_{10} = 1111_2$

UP COUNTERS

The binary counter, as shown in Fig. 3.4-2, above is a binary up-counter where Q-outputs (A-D) of the low order flip/flops drive the T-input of the next stage flip-flop. All the flip/flops are reset to 0s before starting to count. Each time an input pulse occurs, the binary number increases, incrementing the counter by one.

DOWN COUNTERS

It is also possible to produce a down counter, where the input pulse decreases the binary number, decrementing the counter by one. As shown in Fig. 3.4-3, an up-counter has complementary $\overline{Q}$-outputs **($\overline{A}$ - $\overline{D}$)** of the low order flip-flops driving the T-input of the next stage flip/flop in sequence and the flip-flops are reset to 1s before starting to count from maximum number set at Q-outputs. The binary number in the counter decrements by one on each input pulse.
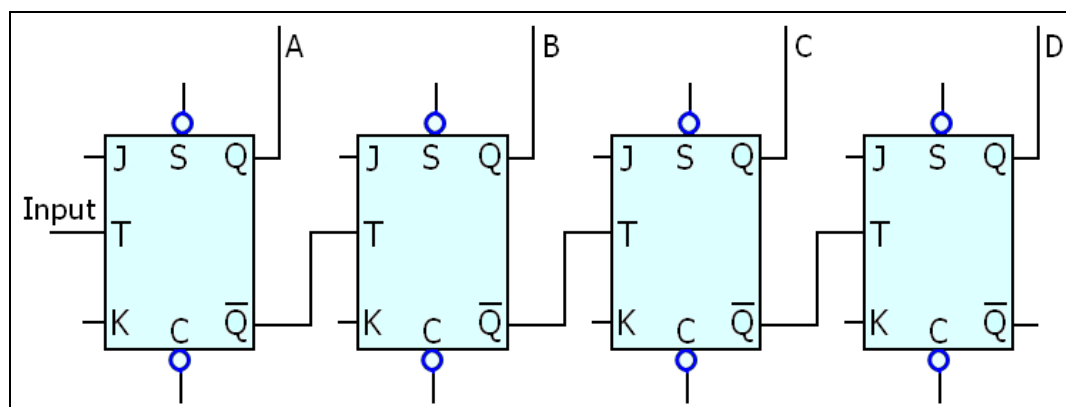
Fig. 3.4-3 Four bit Binary Down Counter

The down count sequence is illustrated in Table 3.4-2 and the corresponding waveforms associated with this counter are shown in Fig. 3.4-4, keeping the same divide by 2 frequency output relationship as the up-counter.

D	C	B	A	DECIMAL
1	1	1	1	15
1	1	1	0	14
1	1	0	1	13
1	1	0	0	12
1	0	1	1	11
1	0	1	0	10
1	0	0	1	9
1	0	0	0	8
0	1	1	1	7
0	1	1	0	6
0	1	0	1	5
0	1	0	0	4
0	0	1	1	3
0	0	1	0	2
0	0	0	1	1
0	0	0	0	0

RECYCL

Table 3.4-2 Count Sequence for Four bit Down Counter
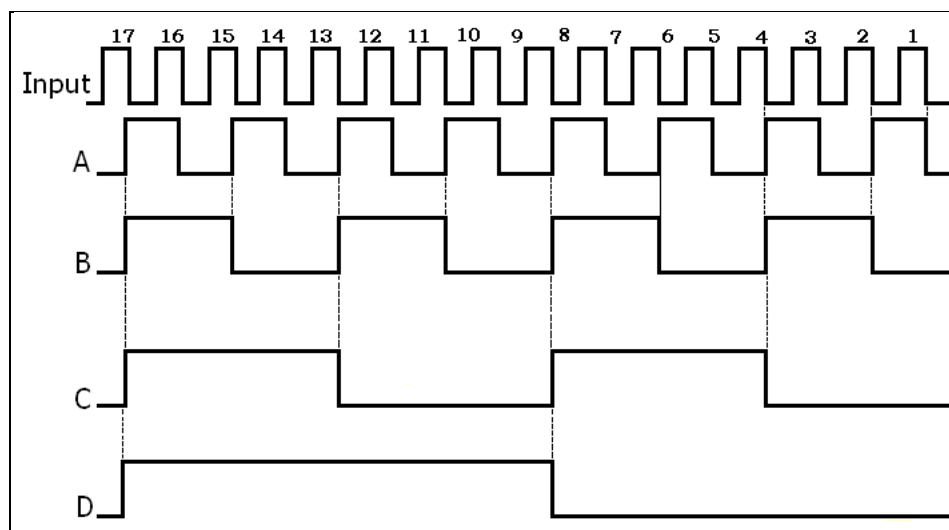
Fig. 3.4-4 Input and Output Waveforms of a Four bit Binary Down Counter

In analyzing the operation of this Counter, keep in mind that we still determine the contents of the counter by observing the normal output of the flip/flops as we did with the up-counter. Assuming the counter is initially reset and its contents are **0000**, the application of an input pulse will cause all flip/flops to set. With the A-flip/flop reset, its complement output is high.

When the first input pulse is applied, the A-flip/flop will set. As it does, its complement output will switch from binary 1 to binary 0, thereby toggling the B flip-flop. The B flip-flop becomes set and its complement output also switches from binary 1 to binary 0, causing the C-flip/flop to set. Similarly, the complement output of the C-flip/flop switches from high to low, thereby, setting the D-flip/flop. The counter recycles from **1111** to **0000**, as shown in Fig. 3.4-4. When the next input pulse arrives, the A flip-flop will again be complemented and reset. As it resets, the complementary output **($\overline{Q}$)** will switch from binary 0 to binary 1. The B-flip/flop ignores this transition. No further state changes take place and the content of the counter is **1110**.

This input pulse causes the counter to be decremented from 15 to 14. Applying another input pulse again complements the A-flip/flop to set state. As it sets, its complementary output switches from binary 1 to binary 0, causing the B flip-flop to reset. As it resets, the complement output B-flip/flop switches from binary 0 to binary 1. The C-flip/flop ignores this transition. The counter now contains **1101** or **13**. Again the input pulse causes the counter to be decremented by one. By using the Table 3.4-2 and the waveforms in Fig. 3.4-4, we can trace the complete operation of the 4 bit binary down counter.

UP/DOWN COUNTER

The up/down counting capabilities can be combined within a single counter, as illustrated in Fig. 3.4-5, using AND & OR gates to couple the flip/flops. The normal output **(Q)** of each flip/flop is applied to AND gate 1 in each stage for up-count control.
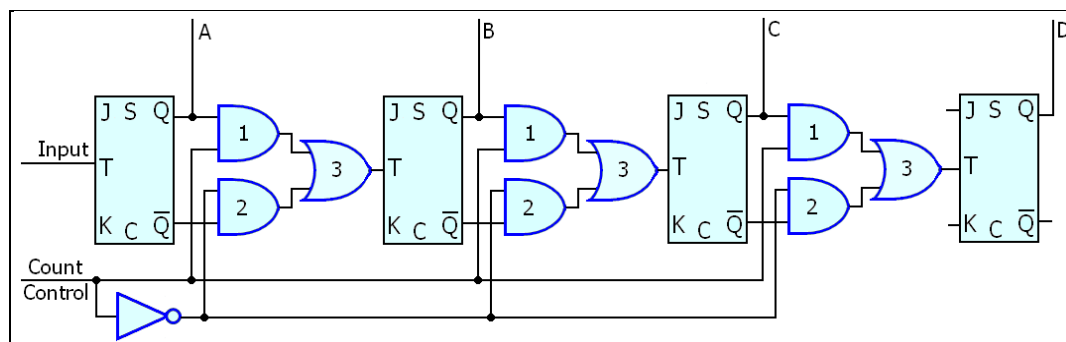

Fig. 3.4-5 Binary Up/Down Counter

The complement output of each flip/flop is connected to AND gate 2 in each stage for down-count control. These gates determine whether the normal or complement signal is applied to the next flip/flop in sequence through NOR gate 3 in each stage.

The count control line determines whether the counter counts up or down. If the count control input is binary 1, all gate 1s are enabled and the normal output of each flip/flop is coupled through gates 1 and 3 to the T-input of the next flip/flop in sequence for up-count while all gate 2s are inhibited. By making the count control line binary 0, all gate 2s are enabled and the complementary output of each flip/flop is coupled through gates 2 and 3 to the T-input of the next flip/flop in sequence for down-count while all gate 1s are inhibited.

ADVANTAGES OF BINARY RIPPLE COUNTER

- The primary advantage of a binary ripple counter is the simplicity in designing moderate speed sequential circuits, economically.

DISADVANTAGES OF BINARY RIPPLE COUNTER

Its primary limitation in counting speed is controlled by the propagation delay of the flip/flops cascaded in the counter. In a ripple counter, the propagation delay of the flip/flops is additive. More the flip/flops in the binary counter chain, more the propagation delay and lower is the frequency of operation. Since each flip/flop in the counter is triggered by the preceding circuit, it can take a significant amount of time for an impulse to ripple through all of the flip/flops and change the state of the last flip/flop in the chain.

The worst case condition in a binary counter occurs when all flip/flops in the counter change state, simultaneously, when maximum/minimum count **(1111/0000)** is reached just before recycling resumes again during up/down counting operation. Referring back to the waveforms for the four bit binary up counter in Fig. 3.4-2, the worst case condition occurs when the counter reaches the maximum count **1111** and the next pulse occurs to reset all flip-flops to **0000** and recycle again. In Fig. 3.4-4 for the four bit binary down counter waveforms, the worst case condition occurs when the counter reaches the minimum count **0000** and the next pulse occurs to set all flip/flops to **1111**

and recycle again. If each flip-flop in the four bit ripple counter has a propagation delay of **50ns**, it can take as long as **4×50 = 200ns** for the D-type flip/flops to change states limiting the maximum input signal frequency to:

f_{max} = 1/ (200ns) = 5MHz

If the input pulses occur at a rate faster than **5MHz**, the counter output transitions may lag the input signal and the binary number stored in the counter may not represent the true number of input pulses that have occurred. This means that the counter can count at speeds up to about 5MHz without counting errors.

At higher frequencies, the states of the flip/flops cannot keep pace with the rapid occurrence of the input pulses. The counter may actually miss several pulses depending upon the input frequency and the propagation delay. The direct solution to this problem, of course, is to use flip/flops with a lower propagation delay. Flip/flops are available to count at high frequencies up to **1GHz** with very small propagation delay. Such flip/flops generally employ non-saturating logic circuits, such as **ECL** to achieve high frequency operation at reasonably higher cost in **RF** applications.

Ex. 3.4-4

A six bit binary ripple counter has JK-flip/flops with propagation delay of 70ns each. Determine the maximum frequency of input signal that should not be exceeded to avoid miscount.

SOLUTION

1 flip-flop propagation delay = 70ns

6 flip-flop propagation delay = **6×70ns = 420ns**

f_{max} = 1/420ns = 2.3MHz **(2MHz)**

SYNCHRONOUS COUNTERS

As shown in Fig. 3.4-6, synchronous counters are the digital sequential circuits in which all flip-flop inputs/outputs are synchronized by a master timing signal known as Clock signal. The clock pulse or the signal to be counted triggers all the flip/flops,

simultaneously. It is possible to reduce the propagation delay effects and increase the counting speed of a binary counter by using Synchronous Counters.

In a synchronous counter, all the flip/flops trigger, simultaneously, by a clock pulse, or the signal to be counted. Since all flip/flops change state at the same time, the total propagation delay for the circuit is essentially equal to that of a single flip/flop. The propagation delays are not additive and, therefore, much higher counting speeds can be achieved. In the synchronous counter, as shown, all T-inputs of the flip/flops are connected together to a common count input line and, hence, due to this connection the name **Synchronous**.
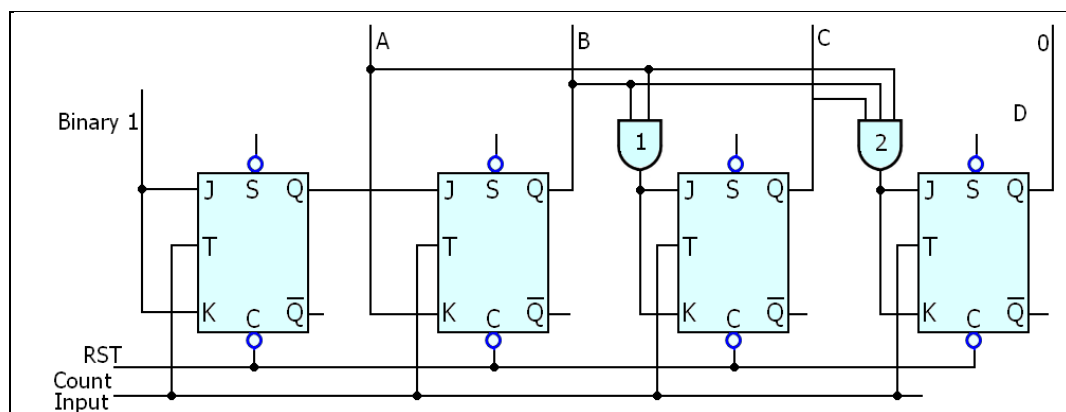
Fig. 3.4-6 Synchronous Binary Counter

The J & K-inputs are used as controls for the flip/flop and may be left open or connected to a binary 1 level. This essentially enables the flip/flop to be toggled or complemented each time the trailing edge of an input signal appears on the T-input line. If the JK-inputs are brought to binary 0, the signal applied to the T-input will be ignored and outputs remain unchanged as set or reset, previously. By using the JK-input lines, as shown, we can enable or inhibit the toggling of the flip-flops. In Fig. 3.4-6 for Synchronous Binary Counter, the JK inputs on the A flip-flop are connected to binary 1 to enable the flip/flops, permanently, for toggling mode.

Each time a count input signal appears the flip/flop will toggle or change state just as the A-flip/flop on the ripple counters. The JK-inputs to the B flip-flop being connected to the A-flip/flop output **(QA)** control the normal output **(QB)** of the B-flip/flop.

That means the only time B-flip/flop can change state is when the output of the A-flip/flop is binary 1. The JK-inputs to the C-flip/flop are controlled by the normal outputs of both the A and the B flip-flops. The A and B signals are ANDed together in gate 1 and its output used to control the JK inputs to the C flip-flop. In order for the C-flip/flop to change state, both A and B must be set **(QA = QB = 1)**.

The C-flip/flop will change state at the first count pulse occurring after A and B are set high. The D flip-flop is controlled by the A, B and C flip-flops where A, B and C signals are ANDed in gate 2 and the output of gate 2 used to control the JK inputs.

The output waveforms are similar to those in Fig. 3.4-2 corresponding to the counting sequence in the Table 3.4-1. Analyzing the state changes in the flip/flop operations will reveal the benefit of this binary counter, as follows: Assume that the counter contains the number **0111 (7)**. This means that the A, B and C-flip/flops are set and JK-inputs to the B, C and-D flip/flops are enabled. This means that upon the occurrence of the next input count pulse, all flip-flops will toggle to change states, simultaneously.

When this pulse occurs, flip-flops A, B and C will reset and the D flip-flop will be set with new number **1000 (8)** in the counter. The maximum delay between the occurrence of the input count pulse and the change of output state is only the longest propagation time of any one flip-flop in the circuit. Normally, all flip/flops of the same type have approximately the same propagation delay unlike the binary ripple counter with accumulative propagation delay.

ADVANTAGES OF SYNCHRONOUS COUNTER

1. The synchronous counter is **much faster** than binary ripple counter for the same type of flip/flops used.

2. All flip/flops in the synchronous counter change states at the same time.

As the counter changes from one state to the next, there are **no ambiguous states** unlike binary ripple counter with accumulative propagation delays that may occur as the frequency of operation increases.

3. The synchronous counter can be expanded to as many bits as required by the application unlike binary ripple counter with accumulative propagation delays.

DISADVANTAGES OF SYNCHRONOUS COUNTER

1. Each flip/flop in the counter must be controlled by all previous flip/flops in the counter through an AND gate.

2. The higher order flip/flops require AND gates with as many inputs as there are previous flip/flops and therefore, require **more complex circuitry** as expanded, adding small propagation delays having minor effects on the counting speed.

SHIFT REGISTERS

The shift register is one of the most versatile of all sequential logic circuits. A single shift register made up of many flip/flops as storage elements can be used as memory for storing many words of binary data. Shift registers can also perform **arithmetic operations**, such as multiplying by 2 (shift left) or division by 2 (shift right).

The shift register is also widely used for **parallel to serial** and **serial to parallel** data conversions in **transmitter** and **receiver**, respectively. The shift registers can also be used for generating a sequence of control pulses for a logic circuit. The shift registers are used in **frequency counter** applications.

BIPOLAR LOGIC SHIFT REGISTER

All shift registers make use of flip-flops in their construction and are available in MSI **(TTL/CMOS/ECL)** IC packages. As shown in **Fig.** 3.4-7, a typical shift register is constructed with JK flip-flops. The serial input data and its complement are applied to the JK inputs of the input A-flip/flop. The other flip-flops are cascaded with the outputs of one connected to the JK inputs of the next with clock pulses applied to the clock T-clock inputs to each flip/flop, simultaneously for synchronous operation. The active low asynchronous Clear C-inputs on each flip/flop, connected together to Vcc bus in series with a 10K resistor forming a Reset line, must be driven low (0V) for manual reset. Data applied to the input is shifted to the right through the flip/flops.

Each clock or shift pulse will cause the data at the input and that stored in the flip/flops to be shifted one bit position to the right.
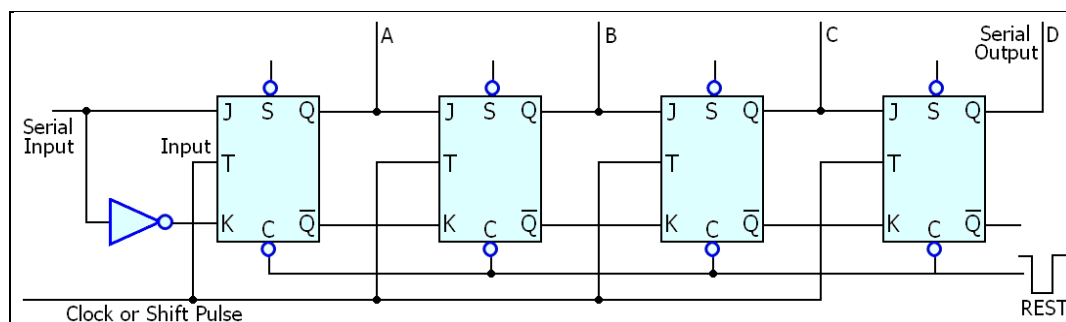
Fig. 3.4-7 Four bit Shift Register using JK-Flip/Flops

The waveforms in Fig. 3.4-8 illustrate how a serial word is loaded into the shift register. As the waveforms show, the binary number **01012** in serial form occurs in synchronization with the input clock or shift pulses from left to right.
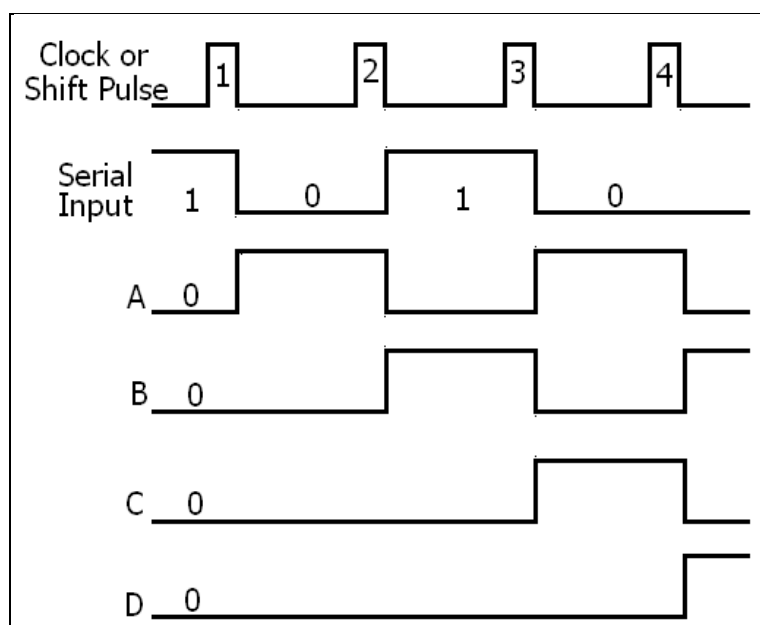
Fig. 3.4-8 Serial Shift Register Waveforms

This means that the clock pulses on the right occur after those on the left. In the same way, the state of the serial input shown on the left occurs prior the states to the right. Note that the shift register is initially reset. The A, B, C, & D-outputs of the flip/flops, therefore, are binary 0 as indicated in the waveforms. Prior to the application of the first shift pulse, the serial input state is binary 1. This represents first bit of the binary word to be entered. On the trailing edge of the first clock pulse, the binary 1 is loaded into the A-flip/flop. The JK inputs of the A-flip/flop are conditioned **(J=1, K=0)** such

that when the clock pulse occurs, the flip/flop will set. The **first clock/shift pulse** also being applied to all other flip-flops, the state stored in the A-flip/flop is transferred to the B flip-flop and the states stored in the B and C-flip/flops are transferred to the C and D flip-flops, respectively. Since all flip-flop states are initially zero, naturally no state changes in the B, C or D-flip/flops will take place when the first clock pulse occurs. After the first clock pulse, the A-flip/flop is set while B, C, and D-flip/flops are still reset. The first clock pulse also causes the serial input word to change.

The clock pulses are generally common to all other circuits in the system and, therefore, any serial data available in the system will generally be synchronized to the clock. The input to the A-flip/flop is now binary 0. When the trailing edge of the second clock pulse occurs, this binary 0 is written into the A-flip/flop. The A-flip/flop, which was set by the first clock pulse, causes the JK inputs to the B flip-flop to be such that it will become set when the second clock pulse occurs. As shown in the waveforms, when the **second clock pulse** occurs, the A flip-flop will reset while the B flip-flop will set. The 0 state previously stored in the B flip-flop is transferred to the C-flip/flop and the C-flip/flop state is shifted to the D flip-flop. At this point the first two bits of the serial data word have been loaded into the shift register. The serial input is now binary 1 representing the third bit of the serial input word. When the **third clock pulse** occurs, the A-flip/flop sets and its zero previously stored is transferred to the B flip-flop. The binary 1 stored in the B flip-flop is now shifted into the C-flip/flop. The D-flip/flop remains reset. The serial input to the A-flip/flop is now binary 0. When the trailing edge of the **fourth clock pulse** occurs, the A-flip/flop is reset. The binary 1 stored there previously is transferred to the B-flip/flop. The 0 stored in the B-flip/flop is shifted into the C flip-flop and the binary in the C-flip/flop now moves to the D-flip/flop. After **four clock pulses** have occurred, the complete **four bit binary** word **0101** is now shifted into the register, as indicated by the states shown in the waveforms. A glance at the flip/flop output waveforms will show the initial binary 1 bit moving to the right with the occurrence of each shift pulse. While we have illustrated the operation of the shift register with only four bits, as many flip/flops as needed, can be cascaded to form longer shift registers. Most shift registers are made up to store a single binary word **(4 bit** or **8 bit)**. Shift registers in digital

systems have a number of bits as a multiple of four bits. While shift registers are readily implemented with JK or D type flip/flops, in most applications **MSI** shift registers are used. MSI shift registers are available in four and eight bit sizes.

74LS95 TTL 4 BIT SYNCHRONOUS SHIFT REGISTER

Fig. 3.4-9 shows the logic diagram of **74LS95** TTL universal serial/parallel shift register. It consists of four flip/flops with the appropriate gating on the JK-inputs where a mode control input logic can gate either of the two clock signals. Depending upon the state of the mode control (0 or 1), either clock 1 or clock 2 is enabled by AND gate 13 or 14, respectively.
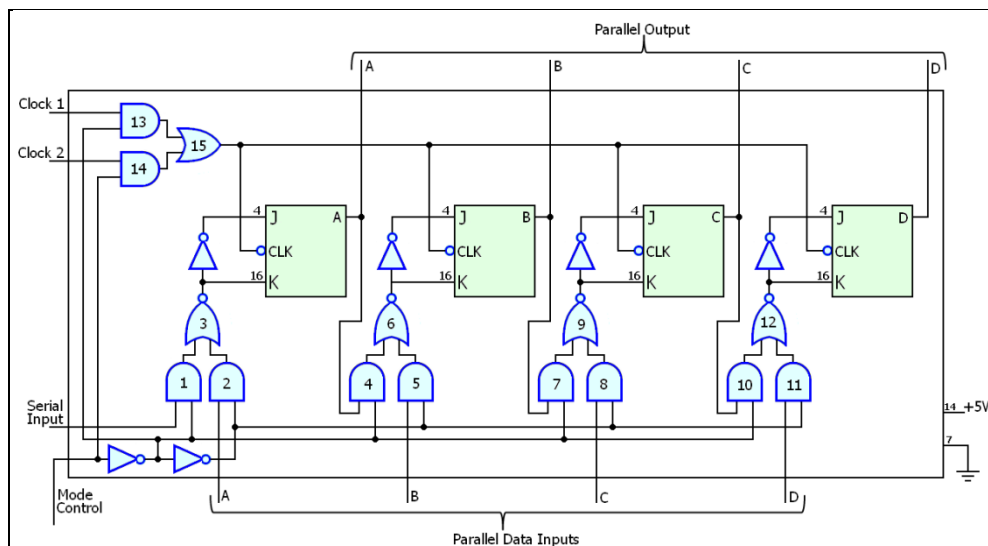
Fig. 3.4-9 Logic Diagram of 74LS95 TTL MSI Shift Register

When the mode control input is a binary 0, gates 1, 4, 7, and 10 are enabled. This causes the shift register to be set up to perform the basic **shift right** operation. Serial input is applied to gate 1 and passes through gate 3 to the JK-inputs of the A-flip/flop. The output of the A-flip/flop is connected to the inputs of the B-flip/flop through gates 4 and 6 and the outputs of the B and C flip-flops are connected to the inputs of the C and D-flip/flops, respectively. Also a binary 0 on the mode control input enables gate 13, permitting clock 1 pulse to pass through gates 13 and 15 to set/reset the flip/flops.

In this mode, the shift register performs the standard **shift right** operation. With mode control in the binary 1 state, gates 2, 5, 8, and 11 are enabled.

With these gates enabled and gates 1, 4, 7, and 10 inhibited, the parallel data inputs are enabled. Note that a binary 1 on the mode control input also enables gate 14 so that clock pulse 2 can set/reset the flip-flops. When a clock pulse occurs, an external 4 bit parallel word will be loaded into the flip/flops. In this mode, the shift register can be parallel loaded or preset to some desired value. With the mode control at the binary 1 logic, shift-left operation can also be performed. To perform a left shift, the D-flip/flop output is connected to the C-data input, the C-output is connected to the B-data input and the B flip-flop output is connected to the A-data input. The external serial data is input to D-input. When clock pulses are applied to gate 14, data will be shifted left from D to C, C to B, and B to A. With this connection, the mode control input acts as a shift right/left control line.

SUMMARY

- The sequential logic circuits consist of counters and shift registers.

- If we let a counter count the input pulses for one second, the binary number stored in the flip/flops represents the frequency of the input signal as pulses/sec or Hz.

- In an asynchronous counter, the first flip/flop in counter chain is clocked by a clock pulse and the output of each flip/flop is triggered by the ↓ output of the previous one independent of the clock.

- A four bit binary counter repeats after ($2^4 = 16$) clock pulses provided no reset is applied in between counting sequence.

- The maximum count capability of a binary counter is a function of the number of flip/flops in the counter.

- The main disadvantage of binary ripple counter is its primary limitation in counting speed controlled by the additive/accumulative propagation delay of the flip-flops cascaded in the counter.

- Shift registers can perform **arithmetic operations**, such as multiplying by 2 (shift left) or division by 2 (shift right).

GLOSSARY

IC:	Integrated Circuit.
TTL:	Transistor-Transistor Logic
MSI:	Medium Scale Integration.
MOS:	Complementary Metal Oxide Semiconductor
ECL:	Emitter-Coupled Logic
BCD:	Binary Coded Decimal.
LSB:	Least Significant Bit.
MSB:	Most Significant Bit.

Digital Clock: An oscillator that generates rectangular pulses at a fixed frequency.

D.C: Duty cycle

FORMULAE

$N = 2^n - 1$ Where N = The maximum count that occurs prior to recycling.

n = The number of flip-flops.

$$\textbf{Duty Cycle} = \frac{\textbf{t}}{\textbf{T}} \times \textbf{100\%}$$ Ratio of On-time **(t)** to the total period **(T)** of clock

REVIEW EXERCISE

CHOOSE THE CORRECT ANSWER FOR EACH OF THE FOLLOWING:

1. In a binary counter using JK-flip/flops (trailing edge trigger), the counter state will change when the T-input changes from:

   a) High to low ↓

   b) Low to high ↑

   c) Both a and b

   d) None of above

2. A four bit binary counter contains the number 0100. Nine input pulses occur. The new counter state is _____:

   a) 0010

   b) 1001

   c) 1011

   d) 1101

3. The output of each flip-flop is _____ the frequency of its input.

   a) one-half

   b) one-third

   c) one-fourth

   d) one-eighth

4. A binary counter constructed with two 74LS193 ICs has a maximum count capability of _____::

   a) 15

   b) 16

   c) 255

   d) 256

5. A binary counter made up of five JK-flip/flops divides an input frequency by ___.

   a) 5

   b) 8

   c) 16

   d) 32

6. If the input to 8 stage counter is a 100kHz square wave, the output at the last flip/flop is, approximately, _____kHz:

   a) 50

   b) 0.39

   c) 12.5

   d) 6.25

7. Determine the maximum number (N) that can be contained in a counter using 12 binary flip/flops.

8. All the flip/flops in a four bit BCD up-counter are, generally, _____ and those in a BCD down-counter are _____ before starting to count.

9. Clearing an up counter to zero is known as _____.

SHIFT REGISTERS

1. A parallel to serial shift register is widely used for data conversions in _____ for data to be transmitted 1 bit at a time.

2. A serial to parallel shift register is widely used for data conversions in the _____ to manipulate the received data words to be processed by the CPU.

3. The active high asynchronous Clear C-input on any CMOS flip/flop/counter/shift register connected to _____ bus in series with a 10K resistor forming a Reset line must be driven _____ for manual reset.

4. Given the logic diagram of 74LS95 TTL serial/parallel shift register in Fig. 3.4-10:

    i)   The mode control input logic can gate either of the two clock signals (1 or 2) through gates ____ or ____.

    a) 13 or 14   b) 13 or 15

    c) 12 or 15   d) 14 or 15

    ii) When the mode control input is a binary 0, gates 1, 4, 7, and 10 are enabled to perform shift right operation by clock 1 input pulse.

    a) True   b) False

    iii) With mode control in the binary 1 state, gates 2, 5, 8, and 11 are enabled and gates 1, 4, 7, and 10 inhibited for parallel data input transfer.
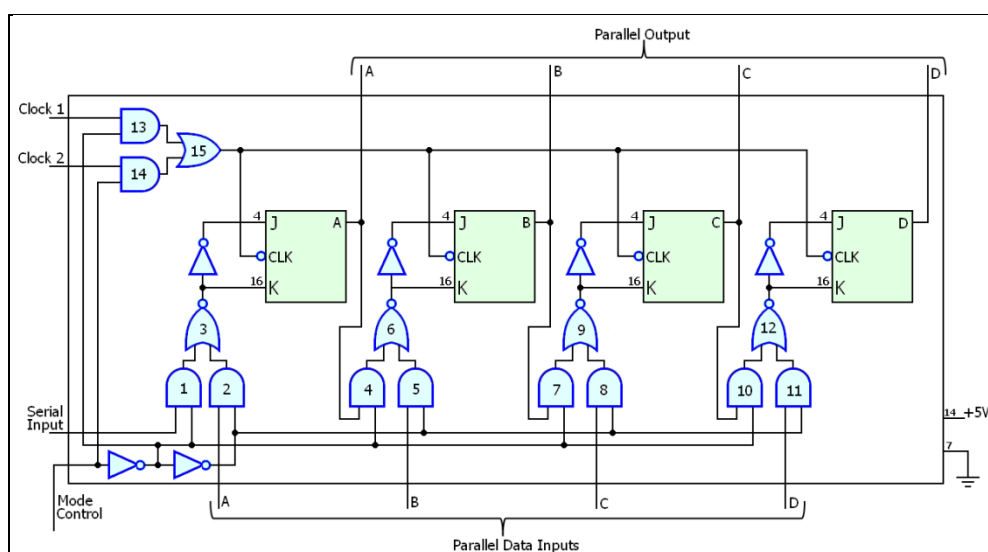
    a) True   b) False

Fig. 3.4-10 Logic Diagram of 74LS95 TTL MSI Shift Register

TASK 3.4-1

BINARY COUNTER

OBJECTIVE

Upon completion of this task, the trainees will be able to:

- Demonstrate the operation and characteristics of a Binary Counter.

TOOLS, MATERIALS, & EQUIPMENT

Heathkit ET-3200 Digital Design Experimenter or equivalent.

DC Voltmeter   2 - 74LS76 dual JK Flip-flop IC **(443-829)**

   -1 - 74LS193 synchronous up/down binary counter IC **(443-815)**

   -1 - 1K resistor

   -   Personal safety equipment as recommended in digital electronic workshop.

PROCEDURE

1.   On your ET-3200 Digital Design Experimenter, construct the four bit binary counter circuit shown in Fig. 1-1. The pin connections for the 74LS76 ICs are given in Fig. 1-2. Take care in wiring the circuit to avoid errors. Be sure to connect pin 5 of each IC to +5 volts and pin 13 of each IC to ground (GND). You will monitor the counter outputs on the LED indicators. You will stop the counter with the A-logic switch.

   Study the counter circuit in Fig. 1-1.
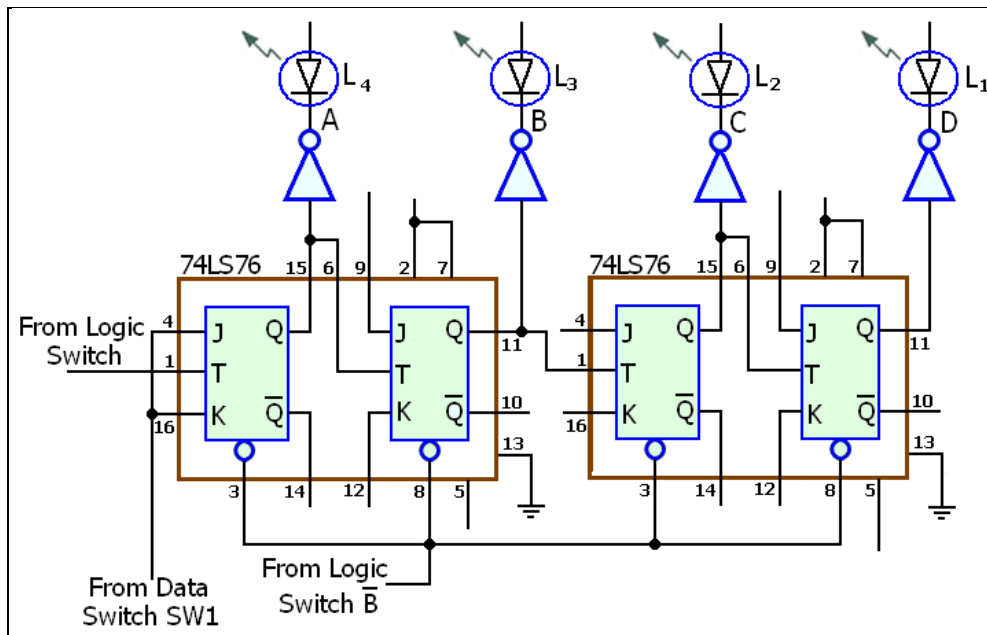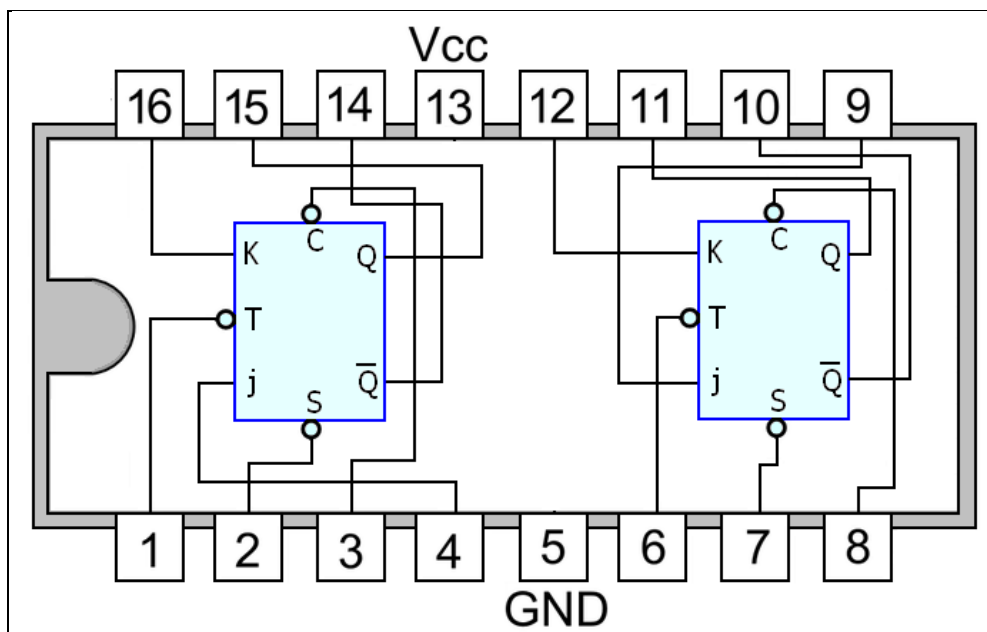
   What type of counter is this? _____

Fig. 1-1 Schematic Diagram of Binary Counter

Fig. 1-2 Pin Connection For Dual Jk-Flip/Flop (74LS76)

2. Set the switch (SW1) to the high or up position. Apply power to the circuit. Note the state of the LED indicators. Record the binary numbers stored in the counter. Note A(L4) = LSB, D(Ll) = MSB

D C B A = _____

3. Depress the B-logic switch. Note the state of the LEDs. Record the value of the binary word stored in the counter.

    D C B A = _____

    Does the change that takes place in the outputs occur on the leading or trailing edge of $\overline{B}$-signal? _____

4. Record the initial counter state obtained in Step 3 in the first (0) position of Table 1-1. Using the A-logic switch, step the counter. Each time you actuate the A-logic switch, observe the LED outputs and record the counter contents in Table 1-1.

    Does the counter state change when you depress or release the A-logic switch? What does this mean? _____

5. Observe your data in Table 1-1.

    What kind of counter did you construct? _____

    Does this data confirm your answer given in Step 1? _____

    When the counter content is DCBA = 1111, what happens when you depress the A-logic switch? _____

    The counter output becomes what? _____

    D C B A = _____

6. Remove the counter input from the A-output and connect it to the CLK-output. Set the clock frequency to 1 Hz. Depress the B-pushbutton and hold it. Observe the LED indicators. Then release the B-pushbutton and let the counter count. As it counts slowly, verify its outputs against your data in **Table 1-1**. Let the counter run until you fully understand the count sequence.

7. As the counter is counting, set data switch SW1 to the low or down position and observe the result. Repeat several times to be sure you understand what happens.

What effect does SW1 have? _____

Depress the B-logic switch while the counter is counting. What happens?

_____

    Return the counter input to the A-output of the logic switch.

	D	**C**	**B**	**A**
0				
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				

Table 1-1 Binary Counter Outputs

8. Modify the counter to conform to the circuit in Fig. 1-3. Be careful in making your wiring changes to avoid errors. Study the counter circuit you have just wired. What kind of counter is it?
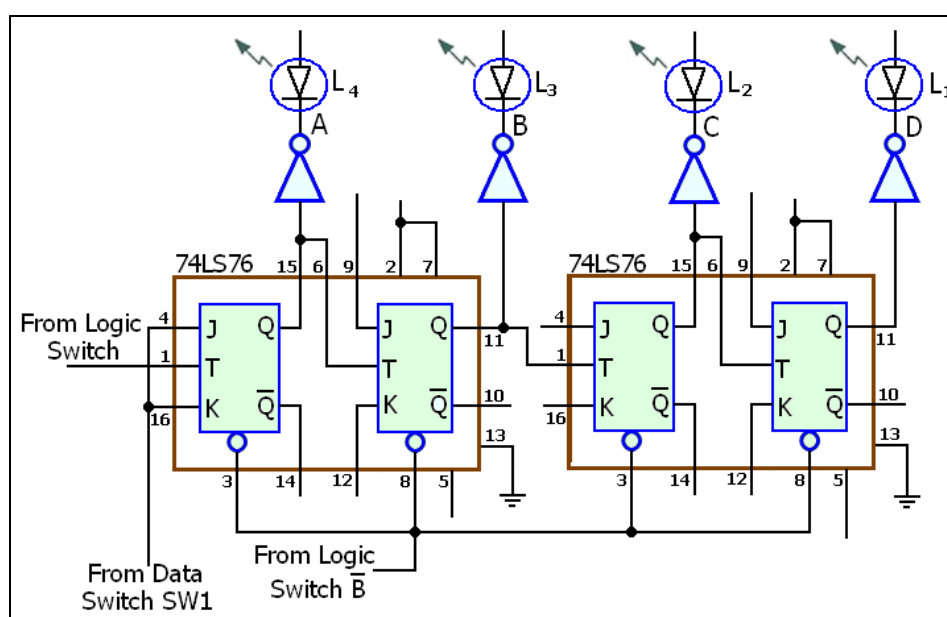

Fig. 1-3 Binary Counter for Steps 8, 9, and 10

9. Apply power and note the counter output state.

    DCBA = _____.

Now momentarily depress the B-logic switch. Record the counter output state below.

DCBA = _____.

What happened here? _____

10. Record the counter state obtained in the latter part of **Step 9** in the first position of **Table 1-2**. Use the A-logic switch and step the counter. In **Table 1-2**, record the counter state after each actuation of A-switch. 11.   Convert   the   binary numbers you recorded in **Table 1-2** into their decimal equivalents and record them in the far right hand column of **Table 1-2**.

12. Observe your data in **Table 1-2**.

    What kind of counter is this? _____

    Does this confirm your answer in **Step 8**? _____

13. Connect the counter input to the CLK-output (1 Hz) as you did in **Step 6**. Let the circuit count. As you do, observe the output states and compare them to your data in **Table 1-2**. Let the counter run for a while until you see the count pattern or sequence.

D	C	B	A	DECIMAL

Table 1-2 Binary Counter Outputs

14. While the counter is stepping, set the SW1-logic switch to binary 0. Note the result. Next, while the counter is stepping, depress the B-logic switch.

What happens in each case? _____

15. Wire the counter circuit shown in **Fig. 1-4**. Use a type- 74LS193 IC (443-815). Be sure to connect +5 volts to pin 16 and ground t. pin 8. The pin connections for the 74LS193 IC are shown in **Fig. 1-5**. You will step the counter with the A logic switch and reset it with the B logic switch. The data switches SW1 through SW4 serve as parallel data source for presetting the counter.
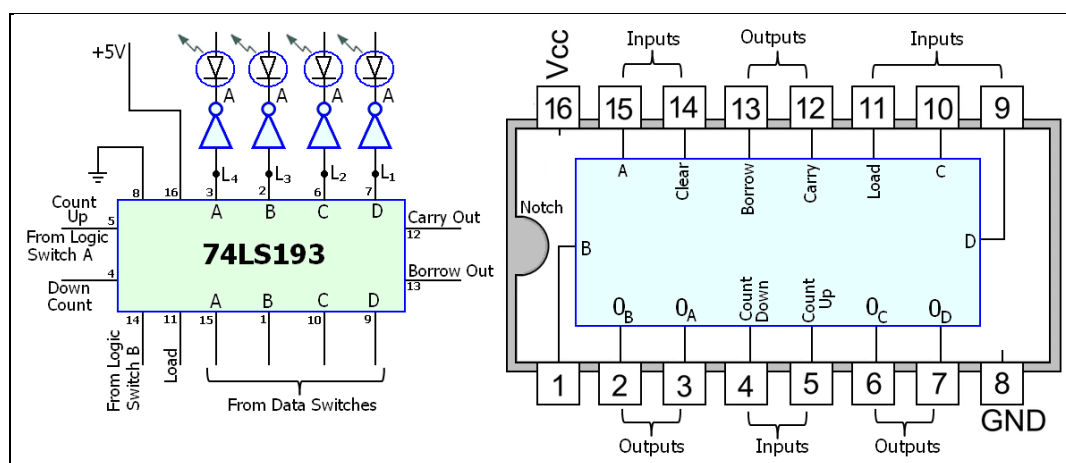
Fig. 1-4 Counter Circuit
using a 74LS193 IC

Fig. 1-5 Pin Connections of
74LS193 Binary Up/Down Counter

16. Apply power to the circuit. If the state of the counter is other than 0000, reset it with the B-pushbutton. Step the counter 16 times with the A-pushbutton. Note the output states on the LED indicators after each step.

Compare the states to those you recorded in Table 1-1.

What type of count sequence does this IC counter generate? _____

17. Reverse the wires at pins 4 and 5 of the IC. Reset the counter with the B-logic switch. Apply 16 pulses with the A-logic switch and observe the counter output states. Compare them to the data you recorded in **Table 1-2**.

What kind of count sequence is generated? _____

18. Remove the wires connected to pins 4 and 5 of the IC. Connect pin 4 to +5V through the 1K resistor. Connect pin 5 of the IC to CLK. Be sure the clock

frequency is set to 1Hz. Connect a DC voltmeter between GND and pin 12 of the IC. Set the meter for a reading in the zero to +5 volt range.

19. Note the voltmeter reading as the counter is stepped by the clock. Record below. At some point in the count cycle, the voltage at pin 12 will change momentarily. When it does, note the new output voltage and the binary state of the counter during the change. Record below.

    Voltage at pin 12 before the change is (during counting): _____ volts

    Voltage at pin 12 after the change is (momentary): _____ volts

    Binary Code DCBA = _____ (during momentary change)

20. Reverse the wires at pins 4 and 5 of the IC. Connect the voltmeter to pin 13. Repeat **Step 19**. Record the data below.

    Voltage at pin 13 before the change is (during counting): _____ volts

    Voltage at pin 13 after the change is (momentary): _____ volts

    Binary Code DCBA = _____ (during momentary change)

21. Remove the wires at pins 4 and 5 of the IC. Connect pin 4 to +5V through the 1K resistor. Connect pin 5 to the A output of logic switch A. Remove the wire between B and pin 14 on the IC. Connect pin 14 to ground. Connect $\overline{B}$ to pin 11. The DC voltmeter can also be removed at this time.

22. Set all of the data switches (SW1-SW4) to binary 1. Depress the B-logic switch. Note the output state of the counter.

    Next, set all data switches to binary 0. Depress the B-logic switch and observe the LED indicators.

    DCBA = _____

    Set the data switches to words indicated below.

SW1	SW2	SW3	SW4
0	1	0	1
1	0	1	0

    After each word is set into the switches, depress B and note the counter state of the LED indicators. Compare this state to the data switch settings.

    What conclusion can you draw from this step? What function is taking place?

23. Leave the data switches set to 0110. Depress the B logic switch. Note the counter state. Then start stepping the counter with the A logic switch.

What happens? _____

TASK 3.4-2

SHIFT REGISTER

OBJECTIVE

Upon completion of this task, the trainees will be able to:

- Demonstrate the operation of TTL Integrated Circuit Shift Registers.

TOOLS, MATERIALS, & EQUIPMENT

- Heathkit Digital Design Experimenter ET-3200
- 1 - 74LS04 IC **(443-755)**
- 2 - 74LS76 IC **(443-829)**
- 1 - 74LS95 IC **(443-814)**
- Personal safety equipment as recommended in digital electronic workshop.

PROCEDURE

1. Construct the four bit shift register circuit shown in Fig. 2-1. You will use type 74LS76 dual JK flip-flops. Shift pulses for the circuit will be derived from A-logic switch. Logic switch B is connected to reset the shift register via the asynchronous clear inputs on the flip-flops. The serial input to the shift register is fed from data switch (SW1). Note that one of the inverters in a 74LS04 IC is used to make the JK inputs of the first complementary flip/flop. The shift register outputs will be monitored on the LED indicators. Don't forget to connect +5 volts and ground to each IC.

2. Apply power to the circuit. Reset the shift register by actuating the B-logic switch. Set data switch (SW1) to the binary 1 position. Then using the A-logic switch, apply 4 shift pulses. Observe the LED indicators as you apply the pulse. Record the binary value of the register contents after four shift pulses.
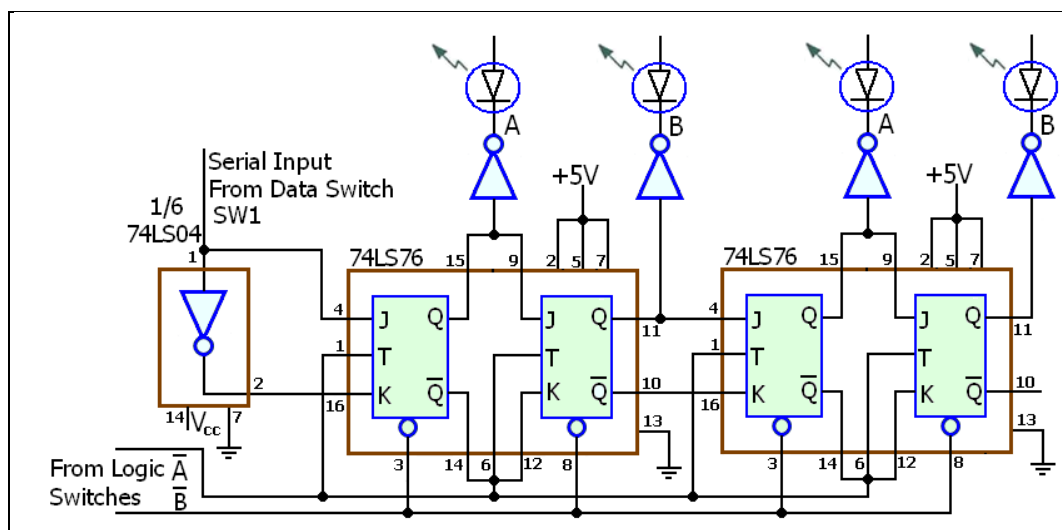
Fig. 2-1 Shift Register Circuit

Next, set the SWl-switch to binary 0. Again apply four shift pulses with the A-logic switch. Again record the binary contents of the register.

ABCD = _____

3. Using the SWl-data switch and the A-logic switch, load the shift register by using the step-by-step procedure given below.

SWl = 1, depress switch A

SWl = 0, depress switch A

SWl = 1, depress switch A

SW1 = 0, depress switch A

After you have loaded the shift register, observe the LED indicators and in the space below write the decimal equivalent of the binary number in the shift register.

Decimal number = _____

4. Construct the shift register circuit shown in **Fig. 2-2**. At this time you can disassemble the shift register circuits used in the previous steps. The shift register shown in Fig. 2-2 is a 74LS95 IC. This is an MSI shift register already completely wired internally and ready to se. The flexibility of the input/output leads permits this device to be used for a wide variety of functions. It eliminates the need to interconnect individual flip/flops to perform shift register operations. As before

you will use the LED indicators to observe the shift register contents. Data switches (SWl) through (SW4) will be used as a parallel data source for the shift register. Logic A-switch will be used to generate the shift pulses as in the previous steps. Logic B-switch will serve as a mode control for the circuit. Don't forget to connect +5 volts and ground to the 74LS95 IC.
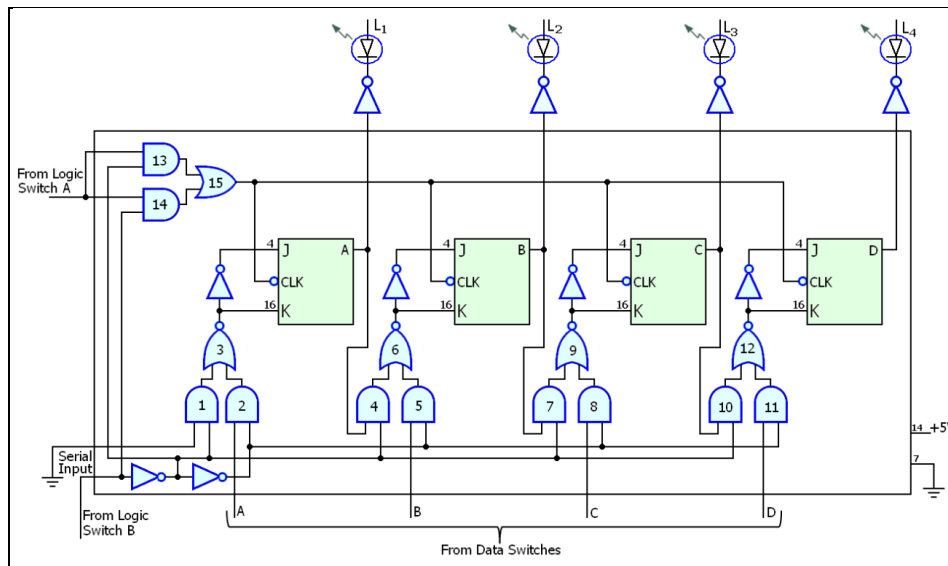

Fig. 2-2 Serial-Shift Register Circuit

5. Apply power to the circuit. As before, the flip/flops in the shift register can come up into any state. Disregard the LED indicator states at this time. Set all of the data switches to binary 0. Then depress the B-logic switch and hold it in the down position. Then momentarily depress the A-logic switch. Note the LED indicator states and record below.

DCBA =-_____

Next, set all of the data switches to binary 1. Again depress the B-logic switch. Holding it in the low position, actuate the A-logic switch momentarily. Release both switches. Observe the LED indicator states and record the binary number below.

DCBA =-_____

Depress the A-logic switch four times and note the LED indicator states. After you have applied four shift pulses, record the LED indicator states below.

DCBA =-_____

6. Modify your 74LS95 shift register circuit to conform to the configuration shown in Fig. 2-3. Here you are connecting the parallel data inputs back around to the outputs in order to permit the shift register to perform shift left operations. As before you will use the A-logic switch to generate shift pulses. Data switch (SW1) will be used for a serial data input for shift right operations. (SW4) will be used as the data source for shift left operations. Switch (SW2) will be used to control the mode of the circuit. The mode control will select either shift right or shift left operations.
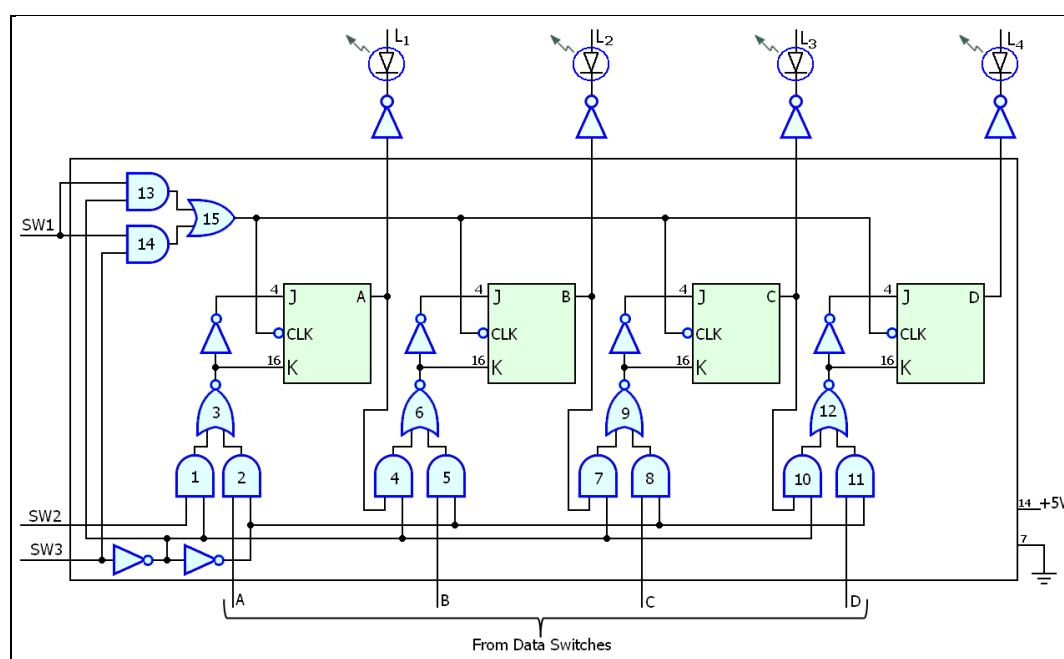
Fig. 2-3 Serial Left/Right-Shift Register Circuit

Studying the circuit in Fig. 2-3, determine the binary state of the mode control input to perform shift left operations. _____

7. Set data switches (SW2), and (SW4) to the binary 0 state. Apply power to the circuit and depress the A-logic switch four times. Record the state of the LED indicators below.

ABCD = _____

Next, set switch (SW1) to the binary 1 position. Depress the A-logic switch four times. Note the direction of shifting as the input pulses are applied. After four pulses have been applied, record the state of the register below.

ABCD = _____

8. Set data switch (SWl) to binary 0. Again depress the A-logic switch four times. Note the direction in which the data shifts. Next, set SW2 to binary 1 and the SW4 switch to binary 1. Apply four shift pulses with the A-logic switch. Again note the direction of shifting, and record the contents of the register below.

ABCD = _____

Set the (SW4) switch to binary 0 and apply two shift pulses. Note the direction of the shifting and record the LED indicator states in the space below.

ABCD = _____
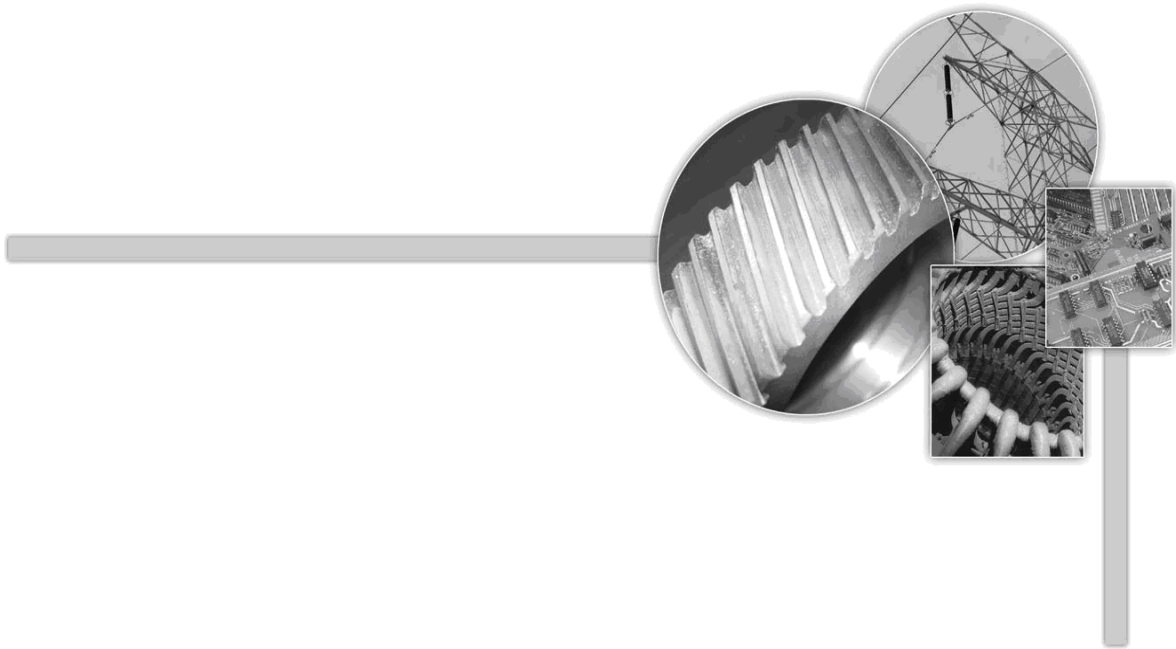
LESSON 3.5

DECODER & ENCODER

LESSON 3.5

DECODER & ENCODER

OVERVIEW

This lesson deals with the construction, operation and application of Decoders, Encoders, Multiplexers and De-Multiplexers. The trainees would learn how to implement, test, maintain and troubleshoot respective hardware circuits to understand their operation in digital applications.

OBJECTIVES

Upon completion of this lesson the trainee should be able to:

- Explain the function of a Decoder.
- Build and test a simple decoder using simple digital gates and inverters.
- Describe the operation of 4-input BCD-Decimal decoder using the truth table.
- Describe the operation of 3-8 and 4-16 decoders.
- Give an application of 4-input BCD-7 Segment decoder to drive displays.
- Describe two methods of driving displays and their advantages and advantages.
- Give examples of BCD-7 Segment Hex decoder/drivers.
- Explain the function and operation of an Encoder and list three applications.
- List the two types of multiplexing techniques.

DECODERS

Combinational logic circuits are digital circuits that are made up of gates and inverters. The output of a combinational logic circuit is a function of the states of its inputs, types of gates used and how they are interconnected. There are certain combinational logic circuits that output logic levels at regular intervals. These circuits are called decoders, encoders, multiplexers, comparators and de-multiplexers. One of the most frequently used combinational logic circuits is the Decoder. A decoder is a logic circuit that converts 1, 2, 3 or 4 bit binary numbers into decimal.

$\quad$ **$2^n = N$** $\qquad$ Where $\qquad$ n = Number of bits at the input of a decoder

$\qquad\qquad\qquad\qquad\qquad\qquad$ N = Number of output states in decimal

A one bit binary decoder is simply an inverter IC forming 1-of-2 decoder and giving two output states 0 or 1. The number of gates required in a decoder is equal to the total number of outputs possible, except the one bit decoder. **$2^1 = 2$**

A 2-bit binary **1-of-4** decoder giving four output states 00_2, 10_2, 10_2 and 11_2 requires **four** 2-input AND gates and two inverters for 0, 1, 2 or 3 outputs, respectively. **$2^2 = 4$**

Similarly, 3-bit binary **1-of-8** decoder giving eight output states 000_2, 001_2, 010_2,…. 111_2 requires **eight** 3-input AND gates and three inverters for 0, 1, 2….7 outputs, respectively. **$2^3 = 8$.** The decoder will detect the presence of a specific binary number or word. The input to the decoder is a parallel binary number and the output is a decimal signal that indicates the presence or absence of that specific number within the binary range in decimal. The basic decoding circuit is an AND gate where the output is a binary 1 only if all inputs are binary 1. By properly connecting the inputs from the data source to an AND gate, the presence of any binary number is detected. **Fig. 3.5-1A** shows a two input AND gate used to detect the presence of the 2-bit binary number 01 (B=1 & A=0), A-input having an inverter in series. The number to be detected consists of two bits A and B with B as the Least Significant Bit **(LSB)**. When A is 0 and B is 1, both inputs to the AND gate are high and the output C will be a binary 1 indicating the presence of the desired number.(1_{10}) The inverter on the A-input causes the upper input to the AND gate to be binary 1 when the A-input is binary 0. For any other combination of input bits the decoder output will be binary 0.
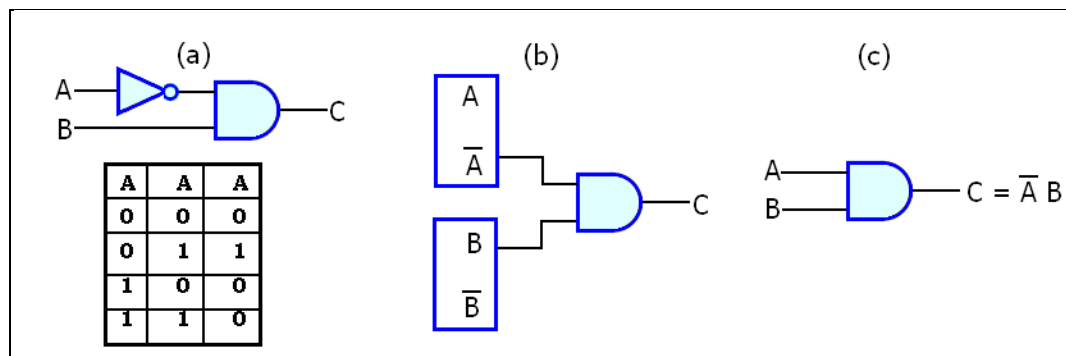
Fig. 3.5-1 Two Input AND Gate Decoders used for detecting Number 01

The truth table accompanying the circuit in Fig. 3.5-1A illustrates the performance of the circuit with all possible combination of the two inputs. Note that when the input number is 01, the output C is binary 1 detecting the presence of the number 01.

For all other two input combinations the output is binary 0. Fig. 3.5-1B shows the AND gate decoder for detecting the number 01 where the binary number input source is a flip-flop register. Since the complement outputs of the flip-flops are available, the inverter is not needed.

When the A flip/flop is reset and the B flip/flop is set, the number stored in the register is 01 so that $\overline{A}$ and $\overline{B}$ outputs are high for the decoder output high. To simplify the drawing of a decoder circuit, the AND gate input source is often omitted, as shown in Fig. 3.5-1C, with only the input states at the gate inputs.

An AND gate can be used to detect any binary number, 00, 01, 10 or 11 at the input.

The number of inputs to the gate will be equal to the number of bits in the binary word. Fig. 3.5-2 shows a four input decoder to detect the binary number $\overline{A}B\ \overline{C}D = 0101$ (5_{10}) where D is the LSB. Note that the decoding gate receives its inputs from a 4-bit parallel input register. When the number 0101 is present in the register, the output of the decode gate will be a binary 1. For any other 4-bit number in the register, the decoder output will be a binary 0.
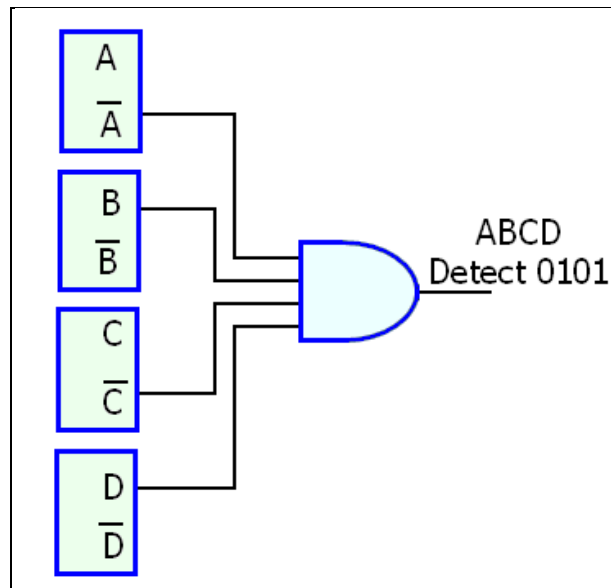
Fig. 3.5-2 4-Input AND Gate used to decode 0101

While there are some situations where the presence of a single binary word must be recognized, most applications require the detection of all possible states that can be represented by the input word. With a 2-bit input word there are total of $2^2 = 4$ different possible combinations of input states 00, 01, 10 and 11, as shown in Fig. 3.5-3 with four AND gates used to decode the four possible combinations.

A two bit binary word with bits A and B (B is the LSB) is stored in a flip/flop register. The Gate 4 detects the 00 input state with binary number AB=00 or complementary $\overline{A}\ \overline{B}$=11 as inputs stored in the flip/flops and thereby producing a binary 1 output.

Inputs			Outputs			
DP	A	B	W	X	Y	Z
0	0	0	1	0	0	0
1	0	1	0	1	0	0
2	1	0	0	0	1	0
3	1	1	0	0	0	1
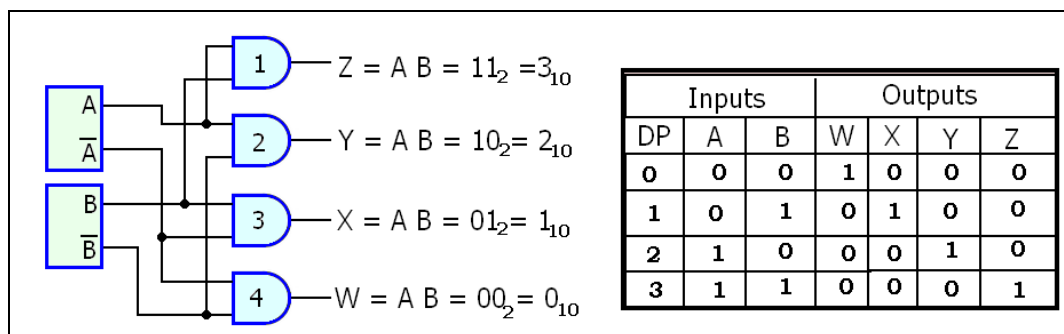
Fig. 3.5-3 One of Four Decoder

Gate. 1, 2 and 3 will have a binary 0 on at least one of their inputs keeping their outputs low. The truth table in Fig. 3.5-3 shows the four possible input states and the

outputs of each of the decoder gates giving four respective decimal number indicators for 0, 1, 2 and 3. If A and B -flip/flops are both set, the register is storing the binary number 11_2 (3_{10}). Gate 1 is enabled and its output indicates the presence of particular number 11_2 in the register. The output of this gate could then be used to turn on an indicator light marked with the decimal number 3.

BCD TO DECIMAL DECODER

One of the most common applications for decoder circuits is binary to decimal conversion. A widely used type of decoder is the BCD to decimal decoder. The input to the decoder is a parallel f4-bit number representing the BCD digits 0000 through 1001. Ten AND gates are used to look at or observe the inputs AND gates decode the ten possible output states 0 through 9. When a BCD number is applied to this decoder, one of the ten output lines will go high indicating the presence of that particular BCD number. The output of such a decoder is generally used to operate a lighted decimal number read-out or display.

A typical BCD to decimal decoder is shown in Fig. 3.5-4. The four bit BCD number with bits designated A, B, C, AND D are applied to ~e inverters which generate the normal AND complement versions of five inputs to be applied to the decoder gates. A-Bit is the LSB. Note also that NAND gates are used instead of AND gates for the decoding process. When all of the inputs to a NAND gate are binary 1, its output will be binary 0. For all other input combinations, the output will be binary 1. For that reason, all of the outputs from the gates in this decoder are high except the one decoding a specific input state in other words, the decoder outputs are active low (0).

74LS42 BCD TO DECIMAL DECODER

The most widely used BCD to decimal decoder **(74LS42)** with active low outputs used as drivers for LED indicators (0-9). The input to the decoder is a parallel 4-bit number representing the BCD digits 0000_2 - 1001_2. The NAND gates are used to decode the ten possible output states 0 through 9. When a BCD number is applied to

the inputs, one of the ten output lines goes low indicating the presence of that particular BCD number. The outputs of such a decoder are generally used to light LEDs or incandescent lamps decimal numbered 0-9, as shown in Fig. 3.5-4. The four bit BCD number with bits designated A **(LSB)**, B, C and D **(MSB)** are applied to the inverters, generating the normal and complements of the inputs to be applied to the decoding gates. The NAND gates are used instead of AND gates for the decoding process so that when all the inputs to a NAND gate are binary 1s, its output will be binary 0 (active low). For all other input combinations the output will be binary 1 (non-active high) and for that reason, all of the outputs from this decoder are high except the one decoding a specific input' combination.
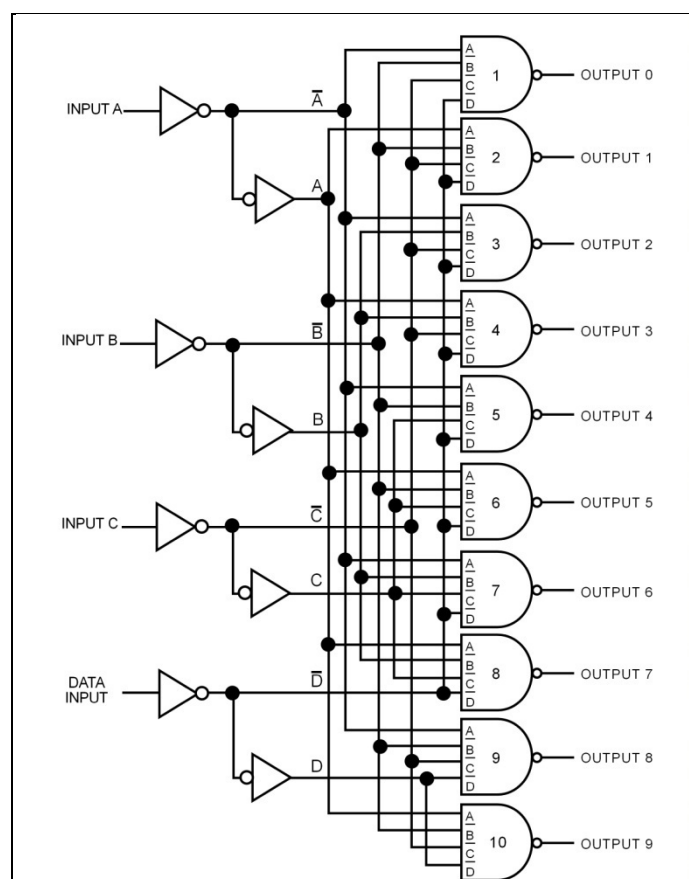
Fig. 3.5-4 TTL 74LS42 BCD to Decimal Decoder

The decoder circuit in Fig. 3.5-4 can be readily constructed using discrete NAND gates and inverters. Fig. 3.5-4(a) depicts internal schematic of the 74LS42 decoder IC and Fig. 3.5-4(b) shows the corresponding pin-outs. Table 3.5-1 shows the truth table

of the BCD to decimal decoder above. When one of the ten 8421 BCD codes is applied to the input, the appropriate output will go low.

For example, when the parallel input 0110 (6_{10}) is applied to the decoder, all inputs to gate 7 will be binary 1. The output of gate 7 goes low indicating the presence of the 4-bit BCD number representing a decimal 6 at the input with all other gate outputs high (de-activated). Notice if any one of the six **invalid** BCD codes above 1001 (9) is applied to the input of the decoder, all outputs will remain high.

#	BCD INPUTS				DECIMAL OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	L	H	H	H	H	H	H	H	H	H
1	0	0	0	1	H	L	H	H	H	H	H	H	H	H
2	0	0	1	0	H	H	L	H	H	H	H	H	H	H
3	0	0	1	1	H	H	H	L	H	H	H	H	H	H
4	0	1	0	0	H	H	H	H	L	H	H	H	H	H
5	0	1	0	1	H	H	H	H	H	L	H	H	H	H
6	0	1	1	0	H	H	H	H	H	H	L	H	H	H
7	0	1	1	1	H	H	H	H	H	H	H	L	H	H
8	1	0	0	0	H	H	H	H	H	H	H	H	L	H
9	1	0	0	1	H	H	H	H	H	H	H	H	H	L
10	1	0	1	0	H	H	H	H	H	H	H	H	H	H
11	1	0	1	1	H	H	H	H	H	H	H	H	H	H
12	1	1	0	0	H	H	H	H	H	H	H	H	H	H
13	1	1	0	1	H	H	H	H	H	H	H	H	H	H
14	1	1	1	0	H	H	H	H	H	H	H	H	H	H
15	1	1	1	1	H	H	H	H	H	H	H	H	H	H

(rows 10–15 marked as **INVALID**)

Table 3.5-1 Truth Table for 74LS42 BCD to Decimal Decoder

OCTAL AND HEXADECIMAL DECODERS

Octal-and hex-decoder circuits are widely used in microprocessor-based systems to decode the memory address to be accessed.
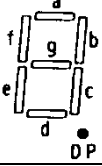
Instead of drawing the complex logic circuitry for a decoder, a simplified block diagram is often used for schematic diagrams. The **74LS138** 3-8 octal decoder, as

shown in **Fig. 3-5(a)**, accepts a parallel 3-bit input word 2^3 (8) to decode any one of eight possible outputs 000-111 (0-7). The 74LS42 BCD to decimal decoder circuit in Fig. 3.5-4 can be used as an octal decoder by simply using the A, B, and C inputs only. The D input is simply wired to a binary 0 condition and the 8 and 9 outputs from gates 9 and 10 are ignored. The 74LS154 4-16 hex decoder, as shown in Fig. 3.5-5(b), decodes any one of 2^4 (16) states represented by 4-bit input combinations, 0000-1111 (0-15).

Fig. 3.5-5(a) 74LS138 Octal 3-8 Decoder   Fig. 3.5-5(b) 74LS154 Hex 4-16 Decoder
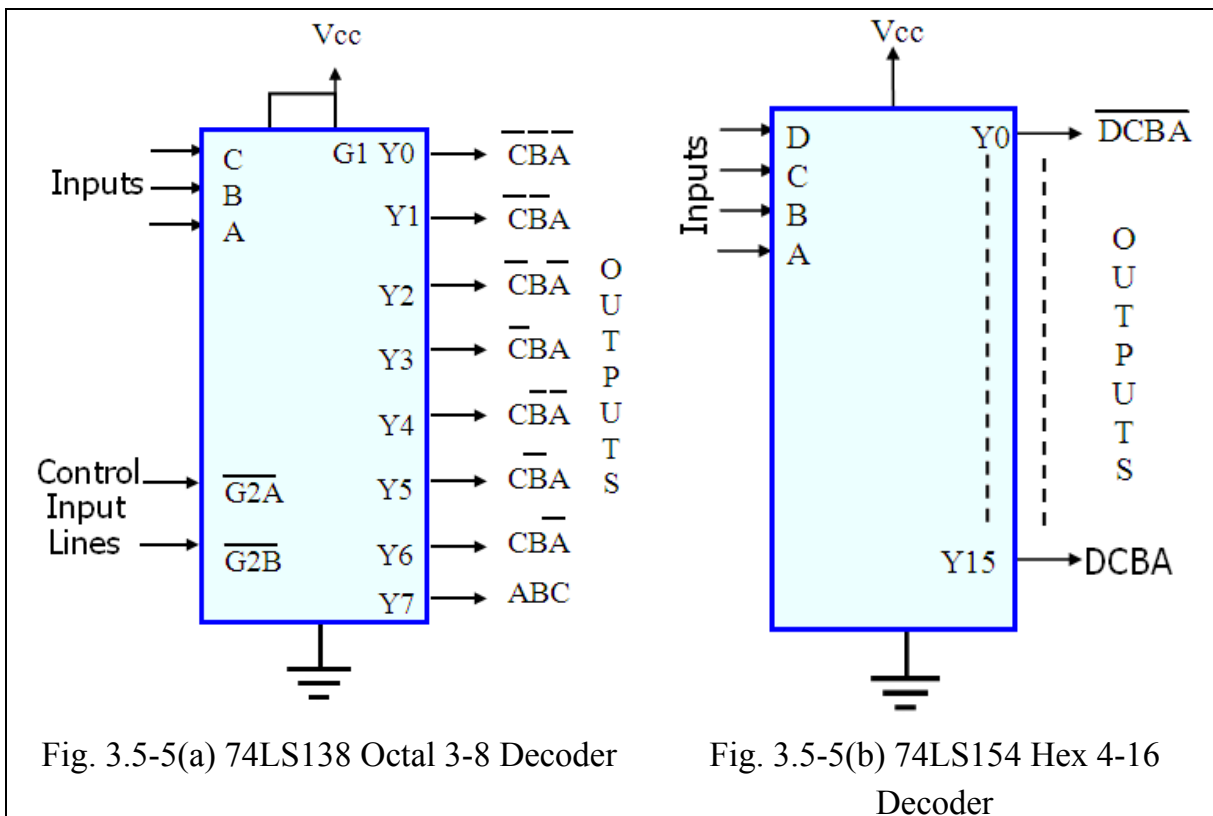
BCD TO 7-SEGMENT DECODER INTERFACING WITH DISPLAY

A special form of decoder circuit **74LS47** is the popular BCD to 7-segment decoder-driver used to drive multiple display segments, as shown in Fig. 3.5-6. This is a combinational logic circuit that accepts the standard 8421 BCD input code to generate a special 7-bit output code to drive the widely used 7-segment decimal readout display and is available in a single **MSI** package.

	Hex						
	DP	10	11	12	13	14	15
Fig. 3.5-6(a) 7-Segment Display	Fig. 3.5-6(b) Special Letters for Hexadecimal						

The standard 7-segment display configuration is shown in Fig. 3.5-6(a). A 7-segment readout is an electronic component used to display the decimal numbers 0 through 9 and other special letters A (10), b (11), c (12), d (13), E (14) and F (15) for hexadecimal range by illuminating two or more segments, as shown in Fig. 3.5-6(b). The segments can be constructed with a variety of light emitting elements such as an incandescent filament, a light emitting diode, fluorescent tube, gas discharge tube or a liquid crystal segment. Fig. 3-7 shows the typical 7-segment representation of these numbers.
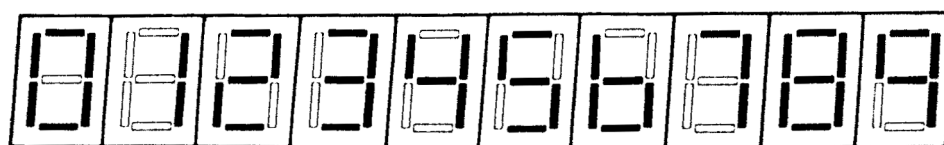
Fig. 3.5-7 7-Segment Format for 0-9 Numbers

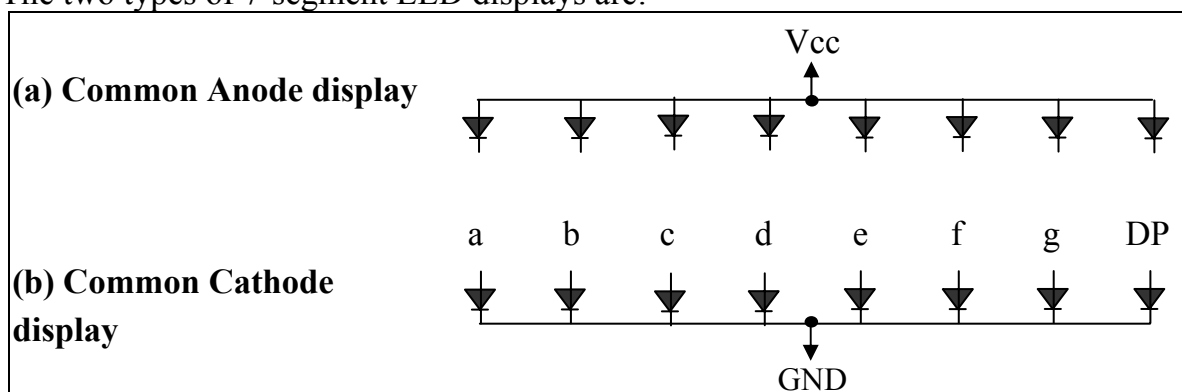The two types of 7-segment LED displays are:

Fig. 3.5-8 7-Segment LED Displays

As shown in Fig. 3.5-8(a), the common Anode terminal is connected to the Vcc side to forward bias the LEDs to be lit sourcing the driving current through the open-collector output circuit of a 7-segment decoder. Similarly, the common Cathode terminal in Fig.

3.5-8(b) is connected to the GND side to forward bias the LEDs to be lit sinking the driving current through the output emitter-follower circuit of a 7-segment decoder.

DIRECT DRIVEN 7-SEGMENT DISPLAYS

Fig. 3.5-9 shows the BCD-to-7 segment decoder to drive the display segments, directly through the 7 current limiting resistors in series. The number 8 is lit when all seven segments are illuminated. If each segment draws **22mA**, the total current is **22mA × 7 = 154mA** per digit, when each segment is current limited by **160Ω**, using 5VDC source and allowing 1.5VDC across each segment. For a 6-digit LED display driven directly, the worst case total current will be **154mA × 6 = 924mA**.

As the number of display digits is increased, the total current increases with the number of decoders and 4-bit latches required, as each display is driven by its own decoder according to the data latched. Once the BCD data is latched, the respective segments are turned ON with the active low output of the decoder and the current flows continuously through the lighted segments.
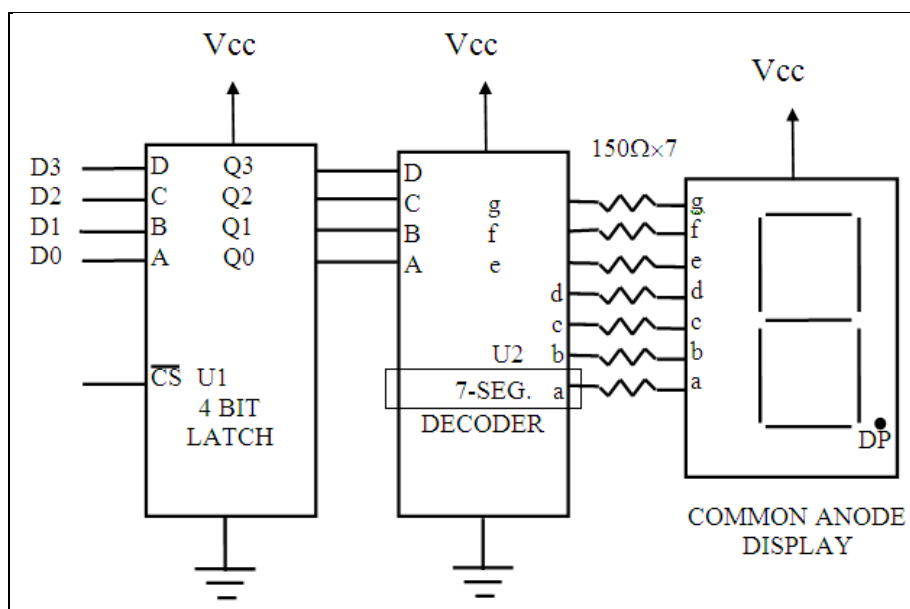

Fig. 3.5-9 Direct Driven Display with Latch/Decoder Driver

The 4-bit BCD data resides in 4-bit latch at the input of the decoder to be displayed. The data bits **D0-3** can be input to the 4-bit latch from a decade counter output or from

the Central Processing Unit **(CPU)**, restricted to input **D0-7** for the two digits at a time. The two 4-bit latches for the two digit display are refreshed any time new data is to be displayed. The Common Anodes of the LEDs are connected to the Vcc and the Cathodes are driven low by the decoder outputs to turn the respective LEDs ON for a particular digit to be lit. The display is drawing the worst case DC current when all segments are lit.

Ex. 3.5-1

A six digit direct driven 7-segment display with an additional decimal point, as shown in Fig. 3.5-9, has 100Ω current limiting resistors for TTL compatible driving circuitry. Determine the worst case DC current flowing through the display section. The worst case occurs when all the 7-segments plus the decimal point are lit. Allow 1.5V voltage drop (VD) across each LED segment to be lit and 4.7V TTL driver output (Vo).

SOLUTION

Total number of segments per digit = 7 segments + 1 Dec. Point = 8

IF = (Vo - VD)/R = (4.7 - 1.5)/100 = 32mA

Total current per digit = 32mA × 8 = 256mA

For a 6-digit LED display, driven directly, the worst case total current:

IF(total) = 256mA × 6 ≈ 1.5A.

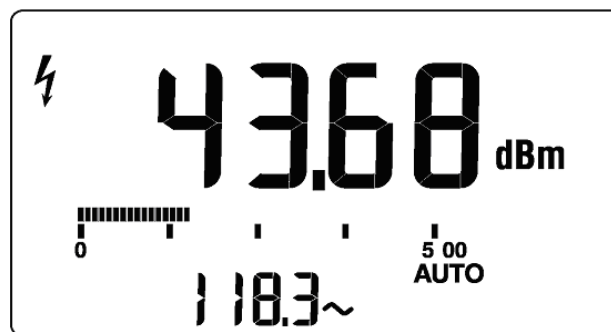A digital multimeter uses a Liquid Crystal Display (LCD), as shown in Fig. 3.5-10.

Fig. 3.5-10 Digital Multimeter LCD

An **MSI** BCD to 7-segment **0-9** decoder-driver circuit is used to operate these display devices by developing the seven output signals to drive the display segments. Table 3.5-2 shows the truth table for **74LS47** decoder circuit used to drive 7-segment LED displays. The BCD inputs **(DCBA)** are in the standard 8421 code format. The outputs are designated a, b, c, d, e, f, and g corresponding to the display elements. A binary 0 in the segment output columns indicates that the corresponding segment is illuminated, except segment **'g'** with binary 1 (not lit). A logic diagram for **74LS47** BCD to 7-segment decoder-driver is shown in Fig. 3.5-11(a). In addition to the four BCD inputs, this circuit also has a blanking input, a ripple blanking input and a lamp test input. When the active low lamp test input is at binary 0, all seven segments of the display are turned on in order to see that none has failed. The active low blanking input logic level blanks the whole display when all zeroes are displayed.
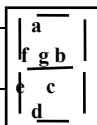
INPUTS					SEGMENT OUTPUTS							
DEC	D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	0	0	0	0	0	0	0	1	
1	0	0	0	1	1	0	0	1	1	1	1	
2	0	0	1	0	0	0	1	0	0	1	0	
3	0	0	1	1	0	0	0	0	1	1	0	
4	0	1	0	0	1	0	0	1	1	0	0	
5	0	1	0	1	0	1	0	0	1	0	0	
6	0	1	1	0	1	1	0	0	0	0	0	
7	0	1	1	1	0	0	0	1	1	1	1	
8	1	0	0	0	0	0	0	0	0	0	0	
9	1	0	0	1	0	0	0	1	1	0	0	

Table 3.5-2 Truth Table for 74LS47 BCD to 7-Segment Decoder

This feature is used where a number of displays are grouped to readout a multi-digit number. This feature blanks or suppresses all leading zeros automatically.

For example, in an 8-digit display without leading zero suppression, the number 1259 would be displayed as 00001259.

With leading zero suppression, only the desired digits 1259 will show to conserve power in LED displays.
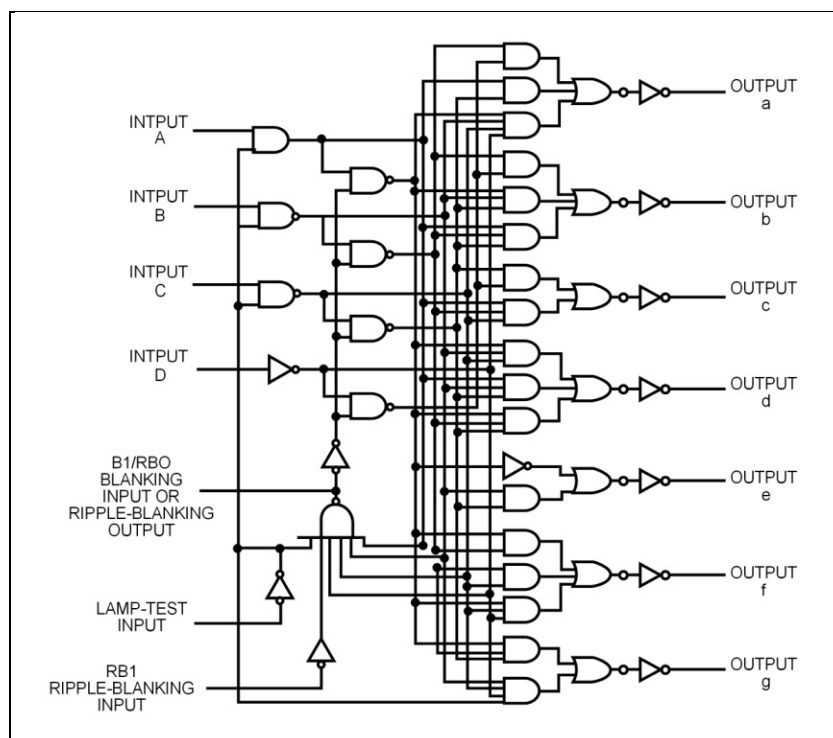
Fig. 3.5-11(a) 74LS47 BCD-to-Seven Segment 0-9 Decoder-Driver IC

The other four displays with leading 0000 will be automatically blanked. By applying a variable Duty Cycle (DC) pulse signal to the ripple blanking input, the intensity of the display can be varied without resorting to supply voltage or current controls. Fig. 3.5-11(b) shows the typical open collector output of the decoder-driver driving a LED display segment. When the output transistor goes into saturation, current flows from Vcc to ground through the LED in series with a current limiting resistor turning it on to be visible with light intensity as desired depending on the value of the resistor.
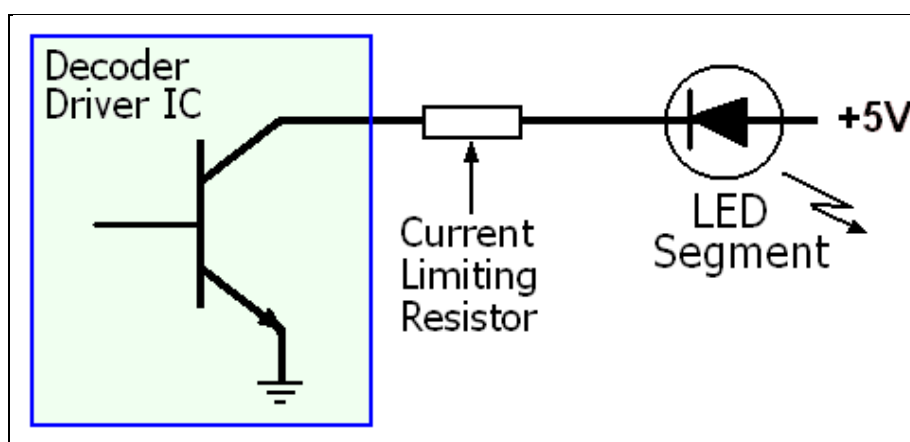

Fig. 3.5-11(b) 74LS47 Seven-Segment 0-9 Decoder Driver
Output Circuit driving LED Segment

Ex. 3.5-2

Verify the segments lit displaying digits 2 and 9 on a 7-segment display in Table 3.5-3.

SOLUTION

#	DISPLAY	SEGMENT LIT						
		g	f	e	d	c	b	a
2		1	0	1	1	0	1	1
9		1	1	0	0	1	1	1

Table 3-5 3-Segment Display

To display digit 9, the binary code 1001_2 is loaded and latched in the 4-bit latch.
The decoder decodes the number 9 into the segment code to be output to drive all other segments, except 'd' and 'e'.

DISADVANTAGES OF DIRECT DRIVEN DISPLAYS

1. **Continuous current** through the ON segments increases the burden on the power supply as the number of digits is increased.
2. **More number of ICs** are required as the number of digits are increased.
3. More **expensive power supply,** with higher current rating for larger displays, is required.
4. The **decoder output is limited** to 0 -9 numbers for 7-segment displays.

BCD TO 7-SEGMENT HEX-DECODER-DRIVER

Fig. 3.5-12(a) shows a simplified block diagram of the **9368** 7-segment **0-F** decoder/driver latch (Fairchild 9368). The 4-bit inputs are applied to the data inputs of latches that are enabled by the active low Latch Enable **(EL)** control line. The outputs of these four flip/flops are fed through a one-of-sixteen decoder. The decoder outputs drive an encoder circuit made up of OR-gates that generate the 7-segment codes necessary to display the digits 0 through 9 and hex-letters A through F. The output devices are current driver transistors that supply the segments currents. The Ripple Blanking circuitry consists of logic gates that are used to control a decoder circuit permitting leading 0 suppression.

The ripple blanking circuit effectively disables the gates in the decoder when the leading 0000 state is detected. This ensures that a leading 0 will not be displayed on 7-segment readout connected to the device.
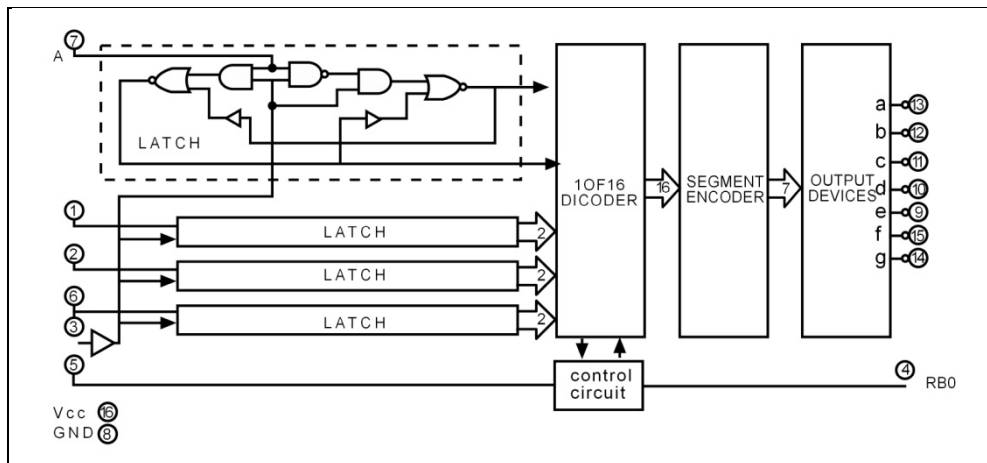

Fig. 3.5-12(a) Block Diagram of 9368 7-Segment 0-F Decoder-Driver IC

When we set **RBI** to the binary 0 state, we effectively produce zero-suppression. When the counter stepped to the 0000 state, the 7-segment display should be blank. If we replace BCD counter with a standard 4-bit binary counter, we will notice that the **9368** decoder-driver does recognize the six states normally considered invalid in the BCD code. In these six states, the decoder-driver causes the letters A, B, C, D, E, and F to be displayed on the 7-segment display where B(b) =11 is displayed in lower-case 'b', not to be confused with six (6) with 'a' segment ON. **Fig. 3-12(b)** shows Fairchild **9368** along with its functional equivalent Mororola-**MC14495** 7-Segment **0-F** decoder drivers' pin-out diagrams.
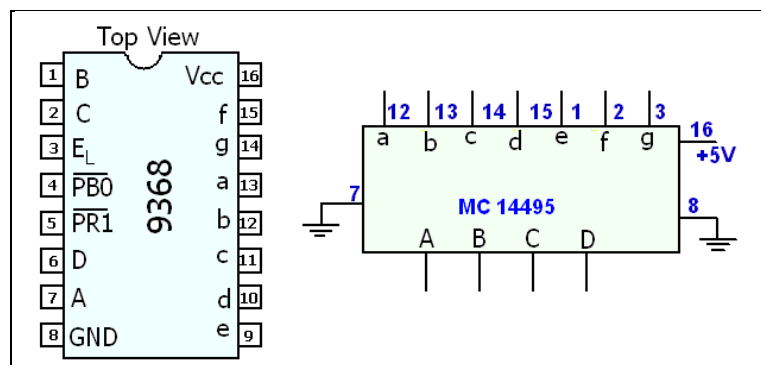

Fig. 3.5-12(b) 9368 Seven-Segment Hex-Decoder Driver (9368) Pin-Outs

ENCODERS

An encoder is a combinational logic circuit that accepts one or more inputs and generates a multi-bit binary output code. In a sense, encoders are exactly the opposite of decoders. Decoders detect or identify specific codes while encoders generate specific codes.

Figure 3.5-14 shows a simple encoder circuit. The inputs are three pushbuttons labeled 1, 2, and 3. The encoder circuit consists of two positive-NAND equivalent gates in negative OR gates forms. The outputs AB form a 2-bit binary code. When pushbutton 1 is depressed, the output of gate 2 goes high. At this time both inputs to gate 1 are high therefore, its output is low. By depressing button 1, the output code 01 is generated.

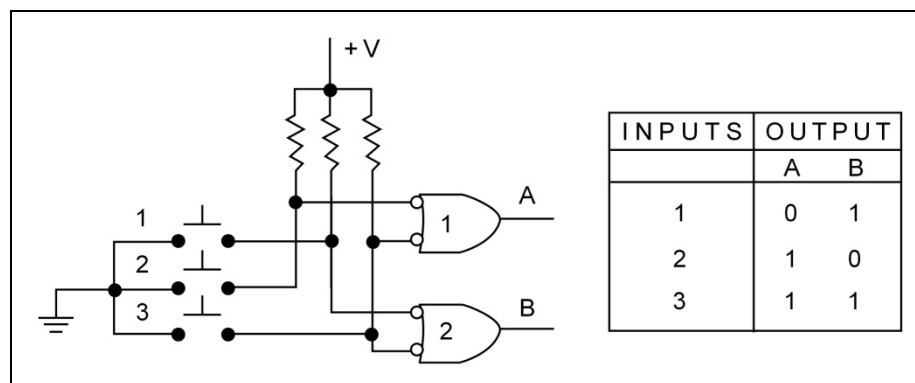| INPUTS	OUTPUT	
	A	B
1	0	1
2	1	0
3	1	1

Fig. 3.5-13

Depressing the number 2 pushbutton forces the output A of gate 1 high. The B-output of gate-2 is low therefore, the output code is 10. Depressing button 3 forces the outputs of both gates high generating the code 11. The binary code corresponding to the decimal number given to each input switch is generated when that switch is closed. The truth table in Figure 3.5-14 summarizes the operation of the circuit. When all of the switches are open (not depressed), the output code is 00.

A typical application for an encoder circuit is in translating a decimal keyboard input signal into a binary of BCD output code. Figure 3.5-14 shows a decimal to BCD encoder circuit. When anyone of the input lines is brought low, the corresponding 4 bit BCD output code is generated. For example, bringing the

number 5 input line low with a pushbutton forces the outputs of gates 1 and 3 high. Gates-2 and-4 have low outputs at this time. The output code on lines DCBA then is 0101 or the binary equivalent of the decimal number 5. This circuit, like all encoders, generates a unique output code for each individual input.
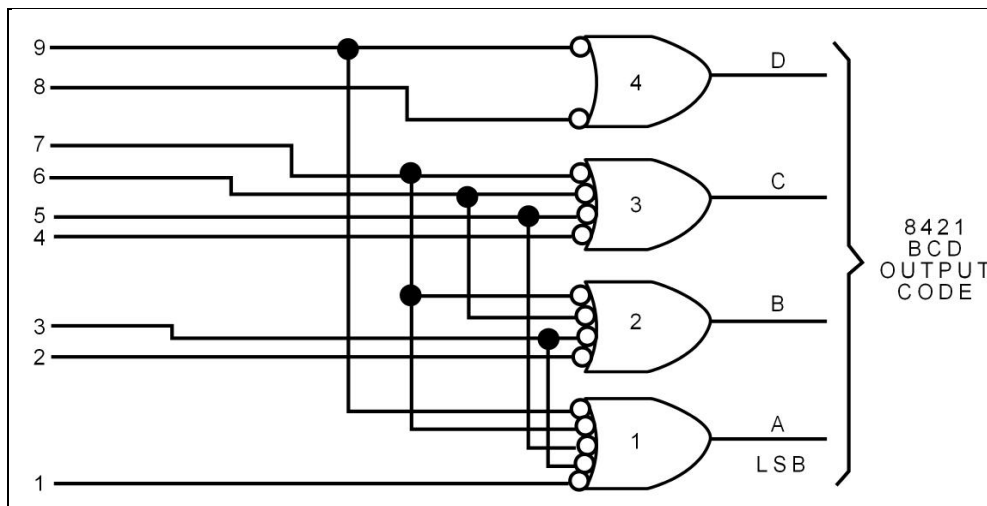

Fig. 3.5-14

SUMMARY

- The number of gates required in a decoder is equal to the total number of outputs possible, except in the one bit decoder.

- An AND gate can be used to detect the presence of any binary number, 00, 01, 10 or 11 using inverter(s) in series with the input(s) for low (0) logic to be detected.

- A NAND gates can be used to detect the presence of any binary number, 00, 01, 10 or 11 using inverter(s) in series for the input(s) with high (1) logic to be detected.

- If any one of the six **invalid** BCD codes above 1001 (9) is applied to the input of the 74LS42 BCD-Decimal decoder, all outputs will remain high.

- An octal decoder accepts a parallel 3-bit input code to decode any one of eight possible outputs 0-7.

- The **74LS154** 4-to-16 hex-decoder decodes any one of 2^4 (16) states represented by four bit input words 0000-1111 (0-15).

- A Common Anode display has all the Anode terminals shorted and Common Cathode display all the Cathode terminals shorted within the display.

- A Common Anode display is usually driven by open-collector output transistors of a decoder.

- A Common Cathode display is usually driven by emitter-follower output transistors of a decoder.

- An Encoder converts human interactive input such as alpha numeric keyboard into computer usable binary format.

GLOSSARY

LSB: Least Significant Bit

MSB: Most Significant Bit

LED: Light Emitting Diode

MSI: Medium Scale Integration

LCD: Liquid Crystal Display

DC: Duty Cycle

DP: Decimal Point

CPU: Central Processing Unit

VD: Voltage drop

RBI: Ripple Blanking Input

EL: Latch Enable

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

MPX/MUX: Multiplexer

WS: Word Select

FORMULAE

$2^n = N$ Where n = Number of bits at the input of a decoder

N = Number of output states in decimal

REVIEW EXERCISE

DECODERS/ENCODERS

1. The basic decoder circuit is a (n) _____ gate.

2. The maximum number of outputs from a decoder with a 5-bit input code is ____:

    $N = 2^n$

    a) 16   b) 8

    c) 4   d) 32

3. Draw a 1 of 4 decoder using 2-input positive NOR/negative AND gates. Assume that both normal and complement signals are available from two flip/flops A and B.

4. Only one output of a 7442 decoder is low while all others are high.

    a) True   b) False

5. An 8-digit direct-driven 7-segment LED display without decimal point, as shown in Fig. 3.5-9, has 150Ω current limiting resistors for TTL compatible driving circuitry. The worst case occurs when all the 7-segments are lit. Allowing 1.5V voltage drop (VD) across each LED segment and 4.7V TTL driver output (Vo), Determine:

    i) The individual segment current is, approximately, _____mA.

        a) 147   b) 21

        c) 31   d) 10

    ii) The total current per digit is, approximately, _____mA.

        a) 147   b) 21

        c) 31   d) 10

    iii) The worst case DC current flowing through the display is, approximately, _____A.

        a) 1.5   b) 2.1

        c) 3.1   d) 1.2A

6. Verify the segments lit displaying digits 3 and 7 on a 7-segment display in Table 3.5-3.

   SOLUTION

#	DISPLAY	SEGMENT LIT						
		g	f	e	d	c	b	a
3								
7								

   Table 3-5 7-Segment Display

7. A 7-segment display must use a _____ to drive the segments.

   a) Decoder   b) Latch

   c) Counter   d) Vcc

8. In Common Anode display, all the _____ are tied to Vcc side.

   a) Cathodes   b) Anodes

   c) Both of above   d) None of above

9. A Common Anode 7-segment display can be turned ON by applying a 0-logic to the proper cathodes.

   a) True   b) False

10. A 10-digit direct driven 7-segment display without an additional decimal point, as shown in Fig. 3.5-9, has 100 Ω current limiting resistors for TTL compatible driving circuitry. The worst case DC current per digit flowing through the display section, is _____ mA.   VD = 1.5V   Vo = 4.75V

   a) 32.5   b) 227.5

   c) 227.5   d) 250.0

TASK 3.5-1

DECODER

OBJECTIVE

Upon completion of this task, the trainees will be able to:

• Demonstrate the operation of a decoder.

TOOLS, MATERIALS & REQUIREMENTS

Heathkit Digital Design Experimenter ET-3200.

-1 - 74 LS00 IC **(443-728)**   -1 - 74LS04 IC **(443-755**)

-1- 74LS20 IC **(443-798)**   -1 - 74LS42 IC **(443-807)**

-   Personal safety equipment as recommended in digital electronic workshop.

PROCEDURE

1. Construct the decoder circuit shown in **Fig. 1-1**. The data switches (SW1-SW4) will provide the input. LED indicator (L4) is the output. Be sure to connect +5 volts and ground to pin 14 and pin 7 of the two ICs.
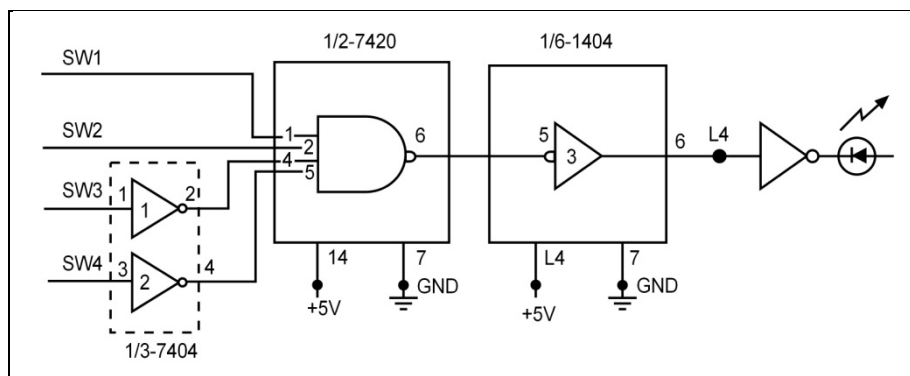

Fig. 1-1 Decoder Circuit for Steps 1 and 2

2. Apply the 16 states 0000 through 1111 to the circuit and observe the output. Record the binary input state where L4 lights. _____

    Assume SW4 is the LSB. **The decimal equivalent is: _____**

3. Construct the circuit shown in Fig. 1-2. Take your time in constructing this circuit to avoid wiring errors. The circuit inputs are applied through (SW3) and SW4 (LSB). You will observe the outputs on LED indicators (L1) through (L4).

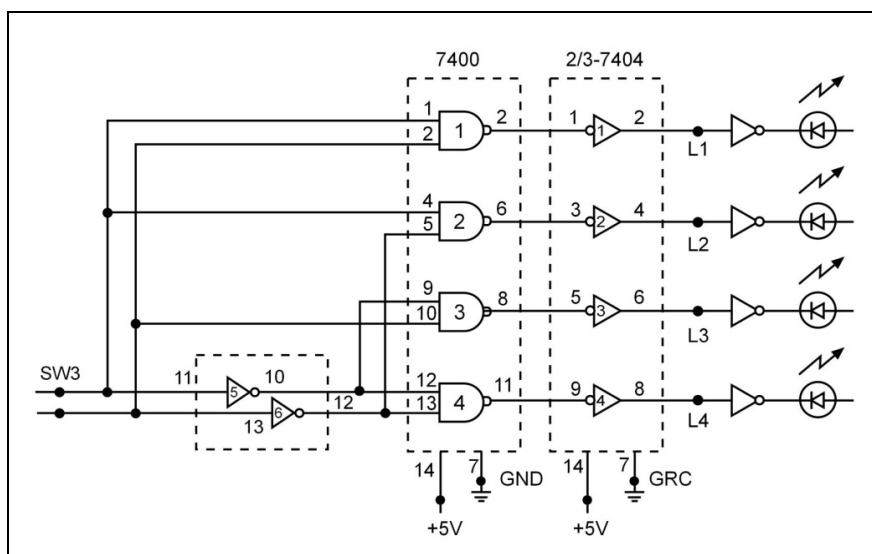   **What type of circuit is this? _____**

Fig. 1-2 2-4 Line Discrete Decoder

4. With SW3 and SW4, apply the inputs indicated in **Table 1-1**. Record the corresponding output states of L1, L2, L3, and L4 for each of input states.

INPUTS		OUTPUTS (STEP 4)				OUTPUTS (STEP 6)			
SW3	SW4	L1	L2	L3	L4	L1	L2	L3	L4
0	0								
0	1								
1	0								
1	1								

Table 1-1 Truth Table for 2-4 Line Decoder Circuit

Which of the following conditions did you observe for each set of inputs?

  a. All outputs low.   **b. All outputs high.**

  c. One output low.   **d. Two outputs high.**

  e. Two outputs low.   **f. One output high.**

5. Remove the connections between the outputs of inverters 1, 2, 3, and 4 and L1, L2, L3, and L4. Connect L1, L2, L3, and L4 to the outputs of the 74LS00 IC gates, pins 3, 6, 8, and 11 respectively.

6. Repeat **Step 4**. Apply the inputs in **Table 1-1** and record the output states in the appropriate places.

Which of the following output conditions did you observe for each set of inputs?

  a. All outputs low.   **b. All outputs high.**

  c. One output high.   **d. One output low.**

  e. Two outputs low.

7. Compare your results from **Step 4** and **6** by observing the data in **Table 1-1**. Then remove the circuit from the bread-boarding socket.

8. Mount a 74LS42 IC on the bread-boarding socket. Connect pin 16 to +5 volts and pin 8 to ground. Connect the inputs to switches SWl - SW4.

    Refer to **Fig. 1-3** and **1-4** for IC pin connections. You will monitor the outputs, one at a time with LED indicator L4.
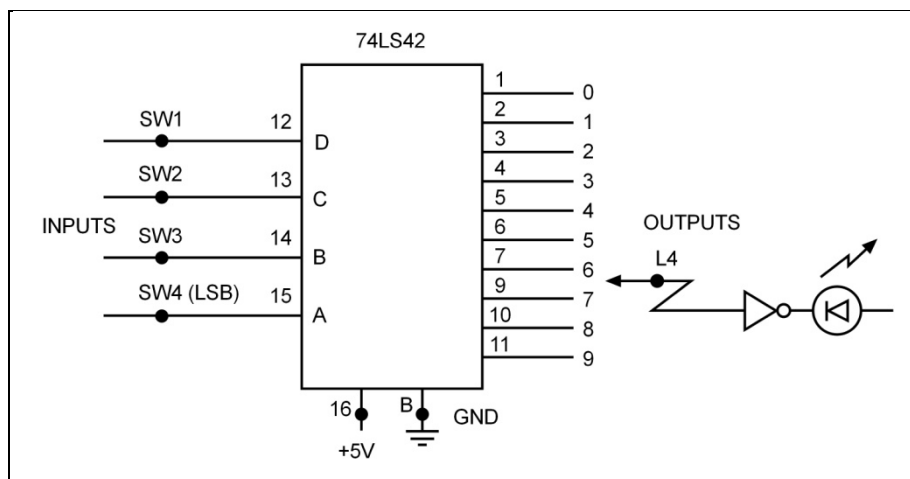

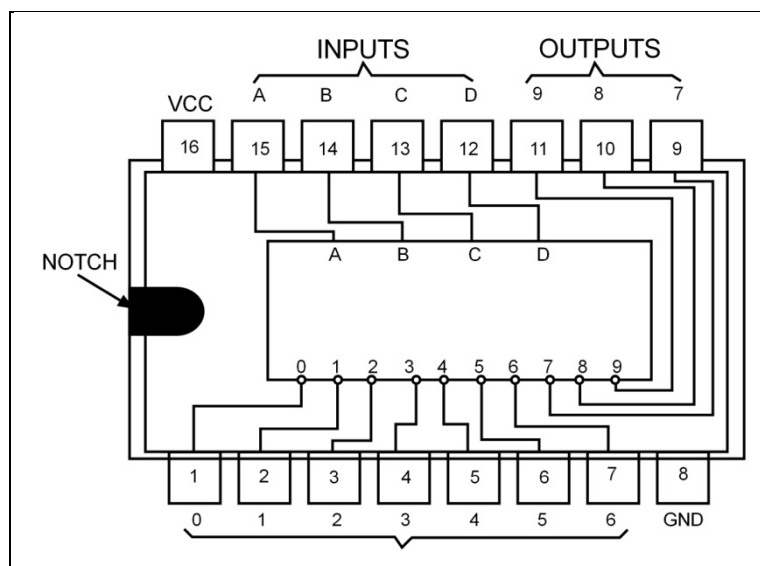Fig. 1-3 BCD Decoder Circuit for Steps 8 and 9

Fig. 1-4 Pin Connections for 74LS42

BCD to Decimal Decoder

9. Apply the inputs given in **Table 1-2**. The LSB (A) is SW4. Observe the 10 outputs, one at a time, with L4 by connecting it sequentially to pins 1, 2, 3, 4, 5, 6, 7, 9, 10, and 11. Record your outputs in Table 2.

   i) **The 74LS42 is a decimal decoder. What does this mean in terms of the outputs you observed?** _____

   ii) **The 74LS42 does not recognize the six states 1010 through 1111.**

      a) True   b) False

INPUTS				OUTPUTS									
D	**C**	**B**	**A**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
0	0	0	0										
0	0	0	1										
0	0	1	0										
0	0	1	1										
0	1	0	0										
0	1	0	1										

0	1	1	0										
0	1	1	1										
1	0	0	0										
1	0	0	1										
1	0	1	0										
1	0	1	1										
1	1	0	0										
1	1	0	1										
1	1	1	0										
1	1	1	1										

Table 1-2 Truth Table for 74LS42 Decoder Circuit

TASK 3.5-2

7-Segment Decoder-Driver and Display

OBJECTIVE

To demonstrate operation of 7-segment decoder-driver and LED display.

TOOLS, MATERIALS & EQUIPMENT

1-Heathkit Digital Design Experimenter (ET-3200)

1 - 74LS90A IC **(443-813)**   1 - 74LS193 IC **(443-815)**

1 - 9368 IC **(443-694)** or Equivalent.   1 - 7-segment LED display **(411-819)**

1 – 1K resistor

- Personal safety equipment as recommended in digital electronic workshop.

PROCEDURE

1. Construct the circuit shown in **Fig. 2-1**. This circuit consists of a 74LS90A BCD counter, a 9368/14495 BCD to 7-segment decoder-driver and a 7-segent LED display. The four BCD outputs of the 74LS90A counter drive the LED indicators L1 through L4 and the decoder-driver. The output of the decoder-driver is used to drive the 7-segment display. The pin connections to the 9368 decoder-driver and the 7-segment LED display are given in **Fig. 2-2**. As before use care in wiring the circuit to prevent wiring errors. Don't forget to connect +5 volts and ground to each IC. The 9368-IC is a 7-segment decoder-driver. It accepts the 4-bit BCD number from the 74LS90A BCD counter. The 9368-IC contains a 4-bit latch that can be used to store the four-bit input. The output of this latch is fed to the decoder circuit that converts the BCD input into the 7-segment output code described earlier. Driver transistors in the IC provide the current necessary to operate the 7-segments of the display. The 4-bit latch is loaded or enabled by the EL-input pin. This IC also contains a ripple blanking input line (RBI) to permit blanking of leading zeros.
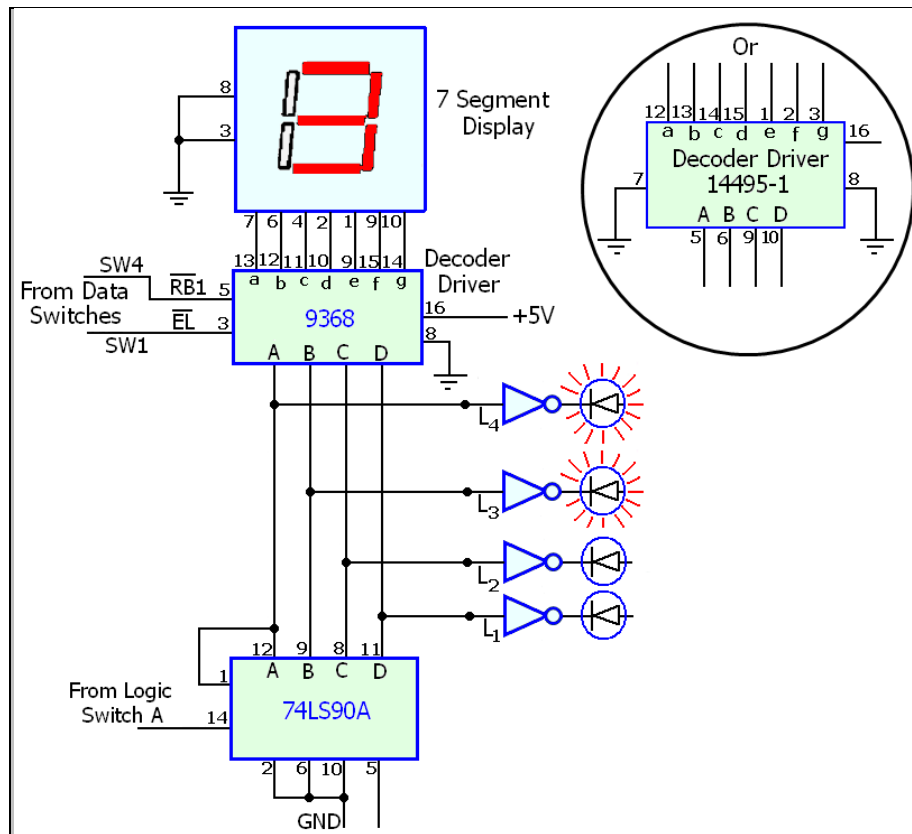
Fig. 2-1 7-Segment Decoder-Driver and Display Circuit

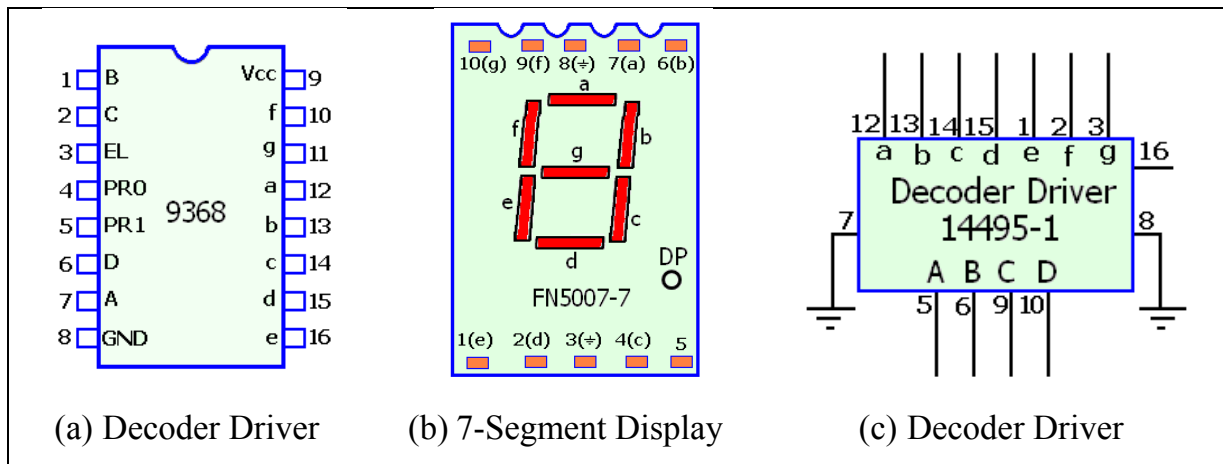(a) Decoder Driver   (b) 7-Segment Display   (c) Decoder Driver

Fig. 2-2(A) Pin Connections for 7-Segment IC Requirements

1. Apply power to the circuit. Set data switch (SW1) to binary 0 and SW4 to binary 1. Step the BCD counter with the A-logic switch. As you do, note the binary LED displays L1 through L4 and the 7-segment display. Check to see that the binary number shown is equivalent to the decimal number indicated. Step the counter through its ten states several times to see that the circuit is performing properly.

2. Remove the lead connecting pin-14 of the 74LS90A counter to the A-logic switch and connect it to the CLK-output. Set the clock frequency to 1 Hz. The clock will now automatically step the counter and permit you to observe both the BCD and decimal outputs of the circuit automatically.

3. When the decimal display reads 7, quickly set SW1 to the binary 1 position. Continue to observe LED indicators L1 through L4 and the 7-segment display and note your result.

4. Set (SWl) back in the binary 0 position. Observe the displays in circuit. Set SW4 to the binary 0 position. Continue to observe the displays and note any differences from the previous operation of the circuit. Specifically, observe the state of the 7-segment LED display when the counter reaches the 0000 state.

5. Modify your experimental circuit so that it appears, as shown in Fig. 2-3. Remove the 74LS90A-IC and in its place install the 74LS193-binary counter. You will continue to use the 1 Hz clock to step the counter. Data switch (SW2) will be used to reset the counter. Connect all unused outputs on IC74LS193 to 5V.
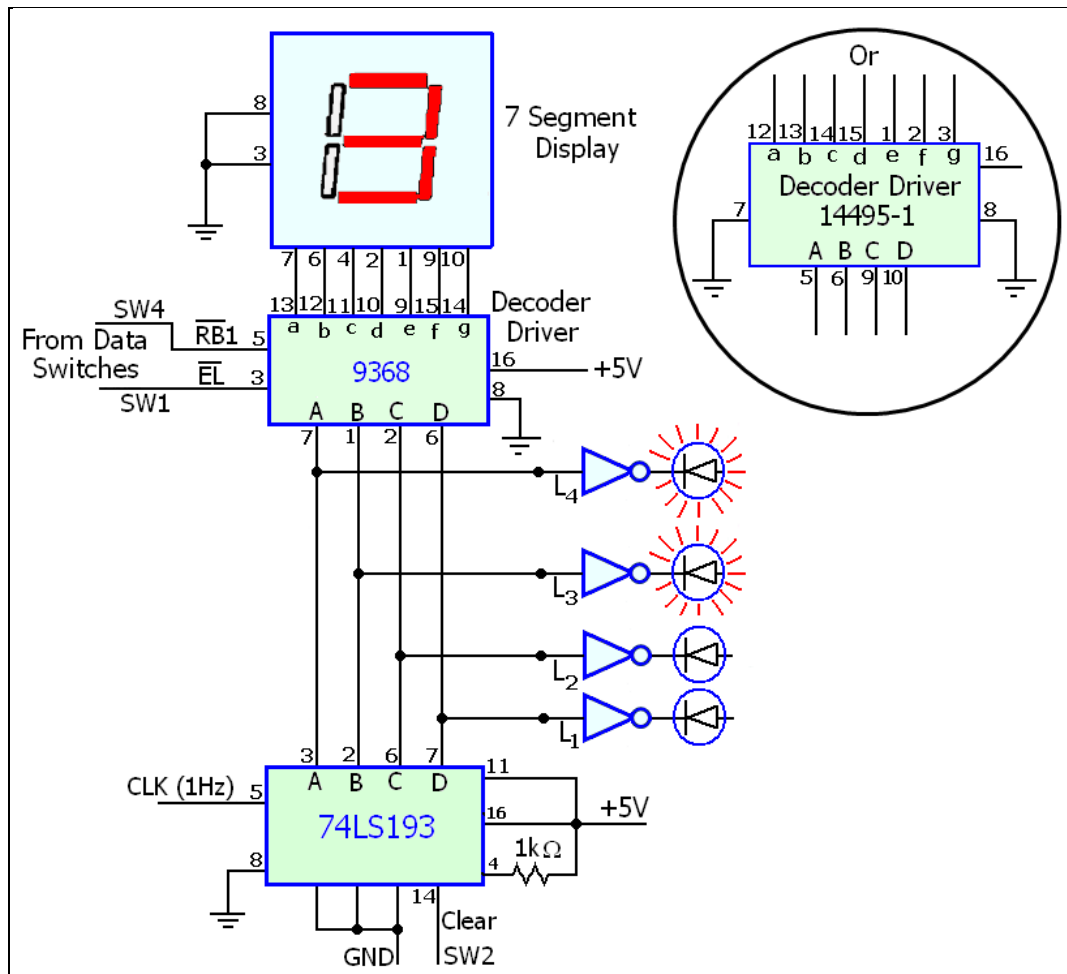
Fig. 2-3 Decoder-Driver Circuit using 74LS193-Counter for Steps 6 and 7

6. Set data switch (SW2) to the binary 0 position. Check to see that (SWl) is in the binary 0 position and SW4 is in the binary 1 position. As before, the counter should change states at 1 Hz rate as indicated by the LED indicators L1 through L4 and the 7-segment display. While you are observing the LED displays, note the status of the 7-segment readout during the 6 invalid codes for BCD operation.

Does the 9368-decoder-driver recognize the six 4-bit binary codes normally considered invalid in the BCD coding system? _____

If your answer to the question above is yes, record the characters displayed by the 7-segment readout during these six invalid states.
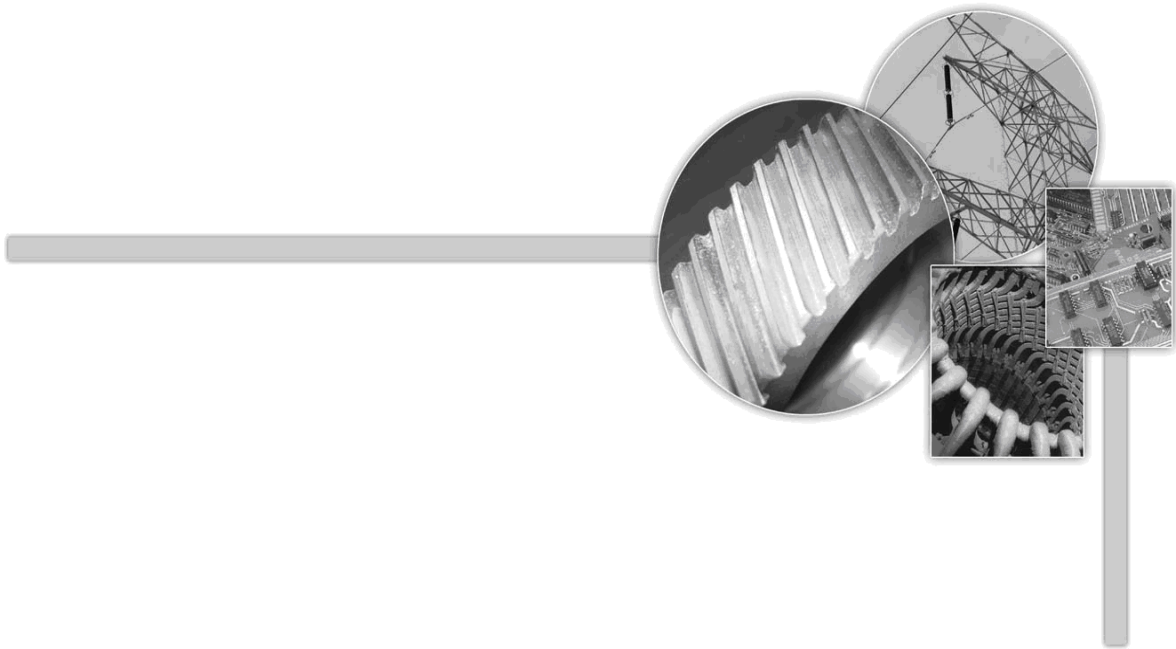
1010 _____

1011 _____

1100 _____

1101 _____

1110 _____

1111 _____

LESSON 3.6

MULTIPLEXER
& DEMULTIPLEXER

LESSON 3.6

MULTIPLEXER AND DEMULTIPLEXER

OVERVIEW

This lesson deals with the construction, operation and application of Multiplexers and De-Multiplexers. The trainees would learn how to implement, test, maintain and troubleshoot respective hardware circuits to understand their operation in digital applications.

OBJECTIVES

Upon completion of this lesson the trainee should be able to:

- Explain the function and operation of a Multiplexer.

- Describe the operation of a multiplexing display application.

- Describe the operation of a data multiplexing in communication application.

- Explain the function and operation of a De-Multiplexer and list an application.

Task 3-6-1: Multiplexer

Task 3-6-2: De-Multiplexer

MULTIPLEXERS

Another name for the multiplexer is Data Selector. A multiplexer is an electronic circuit that is used to select and route any one of a number of input signals to a single output. The simplest analogous form of a multiplexer is a single pole multi-position switch. Fig. 3.6-1 shows a rotary selector switch used as a multiplexer. Any one of six input signals can be connected to the common output line by simply adjusting the position of this mechanical selector switch. Mechanical selector switches are widely used for a variety of manual multiplexing operations in electronic circuits. However, many applications require the multiplexer to operate at high speeds and be automatically selectable. Multiplexers of this type can be readily constructed with electronic components. There are two basic types of electronic multiplexer circuits:

- **Analog Multiplexers**
- **Digital Multiplexers**

The simple manual selector switch multiplexer in Fig. 3.6-1 will work with either analog or digital signals. However, when electronic multiplexers are constructed, they are primarily designed for either analog or digital applications.

For analog applications, relays and bipolar or MOSFET switches are widely used.
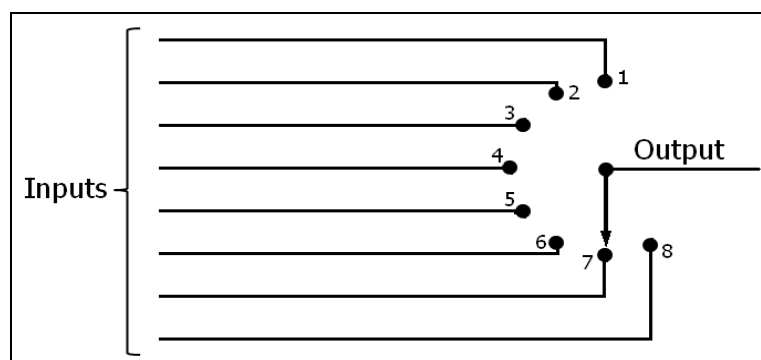

Fig. 3.6-1 Rotary Selector Switch as a Multiplexer

For digital applications involving binary signals, a multiplexer can be simply constructed with standard logic gates. Our primary concern here is the digital multiplexer or binary data selector.

2-INPUT MULTIPLEXER

The circuit in Fig. 3.6-2(a) is the simplest form of digital multiplexer. It has two input data sources and a single output. Either one of the input sources may be selected and fed to the output. The selection process takes place in AND Gates 1 and 2. The flip/flop controls these two gates to determine, which input is allowed to pass through OR Gate 3 to the output. When this flip-flop is set, the Q-output is high enabling Gate-1 when the $\overline{Q}$-output will be low inhibiting gate-2. Data source-1 is, therefore, be allowed to pass through Gate-1 and through the OR gate-3 to the output. Data source-2 will have no effect on the output state Resetting the flip/flop reverses this condition where Gate-1 will be inhibited by **Q** thereby preventing data source-1 from affecting the output. However, data source 2 will be allowed to pass through gates-2 and -3 to the output. This circuit is equivalent to a single pole double throw switch as indicated in Fig. 3.6-2(b).
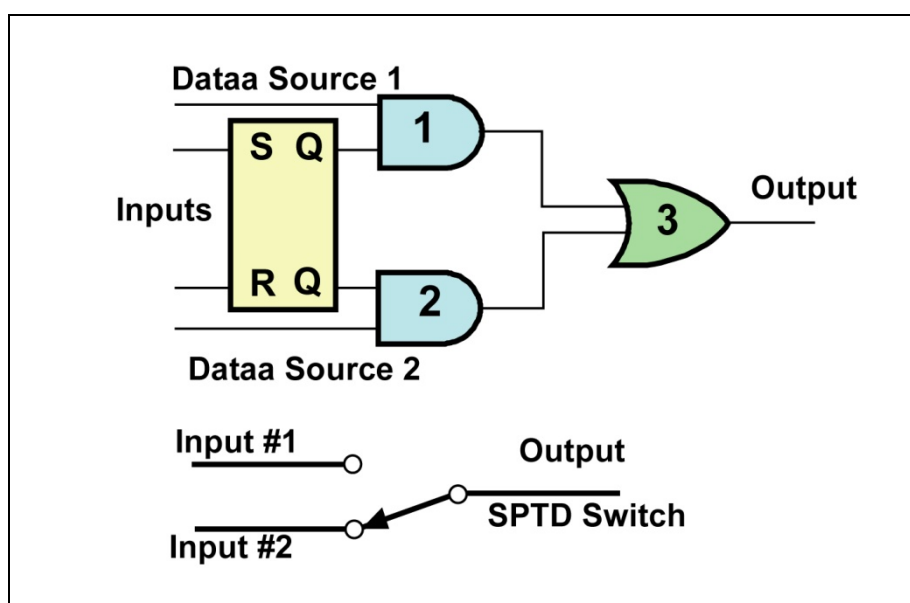

Fig. 3.6-2 (a) Two-Input Digital Multiplexer

(b) Mechanical Equivalent SPDT Switch

A **MSI** functional circuit using this basic 2-input multiplexer is shown in Fig. 3.6-3. Four 2-input multiplexers are combined to form a multiplexer for two 4-bit words. Word-1 has bits A_l, B_l , C_l and Dl where Word-2 has bits A_2, B_2, C_2 and D_2 and Enable **(E)** input controlling the circuit. If Enable is high, the output of inverter-15 is low inhibiting all of the AND gates and thus preventing either input word from appearing at the outputs. With Enable **(E)** low, the circuit is enabled.
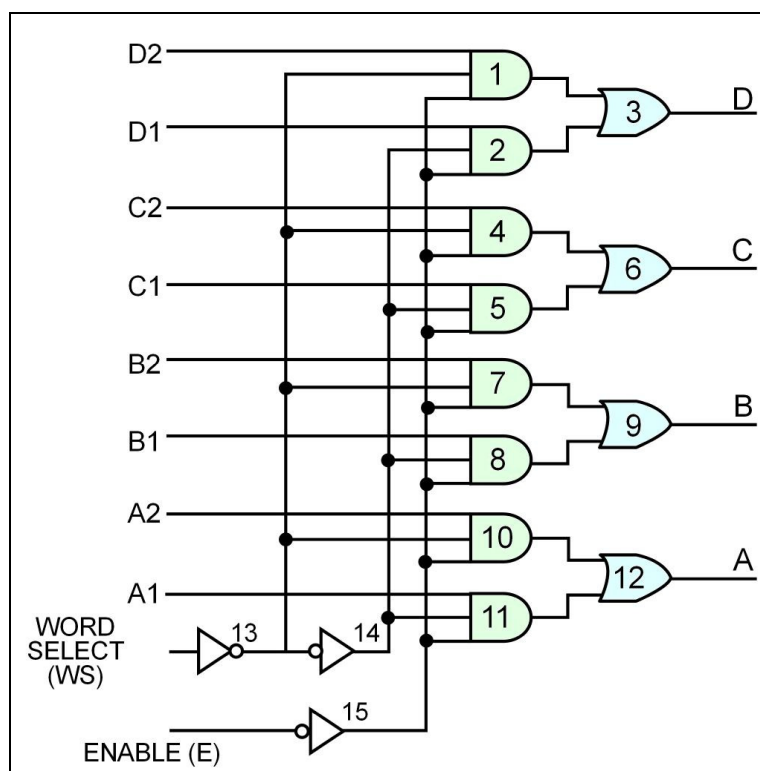

Fig. 3.6-3 Quad 2-Input Multiplexer

The Word Select **(WS)** input specifies, which four bit input word appears at the output. When the select input is high, gates 2, 5, 8 and 11 are enabled, letting input word-1 appear at the output. If the **WS** input is low**,** gates 1, 4, 7 and 10 are enabled permitting word-2 to appear at the output.

4-INPUT MULTIPLEXER

A 4-input multiplexer circuit is shown in Fig. 3.6-4 where each input is applied to a NAND gate that is enabled or inhibited by a 1-of-4 decoder. The outputs of the

NAND gates are ORed together at Gate-5. Only one of the four inputs will be enabled and the selection of the input is made by the decoder circuit to pass through to the output. A 2-bit binary word AB is applied to the decoder and the decoder recognizes one of the four possible input codes and enabling the appropriate gate. When the two-bit input word is 00, the AB output line is high. This enables Gate-1 and input-1 is allowed to pass through to the output.

Input code 01 enables Gate-2, input code-10 enables Gate-3 and input code-11 enables Gate-4.

The simplest way to implement the 4 bit multiplexer is to combine both the decode and enable functions in the same MSI package, as shown in Fig. 3.6-4.
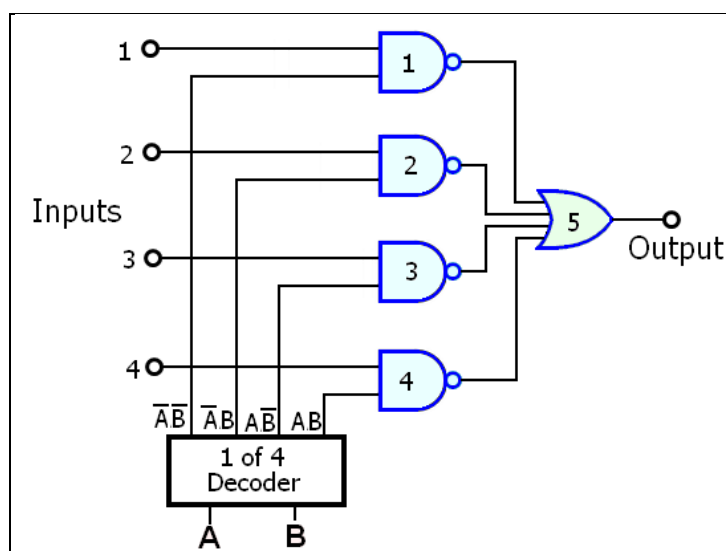

Fig. 3.6-4 4-Input Multiplexer

Additional inputs have been added to the input gates so that they also perform the decoding functions. The normal and complement outputs from the 2-bit binary input word-AB are applied to the enable-gates similar to the decoder gates.
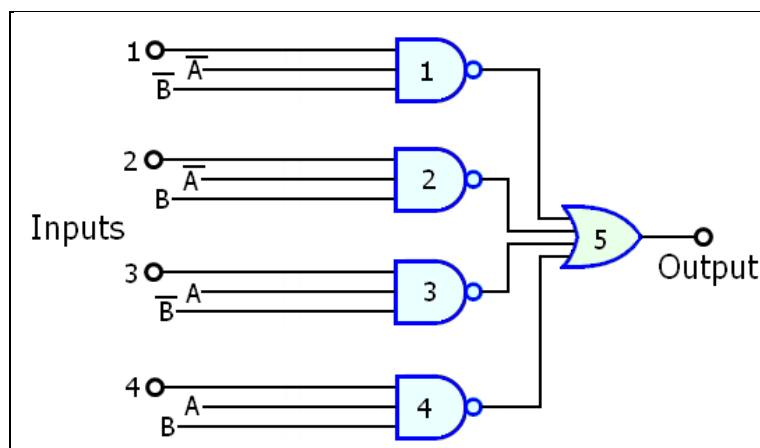
Fig. 3.6-5 4-Input Multiplexer with combined Decode-and-Enable Functions

If the binary input code-00 is applied, the $\overline{A}$ and $\overline{B}$-lines will be high to enable Gate 1 and input 1 will pass through Gate-1 and Gate-5 to the output when Gates-2,3 and 4 will be inhibited.

8-INPUT MULTIPLEXER

An 8-input TTL binary multiplexer is shown in Fig. 3.6-6 where Gates 1-8 enable or inhibit the eight data-input lines **D0-D7**. A 3-bit binary input word **(ABC)** enables one of the eight gates depending upon the input code.

The six inverters at the data select inputs generate the normal and complement signals needed by the select gates.

The 3-input word is an address code that designates, which data input line is selected.

If the binary input is 101, data input-**D5** is selected.

The strobe enable line enables or inhibits all eight select gates.

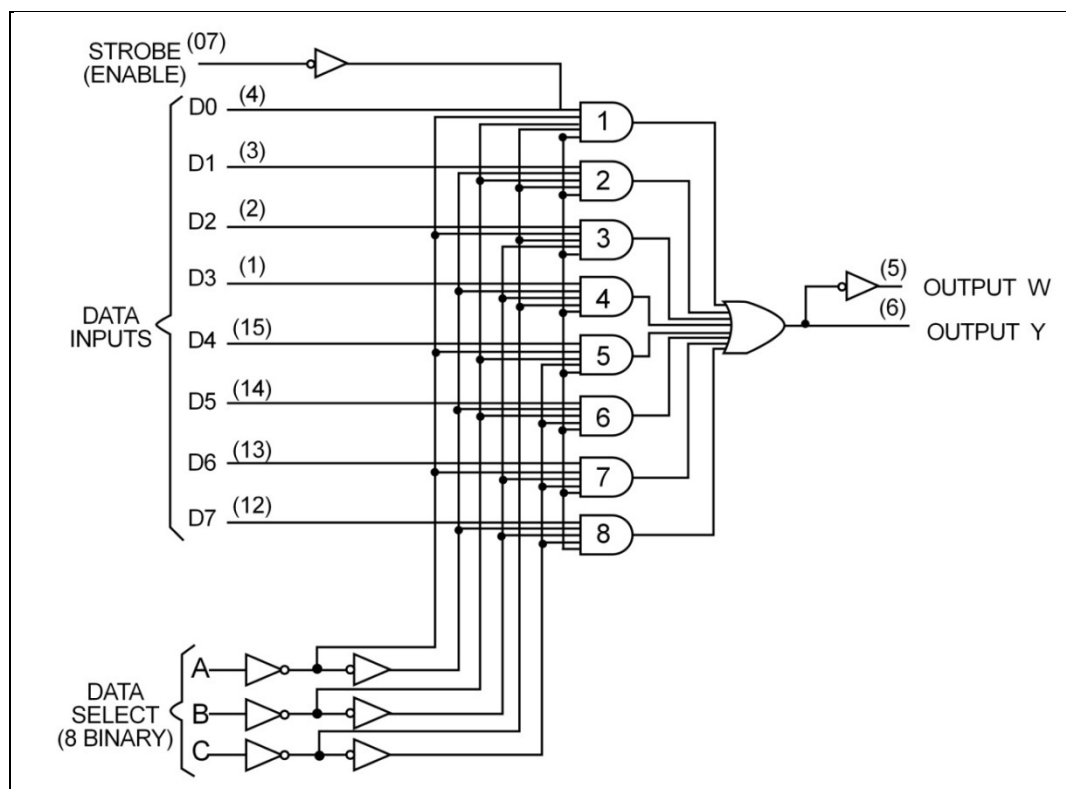Both the normal (W) and complement (Y) output signals are available.

Fig. 3.6-6 8-Input Multiplexer (74LS151)

MULTIPLEXER APPLICATIONS

Besides providing a convenient means of selecting one of several inputs to be connected to its single output, a multiplexer has several special applications.

Besides its data selector application, multiplexer is also used to provide parallel-to-serial data conversion, serial pattern generation and Boolean functions.

PARALLEL-TO-SERIAL CONVERSION

A multiplexer is often abbreviated as MPX or MUX. A 4-input parallel binary word is applied to the inputs of a multiplexer.

The output of the multiplexer becomes a serial representation of the parallel input word by sequencing through the input enabling codes. A 2-bit binary input word AB from a counter is used to select the desired input .The input word **WXYZ** is stored in a 4 bit storage register where the output of each flip/flop in the register is connected to one input of the multiplexer.

As the 2-bit counter is incremented, the AB-input select code is sequenced through its four states 00 through 11.

The-output **(M)** of the multiplexer is equal to the state of the flip/flop connected to the enabled input as illustrated in Fig. 3.6-7 Table 3.6-5 for the multiplexer truth table.

By sequencing through the 4 input states at a fixed rate, the parallel input word is converted to a serial output word.

When the AB input is 00, the state of the W flip/flop appears at the output.

When the AB input state is 01, the state of the X flip-flop appears at the output.

Similarly, input select states 10 and 11 cause the states of Y and Z flip/flops, respectively, to appear at the multiplexer output.

Depending upon how the inputs are connected to the register, the multiplexer can cause either the LSB or the MSB to occur first.
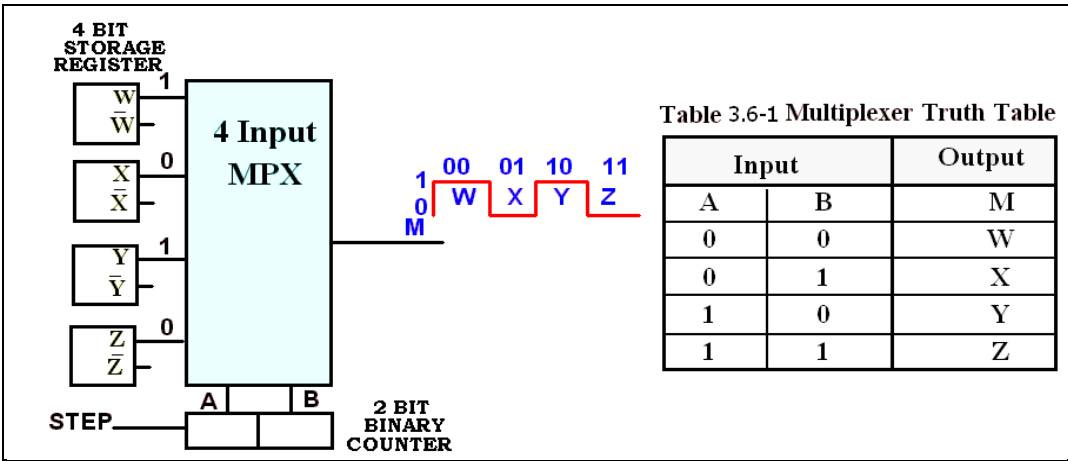

Fig. 3.6-7. 4-Input Multiplexer used in Parallel-to-Serial Converter

SERIAL BINARY WORD GENERATOR

Another application of the multiplexer in digital circuits is the generation of a serial binary word. Fig. 3.6-8 shows an 8-input multiplexer used to generate a fixed serial binary output word. By sequencing through the 3-bit input words from 000 through 111 with a binary counter, the binary states applied to inputs 0-7 are sequentially connected to the output. The binary word 10011010 is generated at the output.

Again, depending upon the application, the connections to the multiplexer input can be made such that either the MSB or LSB occurs at the output first. In this case the MSB appears at the output first as illustrated in Fig. 3.6-8 Table 3.6-6 for the multiplexer truth table.
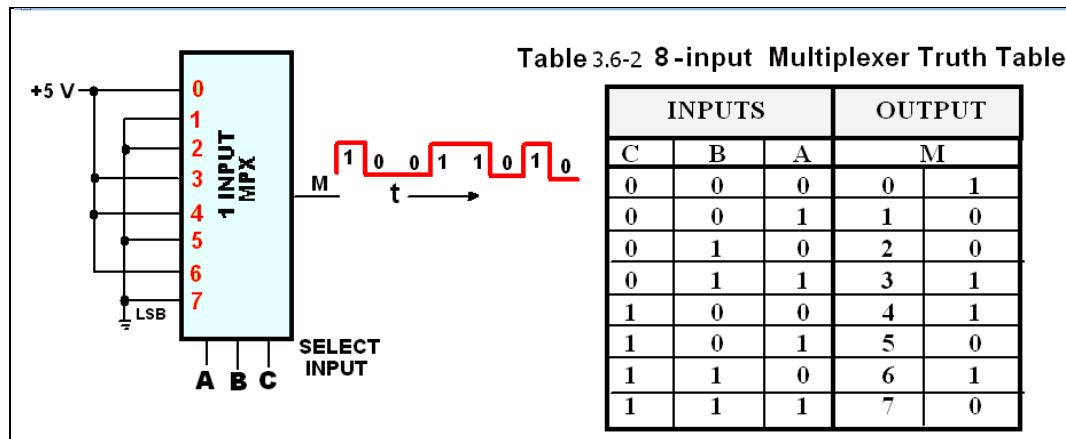

Fig. 3.6-8 8-Input Multiplexer used to generate Serial Binary Word

DE-MULTIPLEXER

The de-multiplexer is also known as a data distributor or data router. A de-multiplexer is a logic circuit that is basically the reverse of a multiplexer. Where the multiplexer has multiple inputs and a single output, the de-multiplexer has a single input and multiple outputs. The input can be connected to any one of the multiple outputs.

TWO-OUTPUT DE-MULTIPLEXER

A simple two output de-multiplexer circuit is shown in Fig. 3.6-9. The single input is applied to both AND gates-1 and-2 where a flip/flop selects one or the other gate to be enabled. When the A Flip/flop is set, Gate-1 is enabled by its Q-output and Gate-2 is inhibited by its $\overline{Q}$-output. The input, therefore, will pass through Gate-1 and finally the input appears at output 1.
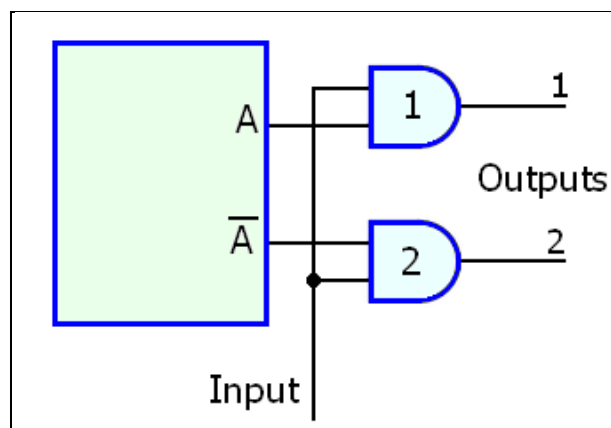
Fig. 3.6-9 2-Output De-multiplexer

4-OUTPUT DATA DE-MULTIPLEXER/DISTRIBUTOR

A 4-output data distributor used in a serial-to-parallel converter is shown in Fig. 3.6-10(a) where the single input is applied to four gates, simultaneously. As in the multiplexer, additional inputs on the select gates are used for decoding. A 2-bit word AB from a counter is used to select which gate is enabled. If the 2-input binary word AB is 11, Gate-4 is enabled and the input will pass through Gate 4 while the other three gates are inhibited. A 4-bit serial word is applied to the input.

As the input bits occur, the 2-bit counter is incremented enabling the gates in the distributor one at a time, sequentially, from top to bottom. The step input to the 2-bit counter is in synchronism with the occurrence of the bits in the serial word. The latch/storage register with flip/flops (WXYZ) is initially reset prior to the application of the serial input. The flip-flops in the storage register are connected to the output of the data distributor and are sequentially set or left reset as the serial word occurs.
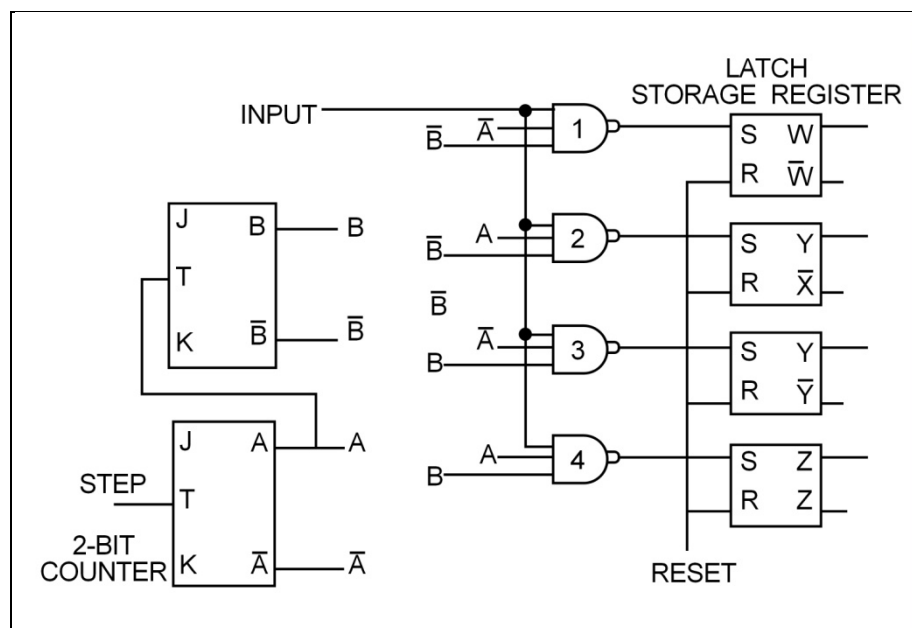
Fig. 3.6-10(a) 4-Output De-Multiplexer in Serial-to-Parallel Converter

Once each of the four gates has been enabled in sequence, the register contains the serial input word. Its outputs can then be observed, simultaneously and the serial input word has been converted to a parallel output word. Fig. 3.6-10(b) shows the waveforms of the circuit in Fig. 3.6-10(a). The input is the serial number 1101 and the waveforms show the outputs of Gates 1-4 and the flip-flop outputs WXYZ.

The first bit of the serial input is a binary 1 and it occurs during the $\bar{A}\,\bar{B}$ input sequence. During this time Gate 1 is enabled and its output goes low setting the W latch so that the W-output is high. The $A\,\bar{B}$-input selection sequence is next. Note that this is synchronized with the next input, which is also a binary 1. This input state causes Gate-2 to be enabled and its output goes low, thereby setting the X-flip/flop so that the X output is high.

During the next input selection sequence $\bar{A}B$, the serial input word is 0. Gate-3 is enabled so that output of Gate-3 remains high. This has no effect on the Y flip-flop so it remains reset. The AB-input selection sequence is next. It occurs in synchronism with the next serial bit, which is a binary-1. Gate-4 is enabled and its output is low setting the Z-flip/flop and causing its output to go high. Looking at the states of the flip/flops after the fourth serial input bit has occurred, the parallel output-1101 is available. Note that all of the reset inputs to the latch flip/flops in the storage register

are connected together to form a common reset line. Prior to the application of the serial input, a low signal is applied to the reset input to clear the register to 0000-state.
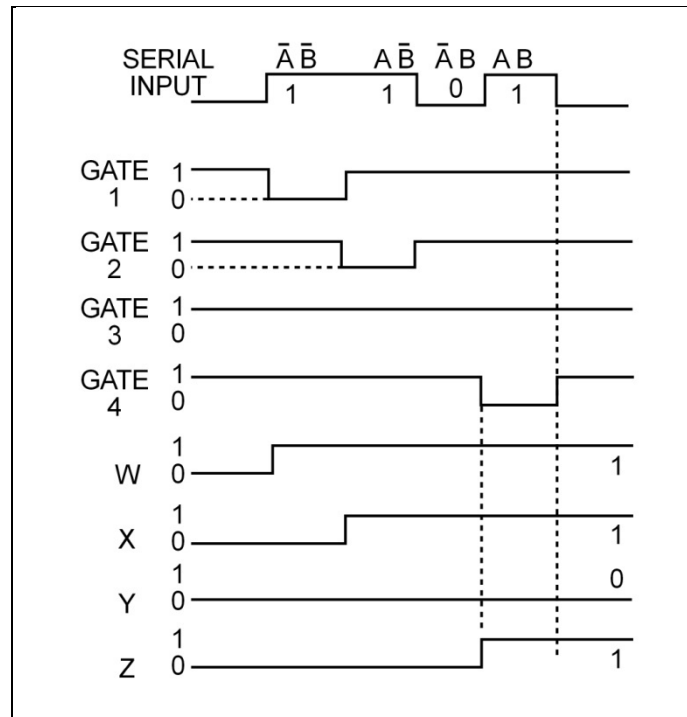

Fig. 3.6-10(b) De-Multiplexer Waveforms in Serial-to-Parallel Converter

The data distributor circuit in Fig. 3.6-10(b) shows that it is essentially a decoder where the decoded gates all have a common input. Because of this particular configuration, a standard MSI decoder circuit can often be used as a data distributor. Fig. 3.6-11 shows how a 7442 BCD to decimal decoder can be used as an 8-output data distributor. When this circuit is used as a data distributor, inputs-A, B, and C are used to select the desired output. These three inputs will enable one of the Gates 1-8. The data input is applied to the D-input of the circuit. Note that data input is inverted by inverter 17 and then applied to Gates 1-8.

The data input will appear at the output of the gate selected by the three bit input word ABC. For example, if the input state is 000, Gate 1 is enabled when the data applied to the D-input appears at the output of Gate-1. In this application Gates-9 and 10 of the decoder are not used.
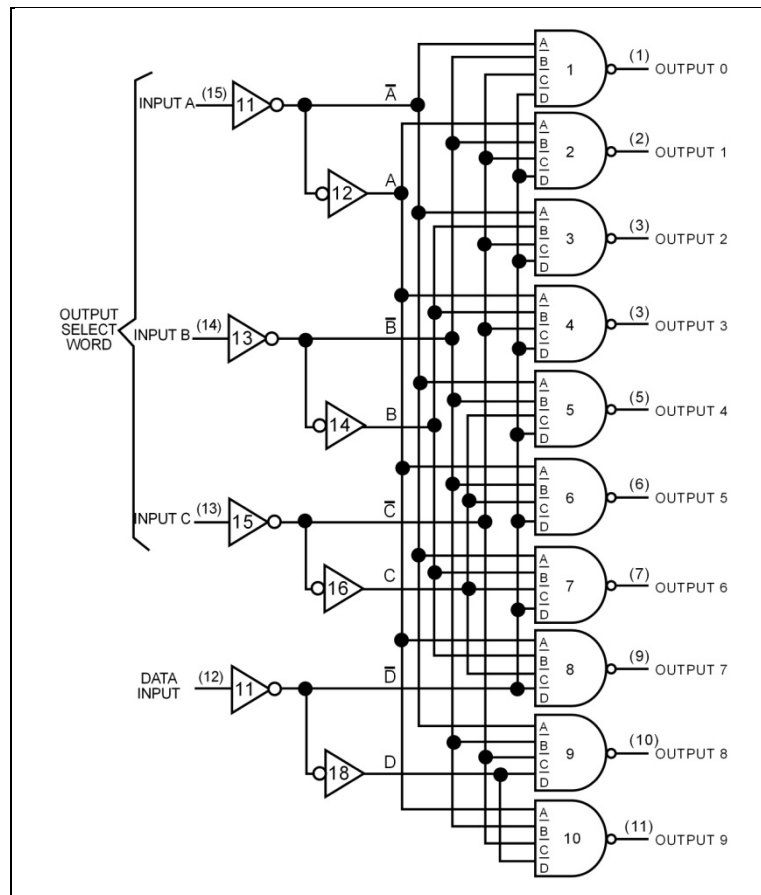
Fig. 3.6-11 7442 Decoder used as 8-Output Data Distributor

SUMMARY

- A multiplexer is a device that select one input among multiple inputs.

- There are two types of multiplexers analog and digital multiplexer.

- The de-multiplexer is a data distributor or data router.

- The de-multiplexer is used to produce data to multiple addresses.

REVIEW EXERCISE

MULTIPLEXER

1. Which of the following definitions best describes a digital multiplexer?

    a) A circuit, which can route a single input to one of several outputs.

    b) A circuit that recognizes a specific input code.

    c) A circuit that connects one of several inputs to any of several outputs.

    d) A circuit that connects one of several inputs to a single output.

2. List two applications of a multiplexer:

    a)   b)

DE-MULTIPLEXER

1. Another name for a De-Multiplexer is _____

2. A typical application of a De-Multiplexer is _____

3. In Fig. 3.6-11 input code (DCBA) _____ must be applied to connect the input to the output of Gate-6.

    a) 0101   b) 1010

    c) 1101   d) 1110

TASK 3.6-1

MULTIPLEXERS

OBJECTIVE

Upon completion of this task, the trainees will be able to:

• Demonstrate the operation and application of digital Multiplexers.

TOOLS, MATERIAL & REQUIREMENTS

Heathkit Digital Design Experimenter (ET-3200)

1 - 74LS00 IC (443-728)   1 - 74LS151 IC (443-878)

1 - 74LS193 IC (443-815)   1 - 1 k Ω resistor

- Personal safety equipment as recommended in digital electronic workshop.

PROCEDURE

1. Construct the circuit shown in Fig. 1-1. Use a 74LS00 IC, and be sure to connect +5 volts and ground to pins 14 and 7 respectively.

   Study the circuit in Fig. 1-1 and answer the questions below.

   a. What type of circuit is this? _____

   b. The two signal sources are: _____ and _____
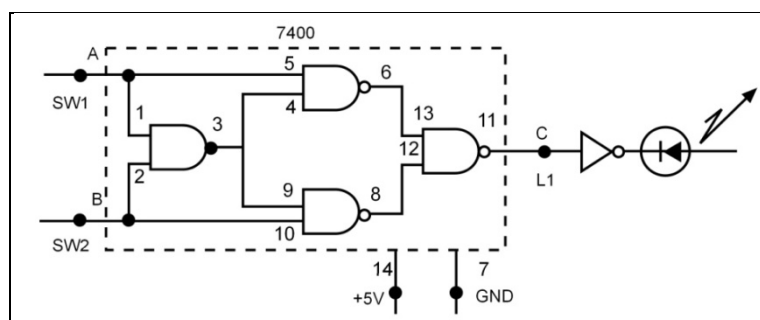
   c. The control input is: _____

Fig. 1-1 Multiplexer Circuit for Steps-1and -2

2. Apply power to the circuit. Set SW1 to the binary-1 position and note the circuit output on LED indicator L1. Note the effect of switching SW4 off then on.

   The output is: _____

   Set SWl to the binary 0 position. Note the effect of switching SW4 off and on.

   The output is: _____

3. Construct the circuit shown in Fig. 1-2. This circuit uses an 8-input data selector 74LS151. The desired input is selected by a 3-bit code ABC that is derived from a 75LS193 binary counter. This 3-bit code is monitored on LED indicators L2 through L4. The counter is stepped manually by logic switch A.

   The inputs to the data selector or multiplexer are derived from data switches SWl through SW4. The data selector output will be monitored on LED indicator Ll. The pin connections for the 74 LS151 data selector are given in Fig. 1-3. The logic diagram for this circuit is shown in Fig. 1-4.

4. Refer to Fig. 1-4. Write the Boolean output equation for the multiplexer circuit shown. Doing this will help you to understand what the circuit does.

   Y = _____

Fig. 1-3 Pin Connections for 74LS151
Multiplexer

Fig. 1-2 Multiplexer Circuit for Steps 3-6
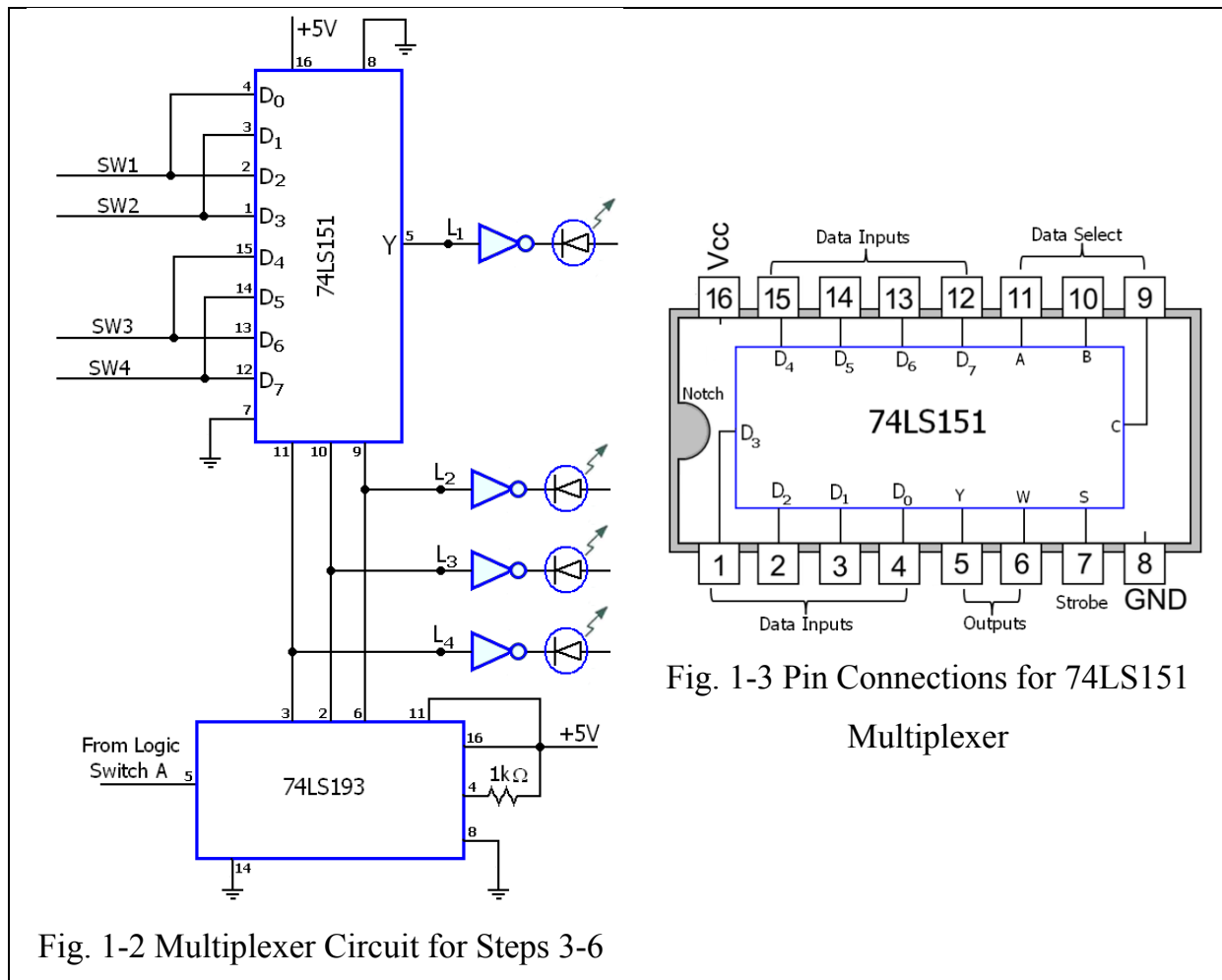
5. Apply power to your experimental circuit. Step the binary counter with the A logic switch until the L2, L3, L4, states are 000. Observing the experimental circuit diagram in Fig. 1-2 and the data selector logic diagram in Fig. 1-4, determine which input on the 74LS151 is enabled with this binary code. Then operate each of the data switches SW1 through SW4 and determine which one affects the data selector output. Record this information in Table 1-1.

Increment the binary counter with logic switch A so that the LED indicators L2 through L4 read 001. Again, determine which input (D0 through D7) of the 74LS151 multiplexer is enabled. Confirm this by actuating SW1 through SW4 until you determine which switch causes a change in the output on indicator Ll. Record this information in Table 1-1. Continue incrementing the counter for all eight states and completing the table as indicated.

Fig. 1-4 Logic Diagram of 74LS151 Multiplexer
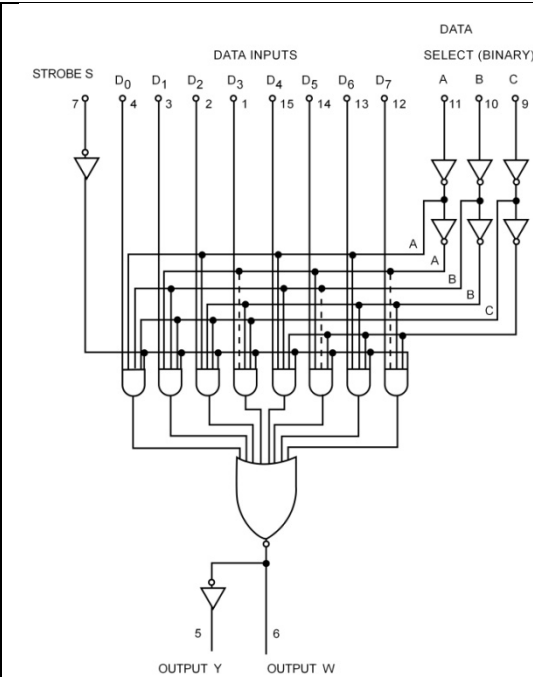
INPUT CODE			MPX INPUT	DATA SOURCE
C	B	A		
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Table 1-1 Truth Table for Multiplexer

6. Modify your experimental circuit to conform to Fig. 1-5. Remove the connections from the multiplexer inputs to data switches-SWl through-SW4. Wire the inputs of the multiplexer, as shown in Fig. 1-5. Connected in this way, the multiplexer becomes a serial data word generator or a Boolean function generator.
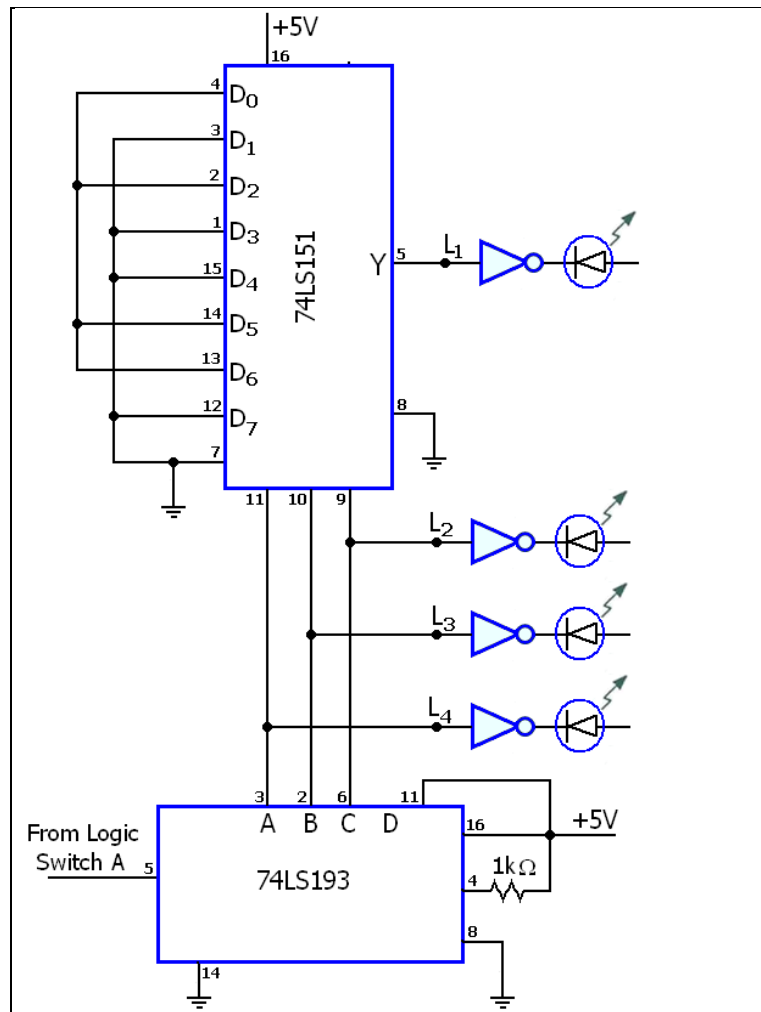
Fig. 1-5 Multiplexer Circuit for Steps 6-10

7. Apply power to the circuit. Step the counter with the A-logic switch until it is in the 000 state as indicated by LED's L2 through L4. At this time observe the multiplexer output on LED indicator LI. This is the first bit of an 8-bit word to be generated by the 74LS151 multiplexer. The state you are observing at this time is the LSB of the eight-bit word.

Next, step the counter with the A logic switch. At each counter state, note the multiplexer output by observing Ll. Increment the counter until the last bit of the word (counter state-111) is obtained. Record the binary word developed and its equivalent decimal value in the spaces provided below.

Serial output binary word = _____

Decimal equivalent = _____

8. Without changing the experimental circuit, assume that it is being used as a Boolean function generator. Step the counter through its eight states and again note the Ll-output condition for each of the counter states. Use this data to complete the truth table shown in Table 1-2.

INPUTS			OUTPUT Y
C	B	A	
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Table 1-2 Truth Table for Multiplexer

9. Using the procedure you learned in a previous section, write the Boolean equation (sum-of-products) from the truth table in Table 1-2. Record your Boolean equation below.

Y = _____

10. Observing the experimental circuit in Fig. 1-5 and using the multiplexer logic diagram in Fig. 1-4 for reference, write the output equation for the multiplexer. Note the states of the multiplexer inputs, then combining this information with the Boolean equation for the multiplexer you developed earlier, you should be able to write the sum-of-products expression of the output-Y for the multiplexer input connections.

Y = _____

Compare the equation developed here with the equation you produced from the truth table in the previous step.

TASK 3-6-2

DE-MULTIPLEXERS

OBJECTIVE

Upon completion of this task, the trainees will be able to:

- Demonstrate the operation of de-multiplexer.

TOOLS, MATERIALS & REQUIREMENTS

Heathkit Digital Design Experimenter (ET-3200)

1 - 74LS00 IC **(443-728)**   1 - 74LS86 IC **(443-891)**

1 - CD4001 IC **(443-695)**

- Personal safety equipment as recommended in digital electronic workshop.

PROCEDURE

1. Wire the circuit shown in Fig. 2-1. You will use a type 74LS00-IC. The inputs-A and B to the circuit are applied through data switches-SW1 and -SW2. The output C will appear on LED Ll-indicator. Be sure to connect +5 volts to pin 14 and ground to pin 7 on the IC.
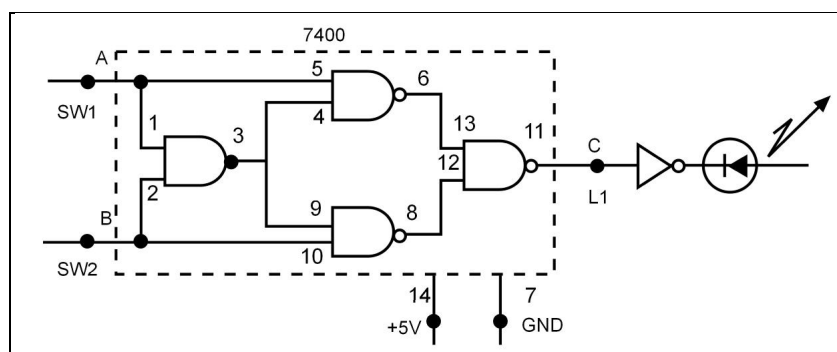

Fig. 2-1 Exclusive OR Circuit for Steps 1 through 3

2. Apply power to the circuit. Using data switches SW1 and SW2, apply the four separate sets of inputs indicated in Table 2-1. For each set of inputs, record the corresponding output-C and complete Table 2-1.

---

3. From the truth table you completed in **Table 4-1**, write the output equation for the circuit you evaluated and record below.

C = _____

From the truth table and the equation you can see that the circuit does perform the _____ logic function.

A	B	C
0	0	
0	1	
1	0	
1	1	

Table 2-1 Truth Table for XOR Gate

4. Mount a 74LS86 IC on the bread-boarding socket. Wire it, as shown in Fig. 2-2. The pin connections for this IC are shown in Fig. 2-3. As in the earlier steps, data switches-SWl and -SW2 will be used to supply the inputs to the circuit. You will monitor the output on LED indicator-Ll.
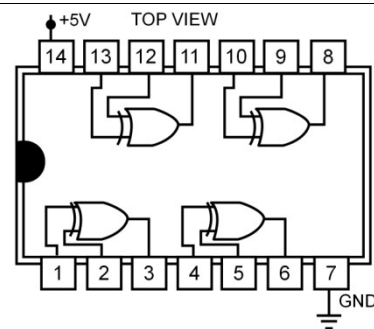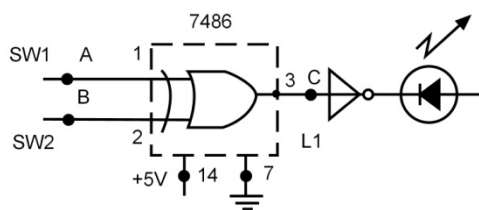

Fig. 2-2 Exclusive NOR Circuit for Steps 4--5   Fig. 2-3 Pin Connections for 74LS86 IC

5. Apply the input states A and B as indicated in Table 2-2 to the experimental circuit. For each set of inputs, monitor the output-C and record the state in the appropriate space in Table 2-2.

Study the truth table and determine what function the circuit is performing.

_____

A	B	C
0	0	
0	1	
1	0	
1	1	

Table 2-2 Truth Table for XOR Gate

6. Construct the circuit shown in Fig. 2-4. The inputs are applied through the data switches (SW1-SW4) and you will observe the outputs on the LED indicators (L1-L4). Switch-SW4 and LED indicator-L4 can be considered to be the LSB of the 4-bit binary input and output words.

7. Set all of the input data switches to the binary 0-state. Observe the output state and record your output value below and in Table 2-3.

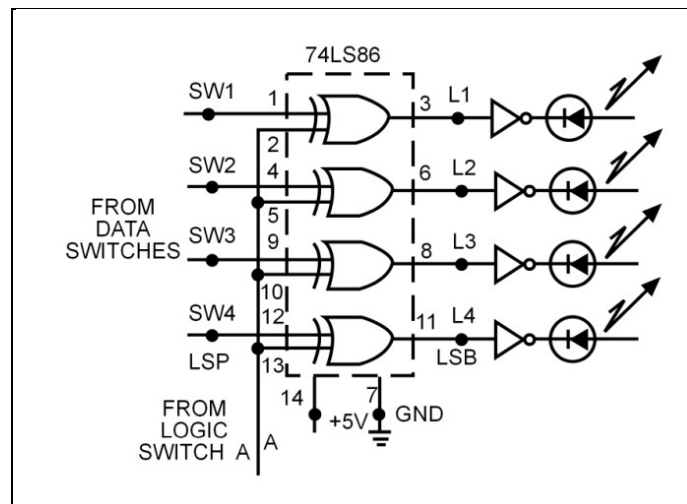**For input = 0000, output = _____**

Fig. 2-4 4-Bit Exclusive-OR Circuit for Steps 6-8

Next, depress the A-logic switch. Again observe the output indicators and record the state presented below and in Table 2-3.

For input = 0000, output = _____

For each of the input states recorded in **Table 4-3**, record the output states with the A logic switch in its normal position and in its depressed position.

8. Study the results in Table 2-3. Using this information and the circuit in Fig. 2-4 plus the results of your previous steps, determine the function of this circuit.

INPUTS				OUTPUTS							
SW 1	SW 2	SW 3	SW 4	A NORMAL				A DEPRESSED			
				L1	L2	L3	L4	L1	L2	L3	L4
0	0	0	0								
1	1	1	1								
1	0	1	0								

Table 2-3 Input /Output Status of X-OR Gate

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